LINEAR TECHNOLOGY

Linear Databook Supplement

EXCLUSIVELY COMMITTED TO LINEAR

The founding theme of Linear Technology Corporation was to create a company capable of leading and directing linear circuit technology and design concepts of the future, and thus become the market's linear specialist. The company believes that the total IC business has become so diverse and so complex that a single company will have great difficulty assembling the engineering talent necessary to lead in all areas of device technology.

Today, the customer base benefits by accessing the best product available in each functional area of the IC market from those vendors who are at the leading edge of performance and technology as a result of their "focused" strategy approach. The customer now has the choice of acquiring the best linear, the best microprocessor, the best memory products, etc., by choosing the best vendor in each area. In order to achieve the goal of becoming the market's first choice in the linear area, LTC has assembled the leading design, test, product, assembly, quality and process engineering talent in the industry, operating in what we feel is the most modern linear integrated circuit facility in production today.

Linear Technology possesses a wide variety of bipolar processes including Super Beta, Bifet, low noise, high speed, thin film resistors, sinkers, sub-surface zeners, and more. The company also has in production a very modern silicon-gate CMOS process, LTCMOS™, which is specifically tailored to satisfy the special needs of linear IC functions.

Linear Technology is committed to servicing the demanding requirements of the Military/Aerospace marketplace. Our 883 DESC Drawing and MIL Drawing programs are designed to consistently provide off-the-shelf high performance linear integrated circuits tested to the requirements of MIL-STD-883 Class B, and fully compliant to Revision C. Our documentation, designs, procedures, and facilities have been carefully established to meet the rigid requirements of MIL-STD-38510 level devices. The company's facility is JAN approved and numerous JAN QPL part types are currently being supplied by Linear Technology. In addition, LTC is committed to supporting the rigorous demands of 'S' level source control drawings to service hi-rel and space applications. All military-grade products are 100% tested at temperature extremes. Both commercial and military outgoing quality levels are sampled over temperature with full lot traceability back to the original wafer from which the device was derived. Presently Linear Technology can boast that its products are used by all of the top 25 largest military contractors in the U.S.

On the commercial side of the business, the company's proprietary products are currently being used by leading manufacturers of automobiles, computers, instruments, cameras, telecommunication systems and in many other areas. The company prides itself in doing business with the major manufacturers and leaders in each of these market segments.

This catalog contains products that already enjoy very wide acceptance status in new and existing end products.

In addition to the commitment to provide better technical solutions, we also commit to our customers that we will strive to make quality and reliability a reason to buy from Linear Technology. Our products address the instrumentation, industrial, data acquisition, peripheral, interface, and military markets with solutions to linear systems application problems.

Linear Technology Corporation

Linear Databook Supplement 1988

NOTE

The 1988 Linear Databook Supplement includes descriptions and specifications for all new products introduced by LTC since the 1986 Linear Databook was published. The index of this supplement lists *all* LTC products, with new products listed in boldface type; data for those not boldfaced can be found in the 1986 publication. Informational sections in this supplement on electrostatic discharge, surface mount devices, military products, packaging, etc., have been updated from the information originally presented in the 1986 volume.

Linear Technology Corporation • 1630 McCarthy Blvd. • Milpitas, CA 95035 • (408) 432-1900 Printed in USA

1988 Linear Databook Supplement

SECTION 1—GENERAL INFORMATION

SECTION 2—OPERATIONAL AMPLIFIERS

SECTION 3—VOLTAGE REGULATORS

SECTION 4—VOLTAGE REFERENCES

SECTION 5—COMPARATORS

SECTION 6—FILTERS

SECTION 7—PULSE-WIDTH MODULATORS

SECTION 8—CMOS/DATA CONVERSION/INTERFACE

SECTION 9—MILITARY PRODUCTS

SECTION 10—NEW PRODUCTS

SECTION 11—SURFACE MOUNT PRODUCTS

SECTION 12—PACKAGE DIMENSIONS

SECTION 13—APPENDICES

SURFACE MOUNT PRODUCTS

SECTION 1—GENERAL INFORMATION

SECTION 1—GENERAL INFORMATION

I. ORDER ENTRY

Orders for products contained herein should be directed to: LINEAR TECHNOLOGY CORPORATION, 1630 McCarthy Boulevard, Milpitas, California 95035. Phone: 408-432-1900.

II. ORDERING INFORMATION

Minimum order value is $2000.00 per order; minimum value per line item is $500.00.

Each item must be ordered using the complete part number exactly as listed on the datasheet.

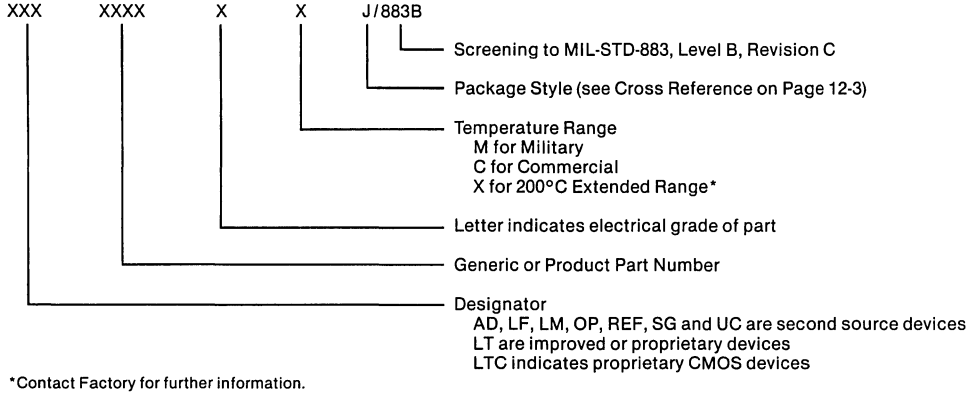
F.O.B.: Milpitas, California.

III. RELIABILITY PROGRAMS

Linear Technology Corporation currently offers the following Reliability Programs:

A. JAN QPL devices.
B. DESC drawings.
C. MIL-STD-883, Level B, Revision C for all military temperature range devices.
D. "R-Flow" Burn-In Program for commercial temperature range devices. Consult Factory regarding burn-in program.

IV. PART NUMBER EXPLANATION



*Contact Factory for further information.

V. PACKAGE SUFFIX EXPLANATION

Letter Designator	Description
D	14, 16, 18 and 20 Pin Side Brazed Hermetic DIP
D8	8 Pin Side Brazed Hermetic DIP
H	Multi Lead Metal Can
J	14, 16, 18 and 20 Pin Ceramic DIP
J8	8 Pin Ceramic DIP
K	TO-3 Metal Can (Steel)
N	14, 16, 18 and 20 Pin Molded DIP
N8	8 Pin Molded DIP
P	TO-247 Molded (3 lead)
S8	8 Lead Small Outline (SO) package (Note 1)
S	16, 18, 20 Pin Small Outline (SO) package (Note 1, 2)
T	TO-220 Molded (3 lead, 5 lead)
Z	TO-92 Molded (3 lead)

Note 1: Pin-out and electrical specifications may differ from standard commercial grade N8 package. See SO datasheet for specific information.

Note 2: These devices are delivered in either 150 MIL (SO) or 300 MIL (SO-L) wide packages depending on device die size. See specific SO datasheet for pin counts and package dimensions.

AMD	
AMD P/N	**LTC DIRECT REPL**
AM686	LT1016
LF155A	LF155A
	LT1055AM*
LF155	LF155
	LT1055M*
LF156A	LF156A
	LT1056AM*
LF156	LF156
	LT1056M*
LF198	LF198
LF355A	LF355A
	LT1055AC*
LF356A	LF356A
	LT1056AC*
LF398	LF398
LM108	LM108
	LT1008M*
LM108A	LM108A
	LT1008M*
LM111	LM111
	LT111A*
	LT1011M*
LM118	LM118
	LT118A*
LM119	LM119
	LT119A*
LM148	LT1014*
LM308A	LM308A
	LT1008C*
LM311	LM311
	LT311A*
	LT1011C*
LM318	LM318
	LT318A*
LM319	LM319
	LT319A*

ANALOG DEVICES	
AD P/N	**LTC DIRECT REPL**
AD101A	LM101A
AD518	LM118**
	LT118A**
AD517	OP07**
	LT1001**
AD510J	OP07E*
	LT1001C*
AD510K	LT1001AC*
AD510L	LT1001AC*
AD510S	OP07A*
	LT1001AM*
ADOP07	OP07
	LT1001M*
ADOP07A	OP07A
	LT1001AM*
ADOP07C	OP07C
	LT1001C*
ADOP07D	OP07D
	LT1001C*
ADOP07E	OP07E
	LT1001C*
AD580	AD580
AD581	AD581
	LT1031**
AD589	LT1004†

FAIRCHILD	
FSC P/N	**LTC DIRECT REPL**
UA101A	LM101A
UA107A	LM107
UA108	LM108
	LT1008M*
UA108A	LM108A
	LT1008M*
UA111	LM111
	LT111A*
	LT1011M*
UA117	LM117
	LT117A*
SH123	LM123
	LT123A*
	LT1003M**
UA124	LT1014M*
UA148	LT1014M*
UA1558M	LT1013M*
UA78H05C	LT1003C**
UA308A	LM308A
	LT1008C**
UA311	LM311
	LT311A*
	LT1011C*
UA317	LM317
	LT317A*
UA318	LM318
	LT318A*
SH323	LM323
	LT323A*
	LT1003M**
UA714	OP07
	LT1001M*
UA714C	OP07C
	LT1001C*
UA714L	OP07D
	LT1001C*
UA714E	OP07E
	LT1001C*

HARRIS	
HARRIS P/N	**LTC DIRECT REPL**
HAOP07	OP07
	LT1001M*

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

HARRIS P/N	LTC DIRECT REPL
HAOP07	OP07
	LT1001AM*
HAOP07C	OP07C
	LT1001C*
HAOP07E	OP07E
	LT1001C*
HA5135-2	OP07
	LT1001M*
HA5130-2	OP07A
	LT1001AM*
HA5135-5	OP07C
	LT1001C*
HA5130-5	OP07E
	LT1001C*
HA2510	LT118A**
	LM118**
HA2512	LT118A**
	LM118A**
HA2515	LT318A**
	LM318**

INTERSIL

INTERSIL P/N	LTC DIRECT REPL
ICL7650 8-Pin	LTC1052*
ICL7652 8-Pin	LTC7652
ICL7660	LTC1044*
ICL8069C	LM385-1.2
	LT1004C-1.2*
ICL8069M	LM185-1.2
	LT1004M-1.2*
LF155A	LF155A
LF155	LF155
LF156A	LF156A
LF156	LF156
LF355A	LF355A
LF356A	LF356A
LH2108A	LH2108A
LH2108	LH2108
LM101A	LM101A
LM107	LM107
LM108	LM108
	LT1008M*
LM108A	LM108A
	LT1008M*
LM111	LM111
	LT111A*
	LT1011M*
LM124	LT1014M*

MOTOROLA

MOTO P/N	LTC DIRECT REPL
LM101A	LM101A
LM107	LM107
LM108	LM108
	LT1008M*
LM108A	LM108A
	LT1008M*

MOTO P/N	LTC DIRECT REPL
LM111	LM111
	LT111A*
	LT1011M*
LM117	LM117
	LT117A*
LM123	LM123
	LT123A*
	LT1003M**
LM137	LM137
	LT137A*
	LT1033M**
LM150	LM150
	LT150A*
LM158	LT1013M*
LM308A	LM308A
	LT1008C*
LM311	LM311
	LT311A*
	LT1011C*
LM317	LM317
	LT317A*
LM323	LM323
	LT323A*
	LT1003C**
LM337	LM337
	LT337A*
	LT1033C**
LM350	LM350
	LT350A*
MC1558	LT1013M*
MC78T05	LM323T
	LT323AT*
MC145406	LT1039**
SG1524	SG1524
	LT1524*
SG1525A	SG1525A
	LT1525A*
SG1527A	SG1527A
	LT1527A*
SG3524	SG3524
	LT3524*
SG3525A	SG3525A
	LT3525A*
SG3527A	SG3527A
	LT3527A*
LF355A	LF355A
LF356A	LF356A
LM148	LT1014M*
LM124	LT1014M*
MC1400U2	LT1019CN8-2.5*
MC1400AU2	LT1019ACN8-2.5*
MC1400U5	LT1019CN8-5*
MC1400AU5	LT1019ACN8-5*
MC1400U10	LT1019CN8-10*
MC1400AU10	LT1019ACN8-10*
LF155A	LF155A
	LT1055AM

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

MOTO P/N	LTC DIRECT REPL
LF155	LF155
	LT1055M
LF156A	LF156A
	LT1056AM
LF156	LF156
	LT1056M
OP27A	OP27A
	LT1007AM*
OP27B	LT1007M*
OP27C	OP27C
	LT1007M
OP27E	OP27E
	LT1007AC*
OP27F	LT1007C*
OP27G	OP27G
	LT1007C*
OP37A	OP37A
	LT1037AM*
OP37B	LT1037M*
OP37C	OP37C
	LT1037M*
OP37E	OP37E
	LT1037AC*
OP37F	LT1037C*
OP37G	OP37G
	LT1037C*

NATIONAL SEMICONDUCTOR

NSC P/N	LTC DIRECT REPL
ADC032	LTC1091
LF155A	LF155A
	LT1055AM*
LF155	LF155
	LT1055M*
LF156A	LF156A
	LT1056AM*
	LT1022AM*
LF156	LF156
	LT1056M*
	LT1022M*
LF198A	LF198A
LF198	LF198
LF355A	LF355A
	LT1055AC*
LF356A	LF356A
	LT1056AC*
	LT1022AC*
LF398A	LF398A
LF398	LF398
LF412A	LF412A
LH0002	LT1010M**
LH0044	LT1001M*
LH0070	LH0070
	LT1031M*
LH2108	LH2108
LH2108A	LH2108A
LM10	LM10

NSC P/N	LTC DIRECT REPL
LM10B	LM10B
LM10C	LM10C
LM101A	LM101A
LM107	LM107
LM108	LM108
	LT1008M*
LM108A	LM108A
	LT1008M*
LM111	LM111
	LT111A*
	LT1011M*
LM112	LT1012M*
LM113	LT1004M-1.2*
LM117	LM117
	LT117A*
LM117HV	LM117HV
	LT117AHV*
LM118	LM118
	LT118A*
LM119	LM119
	LT119A*
LM123	LM123
	LT123A*
	LT1003M*
LM124	LT1014M*
LM129A	LM129A
LM129B	LM129B
LM129C	LM129C
LM133	LT1033M*
LM134	LM134
LM134-3	LM134-3
LM134-6	LM134-6
LM136A	LM136A
	LT1009M*
LM136-2.5	LM136-2.5
	LT1009M*
LM136-5	LT1029M**
LM137	LM137
	LT137A
	LT1033M**
LM137HV	LM137HV
	LT137AHV*
LM138	LM138
	LT138A*
LM148	LT1038M**
LM150	LM150
	LT150A*
LM158	LT1013M*
LM168BY-5.0	LT1019AM-5*
LM168BY-10.0	LT1019AM-10*
LM185-1.2	LM185-1.2
	LT1004M-1.2*
LM185-2.5	LM185-2.5
	LT1004M-2.5*
LM185BX-1.2	LT1034BM-1.2*
LM185BY-1.2	LT1034M-1.2*
LM185BX-2.5	LT1034BM-2.5*
LM185BY-2.5	LT1034M-2.5*

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

NSC P/N	LTC DIRECT REPL
LM196	LT1038M**
LM199	LM199
LM199A	LM199A
LM199A-20	LM199A-20
LM234-3	LM234-3
LM234-6	LM234-6
LM308A	LM308A
	LT1008C*
LM311	LM311
	LT311A*
	LT1011C*
LM317	LM317
	LT317A*
LM317HV	LM317HV
	LT317AHV*
LM318	LM318
	LT318A*
LM319	LM319
	LT319A*
LM323	LM323
	LT323A*
	LT1003C**
LM329A	LM329A
LM329B	LM329B
LM329C	LM329C
LM329D	LM329D
LM333	LT1033C*
LM333A	LT1033C
LM334	LM334
LM336-2.5	LM336
	LT1009C*
LM336B-2.5	LM336B
	LT1009C*
LM336-5	LT1029C*
LM337	LM337
	LT337A*
	LT1033C*
LM337HV	LM337HV
	LT337AHV*
LM338	LM338
	LT338A*
LM350	LM350
	LT350A*
LM368Y-5.0	LT1019AC-5*
LM368-5.0	LT1019AC-5*
LM368Y-10.0	LT1019AC-10*
LM368-10.0	LT1019AC-10*
LM385-1.2	LM385-1.2
	LT1004C-1.2*
LM385-2.5	LM385-2.5
	LT1004C-2.5*
LM385BX-1.2	LT1034BC-1.2*
LM385BY-1.2	LT1034C-1.2*
LM385BX-2.5	LT1034BC-2.5*
LM385BY-2.5	LT1034C-2.5*
LM396	LT1038C**
LM399	LM399

NSC P/N	LTC DIRECT REPL
LM399A	LM399A
LM399A-20	LM399A-20
LM399A-50	LM399A-50
LM1524	SG1524
	LT1524*
LM3524	SG3524
	LT3524*
LM2935	LT1005**
MF5	LTC1059*
MF10	LTC1060*

PMI

PMI P/N	LTC DIRECT REPL
CMP01	LT1011**
CMP02	LT1011**
OP04	LT1013*
OP05	OP05
	LT1001M*
OP05A	OP05A
	LT1001M*
OP05C	OP05C
	LT1001C*
OP05E	OP05E
	LT1001C*
OP07	OP07
	LT1001M*
OP07A	OP07A
	LT1001AM*
OP07C	OP07C
	LT1001C*
OP07E	OP07E
	LT1001C*
OP10	LT1002M*
OP10A	LT1002AM*
OP10C	LT1002C*
OP10E	LT1002C
OP11	LT1014*
OP12A	LT1012M*
OP12B	LT1012M*
OP12C	LT1012M*
OP12E	LT1012C*
OP12F	LT1012C*
OP12G	LT1012C*
OP15A	OP15A
	LT1055AM*
OP15B	OP15B
	LT1055M
OP15C	OP15C
	LT1055M*
OP15E	OP15E
	LT1055AC*
OP15F	OP15F
	LT1055C*
OP15G	OP15G
	LT1055C*
OP16A	OP16A
	LT1056AM*

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

PMI P/N	LTC DIRECT REPL
OP16B	OP16B
	LT1056M*
OP16C	OP16C
	LT1056M*
OP16E	OP16E
	LT1056AC*
OP16F	OP16F
	LT1056C*
OP16G	OP16G
	LT1056C*
OP27A	OP27A
	LT1007AM*
OP27B	LT1007M*
OP27C	OP27C
	LT1007M*
OP27E	OP27E
	LT1007AC*
OP27F	LT1007C*
OP27G	OP27G
	LT1007C*
OP37A	OP37A
	LT1037AM*
OP37B	OP37A
	LT1037M*
OP37C	OP37C
	LT1037M*
OP37E	OP37E
	LT1037AC*
OP37F	OP37E
	LT1037C*
OP37G	OP37G
	LT1037C*
OP77A	LT1001AM**
OP77B	LT1001M**
OP77E	LT1001AC**
OP77F	LT1001C**
OP77G	LT1001C**
OP207A	LT1002M*
OP207B	LT1002M*
OP207E	LT1002C*
OP207F	LT1002C*
OP215A	OP215A
	LT1057AM*
OP215B	OP215A*
	LT1057AM*
OP215C	OP215C
	LT1057M*
OP215E	OP215E
	LT1057C*
OP215F	OP215E*
	LT1057C*
OP215G	OP215G
	LT1057C*
OP221	LT1013*
OP227A	OP227A
OP227B	OP227A
OP227C	OP227C
OP227E	OP227E

PMI P/N	LTC DIRECT REPL
OP227F	OP227E
OP227G	OP227G
OP400A	LT1014AM**
OP400E	LT1014AC**
OP400F	LT1014AC**
OP421	LT1014*
PM108	LM108
	LT1008M*
PM108A	LM108A
	LT1008M*
PM155A	LF155A
	LT1055M*
PM155	LF155
	LT1055M*
PM1008	LT1008
PM1558	LT1013M*
PM156A	LF156A
	LT1056M*
PM156	LF156
	LT1056M*
PM2108A	LH2108A
PM2108	LH2108
PM308A	LM308A
	LT1008C*
PM355A	LF355A
	LT1055C*
PM356A	LF356A
	LT1056C*
REF01	REF01
	LT1019M-10*
	LT1021-10**
REF01A	REF01A
	LT1021-10**
REF01C	REF01C
	LT1019C-10*
	LT1021-10**
REF01E	REF01E
	LT1021-10**
REF01H	REF01H
	LT1019C-10*
	LT1021-10**
REF02	REF02
	LT1019M-5*
	LT1021-5**
REF02A	REF02A
	LT1021-5**
REF02C	REF02C
	LT1019C-5*
	LT1021-5**
REF02D	LT1019C-5*
	LT1021-5**
REF02E	REF02E
	LT1021-5**
REF02H	REF02H
	LT1019C-5*
	LT1021-5**

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

RAYTHEON	
RAYTH P/N	**LTC DIRECT REPL**
LM101A	LM101A
LM107	LM107
LM111	LM111
	LT111A*
	LT1011M*
LM124	LT1014M*
LM148	LM1014M*
LM311	LM311
	LT311A*
	LT1011C*
OP05	OP05
	LT1001M*
OP05A	OP05A
	LT1001AM*
OP05C	OP05C
	LT1001C*
OP05E	OP05E
	LT1001C*
OP07	OP07
	LT1001M*
OP07A	OP07A
	LT1001AM*
OP07C	OP07C
	LT1001C*
OP07E	OP07E
	LT1001C*
OP27A	OP27A
	LT1007AM*
OP27B	OP27A
	LT1007M
OP27C	OP27C
	LT1007M*
OP27E	OP27E
	LT1007AC*
OP27F	OP27F
	LT1007C*
OP27G	OP27G
	LT1007C*
OP37A	OP37A
	LT1037AM*
OP37B	OP37A
	LT1037M
OP37C	OP37C
	LT1037M*
OP37E	OP37E
	LT1037AC*
OP37F	OP37E
	LT1037C*
OP37G	OP37G
	LT1037C*
RC714CH	OP07C
	LT1001C*
RC714EH	OP07E
	LT1001C*
RM1558	LT1013M*
RM714H	OP07
	LT1001M*

SIGNETICS	
SIGNETICS P/N	**LTC DIRECT REPL**
LF398	LF398
LF398A	LF398A
LM101A	LM101A
LM111	LM111
	LT111A*
	LT1011M*
LM119	LM119
	LT119A*
LM124	LT1014M*
LM158	LT1013M*
LM311	LM311
	LT311A*
	LT1011C*
MC1558	LT1013M*
NE1037	LT1037
NE5534	OP37*
	LT1037*
NE5534A	OP37*
	LT1037*
SE5534	OP37*
	LT1037*
SE5534A	OP37*
	LT1037*
SG3524	SG3524
	LT3524*

SILICON GENERAL	
SIL GEN P/N	**LTC DIRECT REPL**
SG101A	LM101A
SG108	LM108
	LT1008M*
SG108A	LM108A
	LT1008M*
SG111	LM111
	LT111A
	LT1011M*
SG117	LM117
SG117A	LT117A
SG123	LM123
SG123A	LT123A
	LT1003M**
SG124	LT1014M*
SG137	LM137
SG137A	LT137A
	LT1033M**
SG138	LM138
SG138A	LT138A
SG150	LM150
SG150A	LT150A
SG1558	LT1013M*
SG311	LM311
	LT311A*
	LT1011C*
SG317	LM317
SG317A	LT317A
SG323	LM323

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

SIL GEN P/N	LTC DIRECT REPL
SG323A	LT323A
	LT1003C**
SG337	LM337
SG337A	LT337A
	LT1033C**
SG338	LM338
SG338A	LT338A
SG350	LM350
SG350A	LT350A
SG1524	SG1524
	LT1524*
SG1525A	SG1525A
	LT1525A*
SG1526	LT1526
SG1527A	SG1527A
	LT1527A*
SG3524	SG3524
	LT3524*
SG3525A	SG3525A
	LT3525A*
SG3526	LT3526
SG3527A	SG3527A*
	LT3527A*

TEXAS INSTRUMENTS

TI P/N	LTC DIRECT REPL
LM101A	LM101A
LM107	LM107
LM111	LM111
	LT111A*
	LT1011M*
LM124	LT1014M*
LM148	LT1014M*
LM158	LT1013M*
LM311	LM311
	LT311A*
	LT1011C*
LM317KC	LM317T
	LM317AT*
LM318	LM318
	LT318A*
LM323	LM323
	LT323A*

TI P/N	LTC DIRECT REPL
LM350	LM350
	LT350A*
LT1009	LT1009
LT1011	LT1011
LT1007	LT1007
LT1037	LT1037
LT1070	LT1070
LTC1044	LTC1044
MC1558	LT1013M*
OP07/714C	OP07C
	LT1001C*
OP07/714D	OP07D
	LT1001C*
OP07/714E	OP07E
	LT1001C*
OP27A	OP27A
	LT1007AM*
OP27B	LT1007M*
OP27C	OP27C
	LT1007M
OP27E	OP27E
	LT1007AC*
OP27F	LT1007C*
OP27G	OP27G
	LT1007C*
OP37A	OP37A
	LT1037AM*
OP37B	LT1037M*
OP37C	OP37C
	LT1037M*
OP37E	OP37E
	LT1037AC*
OP37F	LT1037C*
OP37G	OP37G
	LT1037C*
SG1524	SG1524
	LT1524*
SG1525A	SG1525A
	LT1525A*
SG3524	SG3524
	LT3524*
SG3525A	SG3525A
	LT3525A*

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

UNITRODE	
UNITRODE P/N	**LTC DIRECT REPL**
UC117	LM117
	LT117A*
UC137	LM137
	LT137A*
	LT1033M**
UC150	LM150
	LT150A*
UC317	LM317
	LT317A*
UC337	LM337
	LT337A*
	LT1033C**
UC350	LM350
	LT350A*

UNITRODE P/N	LTC DIRECT REPL
UC1524	SG1524
	LT1524*
UC1525A	SG1525A
	LT1525A*
UC1527A	SG1527A
	LT1527A*
UC1846	UC1846
UC1847	UC1847
UC3524	SG3524
	LT3524*
UC3525A	SG3525A
	LT3525A*
UC3527A	SG3527A
	LT3527A*
UC3846	UC3846
UC3847	UC3847

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.
†Consult factory for guaranteed TC devices.

SECTION 2—OPERATIONAL AMPLIFIERS

SECTION 2—OPERATIONAL AMPLIFIERS

MILITARY

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (NA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
SINGLE								
LT1001AM	15	0.6	2.0	450	0.15	18	H, J8	Extremely Low Offset Voltage Low Noise, Low Drift
LT1001M	60	1.0	3.8	400	0.15	18	H, J8	
LT1006AM	50	1.3	15	1000	0.25	24†	H, J8	Single Supply Operation, Fully Specified for +5V Supply
LT1006M	80	1.8	25	700	0.25	24†	H, J8	
LT1007AM	25	0.6	35	7000	1.7	4.5	H, J8	Extremely Low Noise, Low Drift
LT1007M	60	1.0	55	5000	1.7	4.5	H, J8	
LT1008M	120	1.5	0.1	200	0.1	30	H	Low Bias Current, Low Power
LT1010M	90mV	0.6mV/°C†	150μA	0.995	75	90†	H, K	High Speed Buffer, Drives ±10V into 75Ω.
LT1012M	35	1.5	0.1	200	0.1	30	H	Low V_{OS}, Low Power
LT1022AM	250	5.0	0.05	150	23	50	H	Very High Speed JFET Input Op Amp with Very Good DC Specs.
LT1022M	600	9.0	0.05	120	18	60	H	
LT1028AM	40	0.8	90	7000	11	1.7	H, J8	Lowest Noise, High Speed, Low Drift
LT1028M	80	1.0	180	5000	11	1.9	H, J8	
LT1037AM	25	0.6	35	7000	11	4.5	H, J8	Extremely Low Noise, High Speed
LT1037M	60	1.0	55	5000	11	4.5	H, J8	
LT1055AM	150	4	0.05	150	10	50	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055M	400	8	0.05	120	7.5	60	H	
LT1056AM	180	4	0.05	150	12	50	H	
LT1056M	450	8	0.05	120	9	60	H	
LTC1052M	5	0.05	0.03	1000	3†	0.5μVp-p**	H	Chopper, Stabilized Low Noise
LF155A	2000	5	0.05	75	5	25†*	H	JFET Inputs, Low I Bias, No Phase Reversal, Guaranteed TC V_{OS} on all Grades
LF155	3500	15	0.10	50	5	25†*	H	
LF156A	2000	5	0.05	75	10	15†*	H	
LF156	3500	15	0.10	50	9	15†*	H	
LM10	2000	2†	20	120		50†	H, J8	On-Chip Reference Operates with +1.2V Single Battery
LM101A	2000	15	75	25	0.3	28†	H, J8	Uncompensated Gen. Purp.
LM107	2000	15	75	25	0.3	28†	H, J8	Compensated Gen. Purp.
LM108A	500	5	2	40	0.1	30†	H	Low Bias Current, Low Supply Current
LM108	2000	15	3	25	0.1	30†	H	
LM118	4000		250	25	50	42†	H	High Speed, 15MHz
LT118A	1000		250	200	50	42†	H, J8	High Speed, 15MHz
OP-05A	150	0.9	2	300	0.1	18	H, J8	Low Noise, Low Offset Drift with Time
OP-05	500	2.0	3	200	0.1	18	H, J8	
OP-07A	25	0.6	2	300	0.1	18	H, J8	Low Initial Offset, Low Noise, Low Drift
OP-07	75	1.3	3	200	0.1	18	H, J8	
OP-15A	500	5	0.05	100	10	20†*	H	Precision JFET Input, Low I Bias, No Phase Reversal
OP-15B	1000	10	0.1	75	7.5	20†*	H	
OP-15C	3000	15	0.2	50	5	20†*	H	
OP-16A	500	5	0.5	100	18	20†*	H	Precision JFET Input, High Speed, No Phase Reversal
OP-16B	1000	10	0.1	75	12	20†*	H	
OP-16C	3000	15	0.2	50	9	20†*	H	
OP-27A	25	0.6	40	1000	1.7	5.5	H, J8	Very Low Noise, Unity Gain Stable
OP-27C	100	1.8	80	700	1.7	8.0	H, J8	
OP-37A	25	0.6	40	1000	11	5.5	H, J8	Very Low Noise, Stable for Gains ≥5
OP-37C	100	1.8	80	700	11	8.0	H, J8	
DUAL								
LT1002AM	60	0.9	3.0	400	0.15	20	J	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002M	100	1.3	4.5	350	0.15	20	J	
LT1013AM	150	2.0	20	1500	0.2	24†	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013M	300	2.5	30	1200	0.2	24†	H, J8	
LT1057AM	450	7	0.05	150	10	75	H, J8	Low Offset, JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057M	800	12	0.075	100	8	80	H, J8	
LF412AM	1000	10	0.1	100	10	20†*	H, J8	High Performance Dual JFET Input Op Amp
LH2108A	500	5.0	2	40	0.1	30†	D	Dual, Low Bias Current, Side Brazed Package
LH2108	2000	15.0	2	25	0.1	30†	D	

MILITARY

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (NA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
DUAL								
OP-215A	1000	10	0.1	150	10	20†*	H, J8	High Performance Dual JFET Input Op Amp
OP-215C	3000	20	0.2	50	8	20†*	H, J8	
OP-227A	80	1.0	40	3000	1.7	6	J	Dual Matched OP-27
OP-227C	180	1.8	80	2000	1.7	9	J	
OP-237A	80	1.0	40	3000	10	6	J	Dual Matched OP-37
OP-237C	180	1.8	80	2000	10	9	J	
QUAD								
LT1014AM	180	2.0	20	1500	0.2	24†	J	Precision Quad Op Amp in 14-Pin Package
LT1014M	300	2.5	30	1200	0.2	24†	J	
LT1058AM	600	10	0.05	150	10	75	J	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058M	1000	15	0.075	100	8	80	J	

† Typical Spec *100 Hz Noise **DC to 1 Hz Noise

COMMERCIAL

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (NA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
SINGLE								
LT1001AC	25	0.6	2.0	450	0.15	18	H, J8, N8	Extremely Low Offset Voltage Low Noise, Low Drift
LT1001C	60	1.0	3.8	400	0.15	18	H, J8, N8, S8	
LT1006AC	50	1.3	15	1000	0.25	24†	H, J8, N8	Single Supply Operation, Fully Specified for +5V Supply
LT1006C	80	1.8	25	700	0.25	24†	H, J8, N8	
LT1007AC	25	0.6	35	7000	1.7	4.5	H, J8, N8	Extremely Low Noise, Low Drift
LT1007C	60	1.0	55	5000	1.7	4.5	H, J8, N8	
LT1008C	120	1.5	0.1	200	0.1	30	H, N8	Low Bias Current, Low Power
LT1010C	100mV	0.6mV/°C†	250μA	0.995	75	90†	H, K, T	High Speed Buffer, Drives ±10V into 75Ω.
LT1012C	50	1.5	0.15	200	0.1	30	H, N8	Low V_{OS}, Low Power
LT1012S8	120	1.8	0.28	200	0.1	30	S8	
LT1022AC	250	5.0	0.05	150	23	50	H	Very High Speed JFET Input Op Amp with Very Good DC Specs
LT1022CH	600	9.0	0.05	120	18	60	H	
LT1022CN8	1000	15.0	0.05	100	18	60	N8	
LT1028AC	40	0.8	90	7000	11	1.7	H, J8, N8	Lowest Noise, High Speed, Low Drift
LT1028C	80	1.0	180	5000	11	1.9	H, J8, N8	
LT1037AC	25	0.6	35	7000	11	4.5	H, J8, N8	Extremely Low Noise, High Speed
LT1037C	60	1.0	55	5000	11	4.5	H, J8, N8	
LT1055AC	150	4	0.05	150	10	50	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055C	400	8	0.05	120	7.5	60	H	
LT1055CN8	700	12	0.05	120	7.5	60	N8	
LT1055S8	1500	15	0.1	120	7.5	70	S8	
LT1056AC	180	4	0.05	150	12	50	H	
LT1056C	450	8	0.05	120	9	60	H	
LT1056CN8	800	12	0.05	120	9	60	N8	
LT1056S8	1500	15	0.1	120	9.0	70	S8	
LTC1052C	5	0.05	0.03	1000	3†	0.5μVp-p**	H, N8	Chopper Stabilized, Low Noise
LTC7652C	5	0.05	0.03	1000	3†	0.5μVp-p**	H, N8	
LF355A	2000	5	0.05	75	5	25†*	H, N8	JFET Inputs, Low I Bias, No Phase Reversal
LF356A	2000	5	0.05	75	10	15†*	H, N8	
LM10B	2000	2†	20	120	—	50†	H, J8	On-Chip Reference, Operates with +1.2V Single Battery
LM10BL	2000	2†	20	60	—	50†	H, J8	
LM10C	4000	5†	30	80	—	50†	H, J8, N8	
LM10CL	4000	5†	30	40	—	50†	H, J8, N8	
LM308A	500	5	7	60	0.1	30†	H, N8	Low Bias, Supply Current
LT318A	1000		250	200	50	42†	H, J8, N8	High Speed, 15MHz
LM318	10000		500	25	50	42†	H, J8, N8, S8	High Speed, 15MHz
OP-05C	1300	4.5	7	120	0.1	20	H, J8, N8	Low Noise, Low Offset Drift with Time
OP-05E	500	2.0	4	200	0.1	18	H, J8, N8	

COMMERCIAL

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (NA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/$\sqrt{Hz}$)	PACKAGES AVAILABLE	
SINGLE								
OP-07C	150	1.8	7	120	0.1	20	H, J8, N8, S8	Low Initial Offset, Low Noise, Low Drift
OP-07E	75	1.3	4	200	0.1	18	H, J8, N8	
OP-15E	500	5	0.05	100	10	20†*	H, N8	Precision JFET Input, Low I Bias, No Phase Reversal
OP-15F	1000	10	0.1	75	7.5	20†*	H, N8	
OP-15G	3000	15	0.2	50	5	20†*	H, N8	
OP-16E	500	5	0.05	100	18	20†*	H, N8	Precision JFET Input, High Speed, No Phase Reversal
OP-16F	1000	10	0.1	75	12	20†*	H, N8	
OP-16G	3000	15	0.2	50	9	20†*	H, N8	
OP-27E	25	0.6	40	1000	1.7	5.5	H, J8, N8	Very Low Noise, Unity Gain Stable
OP-27G	100	1.8	80	700	1.7	8.0	H, N8	
OP-37E	25	0.6	40	1000	11	5.5	H, J8, N8	Very Low Noise, Stable for Gains ≥5
OP-37G	100	1.8	80	700	11	8.0	H, N8	
DUAL								
LT1002AC	60	0.9	3.0	400	0.15	20	J, N	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002C	100	1.3	4.5	350	0.15	20	J, N	
LT1013AC	150	2.0	20	1500	0.2	24†	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013C	300	2.5	30	1200	0.2	24†	H, J8, N8	
LT1013D	800	5.0	30	1200	0.2	24†	N8, S8	
LT1057AC	450	7	0.05	150	10	75	H, J8	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057ACN8	450	10	0.05	150	10	75	N8	
LT1057C	800	12	0.075	100	8	80	H, J8	
LT1057CN8	800	16	0.075	100	8	80	N8	
LF412AC	1000	10	0.1	100	10	20†*	H, J8, N8	High Performance Dual JFET Input Op Amp
OP-215E	1000	10	0.1	150	10	20†*	H, J8, N8	
OP-215G	3000	20	0.2	50	8	20†*	H, J8, N8	
OP-227E	80	1.0	40	3000	1.7	6	J, N	Dual Matched OP-27
OP-227G	180	1.8	80	2000	1.7	9	J, N	
OP-237E	80	1.0	40	3000	10	6	J, N	Dual Matched OP-37
OP-237G	180	1.8	80	2000	10	9	J, N	
QUAD								
LT1014AC	180	2.0	20	1500	0.2	24†	J	Precision Quad Op Amp in 14-Pin Package
LT1014C	300	2.5	30	1200	0.2	24†	J, N	
LT1014D	800	5.0	30	1200	0.2	24†	N	
LT1058AC	600	10	0.05	150	10	75	J	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058ACN	600	15	0.05	150	10	75	N	
LT1058C	1000	15	0.075	100	8	80	J	
LT1058CN	1000	22	0.075	100	8	80	N	

† Typical Spec * 100 Hz Noise * * DC to 1 Hz Noise

SELECTION BY DESIGN PARAMETER

Max Input Offset Voltage (T_A = 25°C)

≤15μV	≤25μV	≤75μV	≤150μV	≤1mV	≤5mV	≤10mV
LT1001AM	LT1001AC	LT1001	LT1002	LT1013	LT1055S8	LM301A
LTC7652	LT1007A	LT1002A	LT1006	LT1014	LT1056S8	LM307
LTC1052	LT1037A	LT1006A	LT1008	LT1014A	LT118A	LM308
	OP-07A	LT1007	LT1012S8	LT1022 ALL	LT318A	LM318
	OP-27A	LT1012	LT1013A	LT1055C	LF155A	
	OP-27E	LT1012S8	LT1028	LT1055M	LF155	
	OP-37A	LT1037	LT1055AM	LT1056AM	LF156A	
	OP-37E	OP-07E	LT1055AC	LT1056AC	LF156	
		OP-07	OP-05A	LT1056M	LF355A	
			OP-07C, D	LT1056C	LF355	
			OP-27C	LT1057 ALL	LH2108	
			OP-37C	LT1058 ALL	LM10	
			OP-227A, E	LF412A	LM10B, BL	
			OP-237A, E	LH2108A	LM10C, CL	
				LM108A	LM101A	
				LM308A	LM107	
				OP-05	LM108	
				OP-05E	LM118	
				OP-15A, E	OP-05C	
				OP-15B, F	OP-15C, G	
				OP-16A, E	OP-16C, G	
				OP-16B, F	OP-215C, G	
				OP-215A, E		

Max Input Bias Current (T_j = 25°C)

≤0.2nA	≤3nA	≤5nA	≤10nA	≤50nA	≤100nA	>200nA
LT1008	LT1001A	LT1001	OP-05C	LT1007A	LT1007	LT118A
LT1012	LT1002A	LT1002	OP-07	LT1013A	LT1028	LT318A
LT1022 ALL	LT1006 ALL	OP-05E	LM308A	LT1013	LT1037	LM301A
LT1055 ALL	LM108	OP-07E		LT1014A	LM101A	LM307
LT1056 ALL	LM108A			LT1014	LM107	LM118
LT1057 ALL	OP-05A			LT1028A	OP-27C, G	LM318
LT1058 ALL	OP-05			LT1037	OP-37C, G	
LF155 ALL	OP-07A			LM10 (ALL)	OP-227C, G	
LF156 ALL	OP-07			OP-27A, E	OP-237C, G	
LF412A ALL				OP-37A, E		
LTC7652				OP-227A, E		
LTC1052				OP-237A, E		
OP-15 ALL						
OP-16 ALL						
OP-215 ALL						

SELECTION BY DESIGN PARAMETER

Typ Equivalent Input Noise Voltage per $\sqrt{Hz}$, f = 10Hz, R_S = 100Ω

≤1nV/$\sqrt{Hz}$	≤25nV/$\sqrt{Hz}$
LT1028 ALL	LT1001 ALL
	LT1002 ALL
	LT1006 ALL
	LT1008
	LT1012
	LT1013 ALL
	LT1014 ALL
	LT1022 ALL
	LTC1052
	*LT1055 ALL
	*LT1056 ALL
	LTC7652
	*LF155 ALL
≤5nV/$\sqrt{Hz}$	*LF355 ALL
	*LF156 ALL
LT1007 ALL	OP-05 ALL
LT1037 ALL	OP-07 ALL
	*OP-15 ALL
	*OP-16 ALL
	OP-27 ALL
	OP-37 ALL
	OP-227 ALL
	OP-237 ALL

*100Hz Noise

Typ Slew Rate

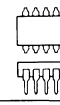
≤1V/μs	≥2V/μs	≥10V/μs	≥50V/μs
LT1001 ALL	LT1007 ALL	LT1022 ALL	LT118A/318A
LT1002 ALL	LT1056M	LT1028 ALL	LM118/318
LT1006 ALL	LT1056C	LT1037 ALL	LT1010
LT1008	LT1057	LT1055 ALL	
LT1012	LT1058	LT1056A	
LT1013 ALL	OP-27 ALL	OP-37 ALL	
LT1014 ALL	OP-15 ALL	OP-16A, B	
LH2108 ALL	OP-16C, G	OP-16E, F	
OP-05	OP-215B, C, F, G	OP-237 ALL	
OP-07	OP-227 ALL	LF412A	
LM101A/301A	LF155 ALL	OP-215A, E	
LM107/307	LF355 ALL	LT1057A	
LM108/308	LF156 ALL	LT1058A	
LM108A/308A	LF356 ALL		

Gain

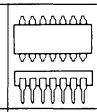
≥15 $\frac{V}{mV}$	≥50 $\frac{V}{mV}$	≥200 $\frac{V}{mV}$	≥1000 $\frac{V}{mV}$
LM301A	LT1022 ALL	LT1001	LT1006A
LM307	LT1055 ALL	LT1002	LT1007
LM308	LT1056 ALL	LT1006	LT1013
LM318	LM101A	LT1008	LT1014
	LM107	LT1012	LT1028
	LM108	LT118A	LT1037
	LM118	LT318A	OP-27
	LM10	OP-05	OP-37
		OP-07	OP-227
			OP-237
			LTC1052
			LTC7652

Packages

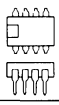
H
TO-5
8 LEAD
10 LEAD



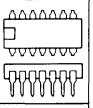
J8
HERMETIC
DIP
8 LEAD



J
HERMETIC
DIP
14 LEAD
16 LEAD
18 LEAD



N8
PLASTIC
DIP
8 LEAD



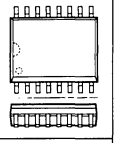
N
PLASTIC
DIP
14 LEAD
16 LEAD
18 LEAD

D8
HERMETIC
DIP
8 LEAD

D
HERMETIC
DIP
14 LEAD
16 LEAD
18 LEAD

S8
PLASTIC
SO
8 LEAD

S
PLASTIC
SO
14 LEAD
16 LEAD



S
PLASTIC
SOL
16 LEAD
18 LEAD
20 LEAD

Precision, Single Supply Op Amp

FEATURES

- Single Supply Operation
  Input Voltage Range Extends to Ground
  Output Swings to Ground while Sinking Current
- *Guaranteed* Offset Voltage 50μV Max.
- *Guaranteed* Low Drift 1.3μV/°C Max.
- *Guaranteed* Offset Current 0.5nA Max.
- *Guaranteed* High Gain
  5mA Load Current 1.5 Million Min.
  17mA Load Current 0.8 Million Min.
- *Guaranteed* Low Supply Current 520μA Max.
- Supply Current can be Reduced by a Factor of 4
- Low Voltage Noise, 0.1Hz to 10Hz 0.55μVp-p
  Low Current Noise—
  Better than OP-07 0.07pA/$\sqrt{Hz}$ at 10Hz
- High Input Impedance 250MΩ Min.
- *Guaranteed* Minimum Supply Voltage 2.7V Min.

APPLICATIONS

- Low Power Sample and Hold Circuits
- Battery Powered Precision Instrumentation
  Strain Gauge Signal Conditioners
  Thermocouple Amplifiers
- 4mA–20mA Current Loop Transmitters
- Active Filters

DESCRIPTION

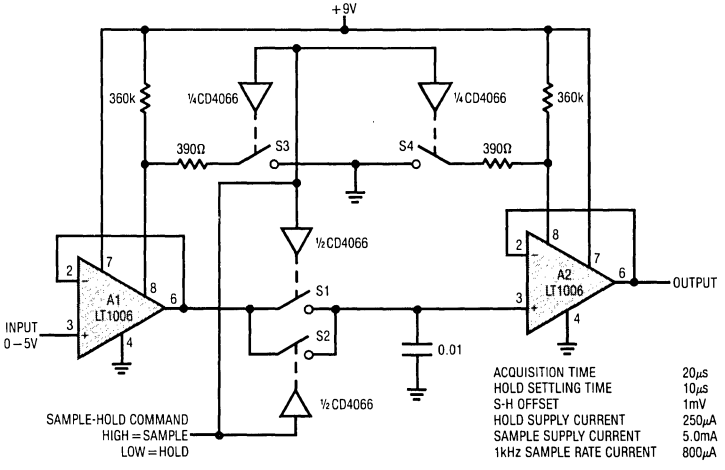
The LT1006 is the first precision single supply operational amplifier. Its design has been optimized for single supply operation with a full set of specifications at 5V. Specifications at ± 15V are also provided.

The LT1006 has low offset voltage of 20μV, drift of 0.2μV/°C, offset current of 120pA, gain of 2.5 million, common-mode rejection of 114dB, and power supply rejection of 126dB.

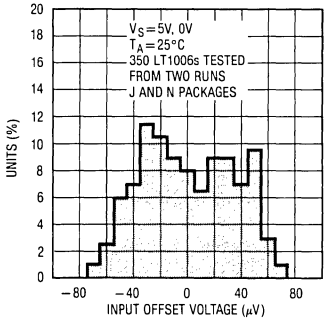
Although supply current is only 340μA, a novel output stage can source or sink in excess of 20mA while retaining high voltage gain. Common-mode input range includes ground to accommodate low ground-referenced inputs from strain gauges or thermocouples, and output can swing to within a few millivolts of ground. If higher slew rate (in excess of 1V/μs) or micropower operation (supply current down to 90μA) is required, the operating currents can be modified by connecting an external optional resistor to Pin 8.

For similar single supply precision dual and quad op amps, please see the LT1013/LT1014 data sheet.

LT1006 Single Supply, Micropower Sample and Hold



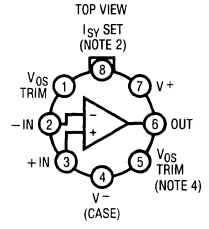
Distribution of Input Offset Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage ..... Equal to Positive Supply Voltage
..... 5V Below Negative Supply Voltage
Differential Input Voltage..... 30V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1006AM, M ..... –55°C to 125°C
LT1006AC, C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

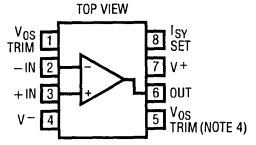
PACKAGE/ORDER INFORMATION



H8 PACKAGE TO-5 METAL CAN

ORDER PART NUMBER

LT1006AMH
LT1006MH
LT1006ACH
LT1006CH



J8 PACKAGE HERMETIC DIP
N8 PACKAGE PLASTIC DIP

LT1006AMJ8
LT1006MJ8
LT1006ACJ8
LT1006CJ8
LT1006CN8

ELECTRICAL CHARACTERISTICS $V_S = 5V$, $V_{CM} = 0V$, $V_{OUT} = 1.4V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM/AC MIN	LT1006AM/AC TYP	LT1006AM/AC MAX	LT1006M/C MIN	LT1006M/C TYP	LT1006M/C MAX	UNITS
V_{OS}	Input Offset Voltage			20	50		30	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.4			0.5		μV/Mo
I_{OS}	Input Offset Current			0.12	0.5		0.15	0.9	nA
I_B	Input Bias Current			9	15		10	25	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.55			0.55		μVp-p
	Input Noise Voltage Density	f_O = 10Hz (Note 3) f_O = 1000Hz (Note 3)		23 22	32 25		23 22	32 25	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz		0.07			0.08		pA/√Hz
	Input Resistance Differential Mode Common-Mode	(Note 1)	 180	 400 5		 100	 300 4		 MΩ GΩ
	Input Voltage Range		3.5 0	3.8 –0.3		3.5 0	3.8 –0.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V	100	114		97	112		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V, V_O = 0V	106	126		103	124		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.03V to 4V, R_L = 10k V_O = 0.03V to 3.5V, R_L = 2k	1.0 0.5	2.5 2.0		0.7 0.3	2.0 1.8		V/μV V/μV
	Maximum Output Voltage Swing	Output Low, No Load Output Low, 600Ω to GND Output Low, I_{SINK} = 1mA Output High, No Load Output High, 600Ω to GND	 4.0 3.4	15 5 220 4.4 4.0	25 10 350	 4.0 3.4	15 5 220 4.4 4.0	25 10 350	mV mV mV V V
SR	Slew Rate		0.25	0.4		0.25	0.4		V/μs
I_S	Supply Current	R_{SET} = ∞ R_{SET} = 180k Pin 8 to Pin 7 (Note 2)		340 90	520		350 90	570	μA μA
	Minimum Supply Voltage		2.7			2.7			V

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1006AM MIN	LT1006AM TYP	LT1006AM MAX	LT1006M MIN	LT1006M TYP	LT1006M MAX	UNITS
V_{OS}	Input Offset Voltage		●		40	180		60	250	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift		●		0.2	1.3		0.3	1.8	µV/°C
I_{OS}	Input Offset Current		●		0.4	2.0		0.5	4.0	nA
I_B	Input Bias Current		●		13	25		16	40	nA
A_{VOL}	Large Signal Voltage Gain	V_O = 0.05V to 3.5V, R_L = 2k	●	0.25	0.8		0.15	0.7		V/µV
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.1V to 3.2V	●	90	103		87	102		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V, V_O = 0V	●	100	117		97	116		dB
	Maximum Output Voltage Swing	Output Low, 600Ω to GND	●		6	15		6	18	mV
		Output High, 600Ω to GND	●	3.2	3.8		3.1	3.8		V
I_S	Supply Current		●		380	630		400	680	µA

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0V, V_O = 1.4V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1006AC MIN	LT1006AC TYP	LT1006AC MAX	LT1006C MIN	LT1006C TYP	LT1006C MAX	UNITS
V_{OS}	Input Offset Voltage				30	110		45	160	µV
		LT1006N8	●					50	190	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift				0.2	1.3		0.3	1.8	µV/°C
		LT1006N8	●					0.5	2.5	µV/°C
I_{OS}	Input Offset Current		●		0.25	1.2		0.3	2.5	nA
I_B	Input Bias Current		●		11	20		12	30	nA
A_{VOL}	Large Signal Voltage Gain	V_O = 0.04V to 3.5V, R_L = 2k	●	0.35	1.3		0.25	1.2		V/µV
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.4V	●	96	109		92	108		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V, V_O = 0V	●	101	120		97	118		dB
	Maximum Output Voltage Swing	Output Low, 600Ω to GND	●		6	13		6	13	mV
		Output High, 600Ω to GND	●	3.3	3.9		3.2	3.9		V
I_S	Supply Current		●		350	570		360	620	µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is guaranteed by design and is not tested.

Note 2: Regular operation does not require an external resistor. In order to program the supply current for low power or high speed operation, connect an external resistor from Pin 8 to Pin 7 or from Pin 8 to Pin 4, respectively. Supply current specifications (for R_{SET} = 180k) do not include current in R_{SET}.

Note 3: This parameter is tested on a sample basis only. All noise parameters are tested with V_S = ±2.5V, V_O = 0V.

Note 4: Optional offset nulling is accomplished with a potentiometer connected between the trim terminals and the wiper to V^-. A 10k pot (providing a null range of ±6mV) is recommended for minimum drift of nulled offset voltage with temperature. For increased trim resolution and accuracy, two fixed resistors can be used in conjunction with a smaller potentiometer. For example: two 4.7k resistors tied to pins 1 and 5, with a 500Ω pot in the middle, will have a null range of ±150µV.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM/AC MIN	LT1006AM/AC TYP	LT1006AM/AC MAX	LT1006M/C MIN	LT1006M/C TYP	LT1006M/C MAX	UNITS
V_{OS}	Input Offset Voltage			30	100		50	180	μV
I_{OS}	Input Offset Current			0.1	0.5		0.15	0.9	nA
I_B	Input Bias Current			7.5	12.0		8.0	20.0	nA
	Input Voltage Range		13.5 −15.0	13.8 −15.3		13.5 −15.0	13.8 −15.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V, -15V$	100	117		97	116		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	106	126		103	124		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$ $V_O = \pm 10V, R_L = 600\Omega$	1.5 0.8	5.0 1.5		1.2 0.5	4.0 1.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L = 2k$	±13	±14		±12.5	±14		V
SR	Slew Rate	$R_{SET} = \infty$ $R_{SET} = 390\Omega$ Pin 8 to Pin 4	0.25 1.0	0.4 1.2		0.25 1.0	0.4 1.2		V/μs V/μs
I_S	Supply Current			360	540		360	600	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

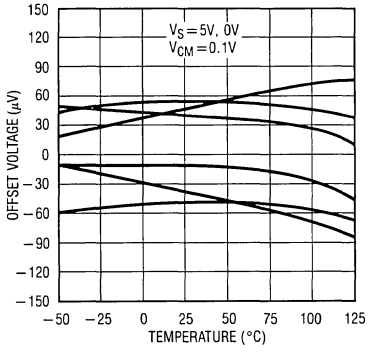
SYMBOL	PARAMETER	CONDITIONS		LT1006AM MIN	LT1006AM TYP	LT1006AM MAX	LT1006M MIN	LT1006M TYP	LT1006M MAX	UNITS
V_{OS}	Input Offset Voltage		●		80	320		110	460	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift		●		0.5	2.2		0.6	2.8	μV/°C
I_{OS}	Input Offset Current		●		0.2	2.0		0.3	3.0	nA
I_B	Input Bias Current		●		9	18		11	27	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	0.5	1.5		0.25	1.0		V/μV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13V, -14.9V$	●	97	114		94	113		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	●	100	117		97	116		dB
	Maximum Output Voltage Swing	$R_L = 2k$	●	±12	±13.8		±11.5	±13.8		V
I_S	Supply Current		●		400	650		400	750	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

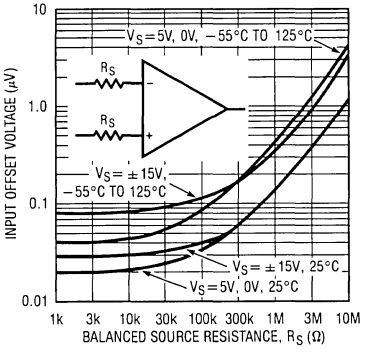
SYMBOL	PARAMETER	CONDITIONS		LT1006AC MIN	LT1006AC TYP	LT1006AC MAX	LT1006C MIN	LT1006C TYP	LT1006C MAX	UNITS
V_{OS}	Input Offset Voltage	 LT1006N8	●		50	200		75 80	300 330	μV μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift	 LT1006N8	●		0.5	2.2		0.6 0.7	2.8 3.5	μV/°C μV/°C
I_{OS}	Input Offset Current		●		0.15	1.0		0.25	2.0	nA
I_B	Input Bias Current		●		8.0	15		10	23	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	1.0	3.0		0.7	2.5		V/μV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$	●	98	116		94	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	●	101	120		97	118		dB
	Maximum Output Voltage Swing	$R_L = 2k$	●	±12.5	±13.9		±11.5	±13.8		V
I_S	Supply Current		●		370	600		380	660	μA

TYPICAL PERFORMANCE CHARACTERISTICS

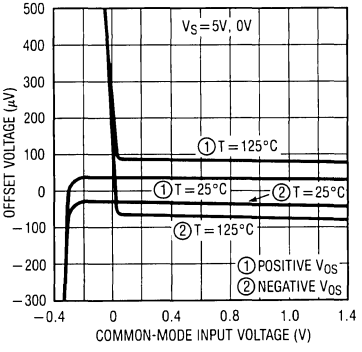
Offset Voltage Drift with Temperature of Representative Units



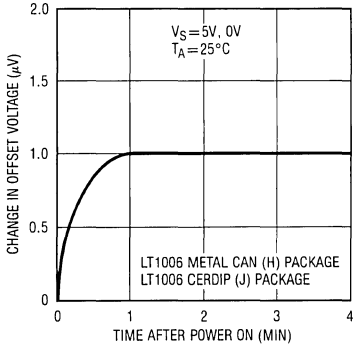
Offset Voltage vs Balanced Source Resistor



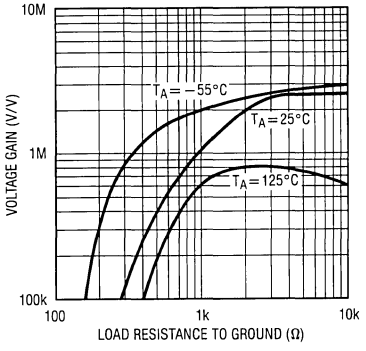
V_{OS} vs Common-Mode Voltage vs Temperature



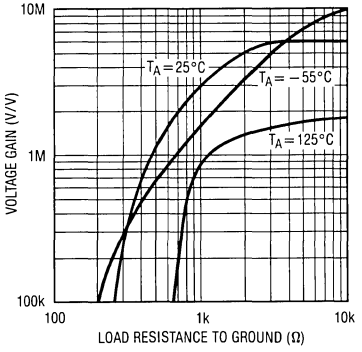
Warm-Up Drift



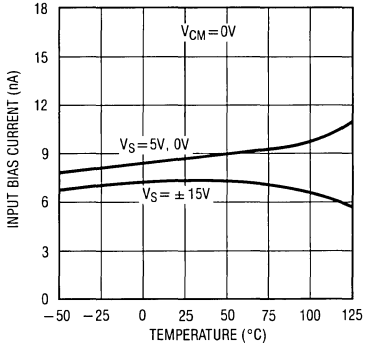
Voltage Gain vs Load Resistance, V_S = 5V, 0V



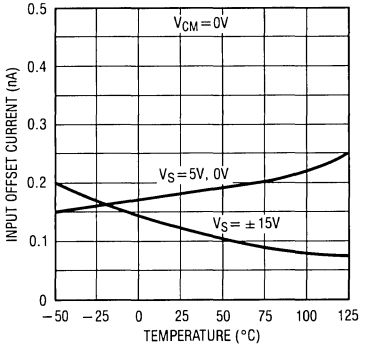
Voltage Gain vs Load Resistance with V_S = ±15V



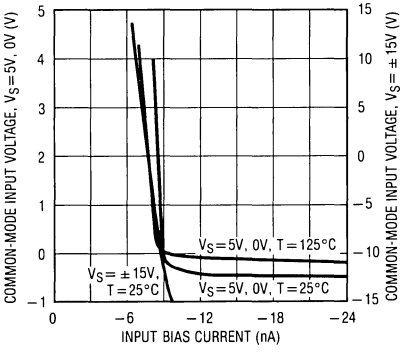
Input Bias Current vs Temperature



Input Offset Current vs Temperature

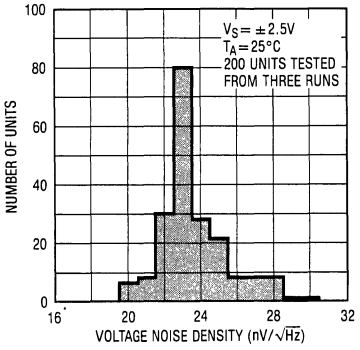


Input Bias Current vs Common-Mode Voltage

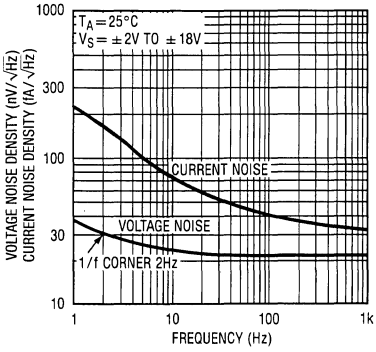


TYPICAL PERFORMANCE CHARACTERISTICS

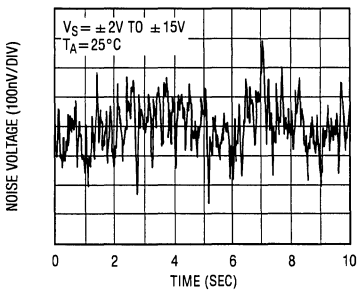
10Hz Voltage Noise Distribution



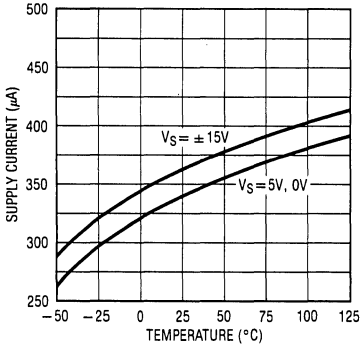
Noise Spectrum



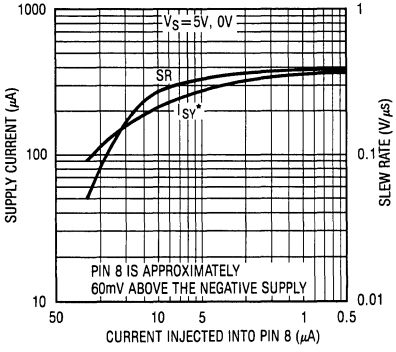
0.1Hz to 10Hz Noise



Supply Current vs Temperature

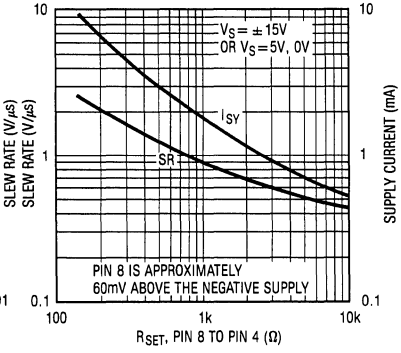


Reducing Power Dissipation

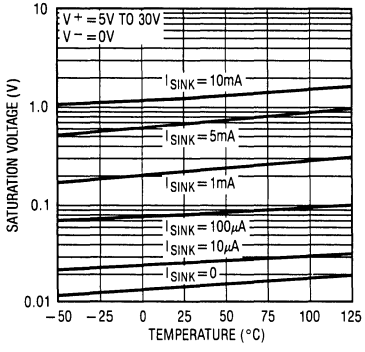


*I_{SY} DOES NOT INCLUDE CURRENT THROUGH R_{SET}

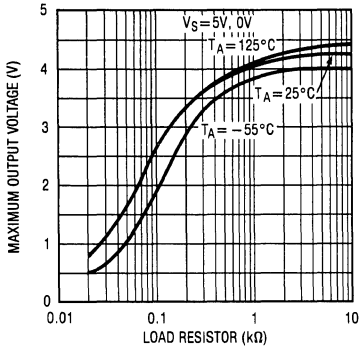
Increasing Slew Rate (R_{SET} to V^-)



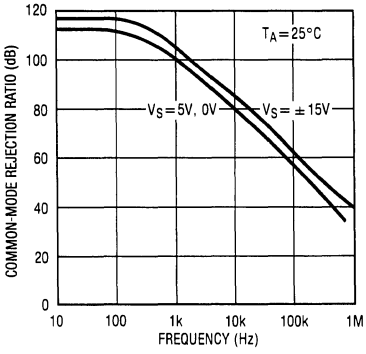
Output Saturation vs Sink Current vs Temperature



Maximum Output Swing vs Load Resistor

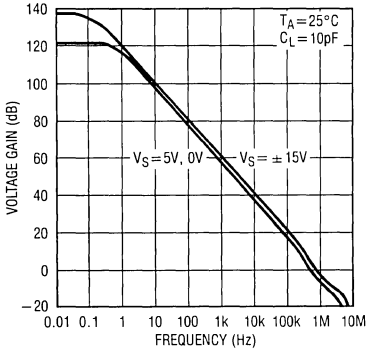


Common-Mode Rejection Ratio vs Frequency

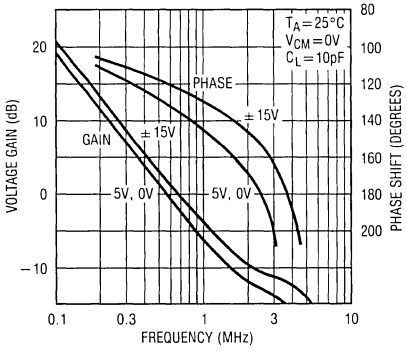


TYPICAL PERFORMANCE CHARACTERISTICS

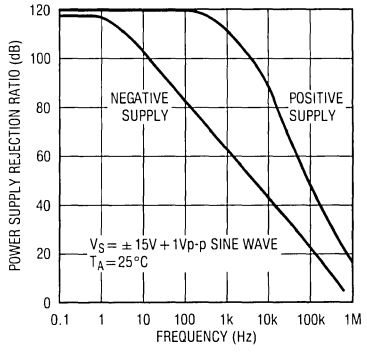
Voltage Gain vs Frequency



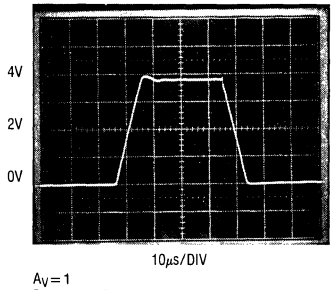
Gain, Phase vs Frequency



Power Supply Rejection Ratio vs Frequency

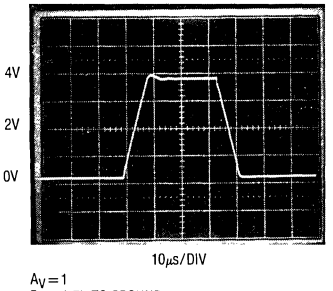


Large Transient Response, $V_S = 5V, 0V$



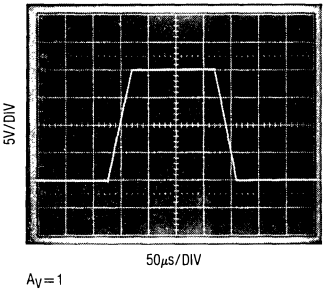
$A_V = 1$
$R_L = 4.7k$ TO 5V
INPUT = 0V TO 3.8V

Large Signal Transient Response, $V_S = 5V, 0V$



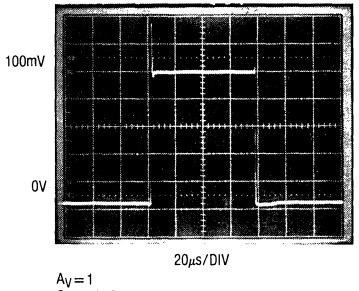
$A_V = 1$
$R_L = 4.7k$ TO GROUND
INPUT = 0V TO 3.8V

Large Signal Transient Response, $V_S = \pm 15V$



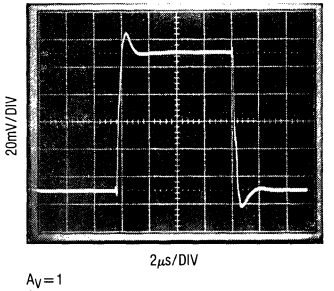
$A_V = 1$

Small Signal Transient Response, $V_S = 5V, 0V$



$A_V = 1$
$C_L = 10pF$
$R_L = 600\Omega$ TO GND
INPUT = 0V TO 100mV PULSE

Small Signal Transient Response, $V_{CC} = \pm 2.5V$ to $\pm 15V$



$A_V = 1$
$C_L = 10pF$

APPLICATIONS INFORMATION

The LT1006 is fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1006 has specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1006, the 400Ω resistors, in series with the input (see schematic diagram), protect the devices even when the input is 5V below ground.

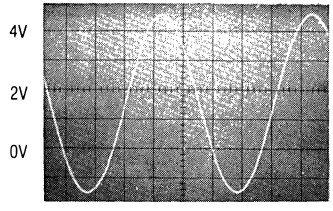
b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1006's output does not reverse, as illustrated below, even when the inputs are at – 1.5V.

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1006's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

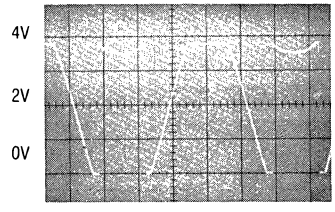
In dual supply operations, the output stage is crossover distortion-free.

Since the output cannot go exactly to ground, but can only approach ground to within a few millivolts, care should be exercised to ensure that the output is not saturated. For example, a 1mV input signal will cause the amplifier to set up in its linear region in the gain 100 configuration shown below, but is not enough to make the amplifier function properly in the voltage follower mode.

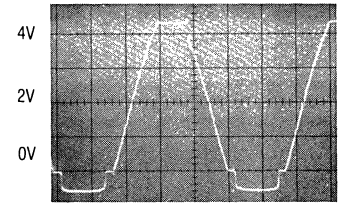
Voltage Follower with Input Exceeding the Negative Common-Mode Range (V_S = 5V, 0V)



6Vp-p INPUT, –1.5V TO 4.5V

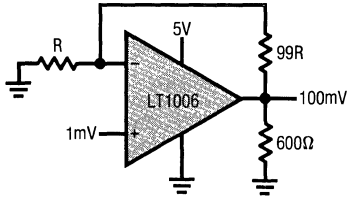


LM324, LM358, OP-20, OP-21 EXHIBIT OUTPUT PHASE REVERSAL

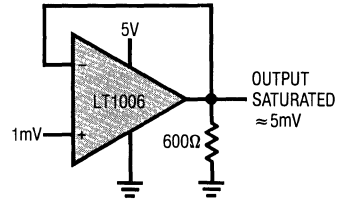


LT1006 NO PHASE REVERSAL

Gain 100 Amplifier



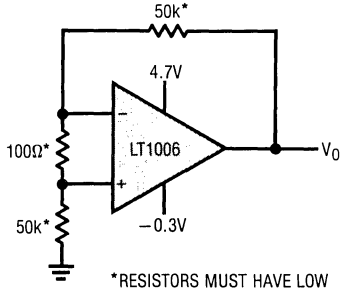
Voltage Follower



APPLICATIONS INFORMATION

In automated production testing the output is forced to 1.4V by the test loop; offset voltage is measured with a common-mode voltage of zero and the negative supply at zero (Pin 4). Without the test loop, these exact conditions cannot be achieved. The test circuit shown ensures that the output will never saturate even with worst-case offset voltages (−250μV over the −55°C to 125°C range). The effective common-mode input is 0.3V with respect to the negative supply. As indicated by the common-mode rejection specifications the difference is only a few microvolts between the two methods of offset voltage measurement.

Test Circuit for Offset Voltage and Offset Drift with Temperature



*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.
**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO ±20V.
$V_O = 1000V_{OS}$

Low Supply Operation

The minimum guaranteed supply voltage for proper operation of the LT1006 is 2.7V. Typical supply current at this voltage is 320μA, therefore power dissipation is only 860μW.

Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1028 data sheet.

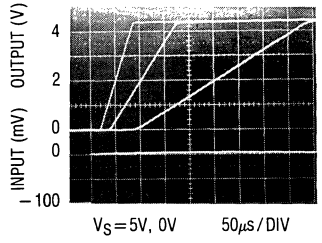
Supply Current Programming

Connecting an optional external resistor to Pin 8 changes the biasing of the LT1006 in order to increase its speed or to decrease its power consumption. If higher slew rate is required, connect the external resistor from Pin 8 to Pin 4 [see performance curves for Increasing Slew Rate (R_{SET} to V^-)]. For lower power consumption, inject a current into Pin 8 (which is approximately 60mV above V^-) as shown on the Reducing Power Dissipation plot. This can be accomplished by connecting R_{SET} to the positive supply, or to save additional power, by obtaining the injected current from a low voltage battery.

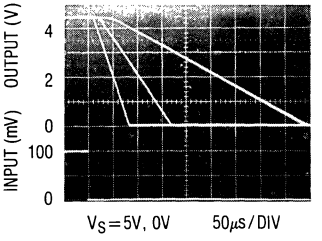
Comparator Applications

The single supply operation of the LT1006 and its ability to swing close to ground while sinking current lends itself to use as a precision comparator with TTL compatible output.

Comparator Rise Response Time to 10mV, 5mV, 2mV Overdrives

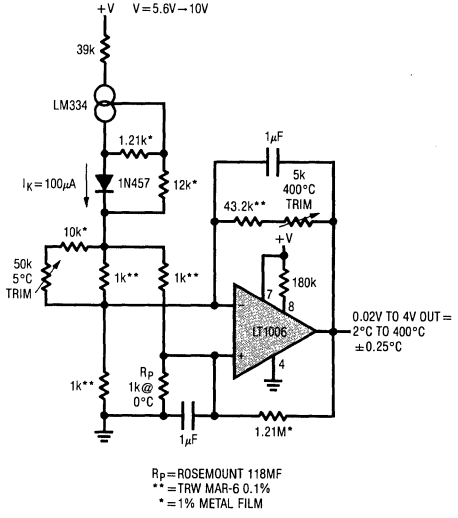


Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives

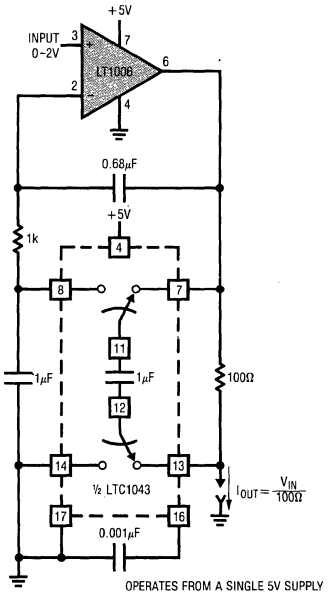


TYPICAL APPLICATIONS

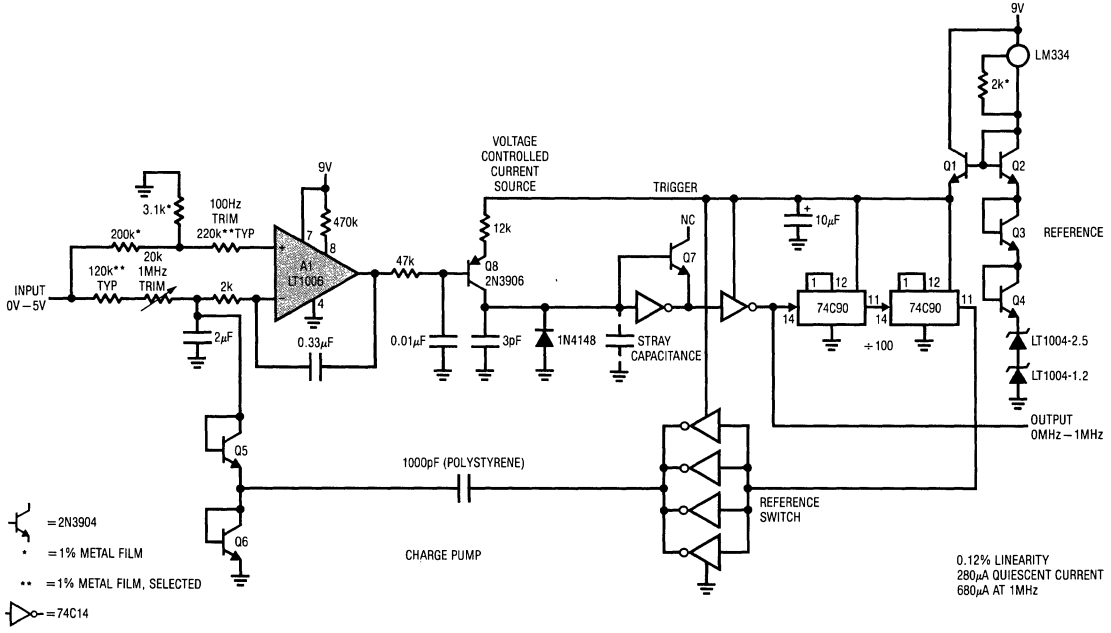
Platinum RTD Signal Conditioner with Curvature Correction



Voltage Controlled Current Source with Ground Referred Input and Output

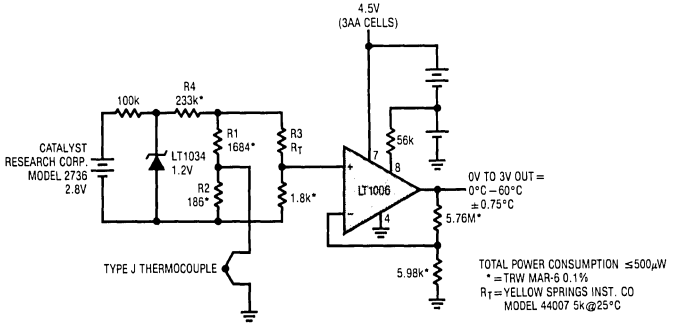


Micropower 1MHz V→F Converter

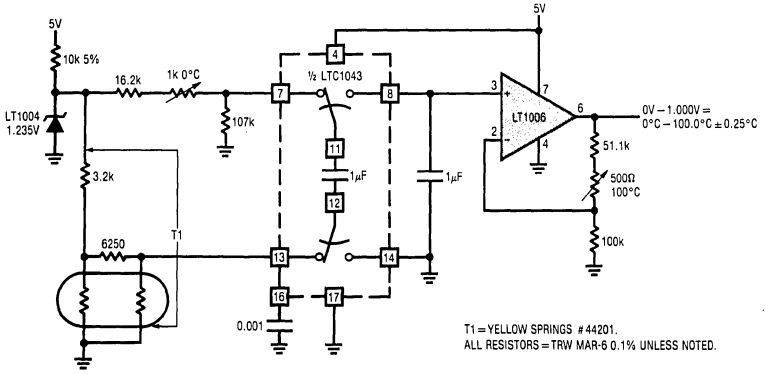


TYPICAL APPLICATIONS

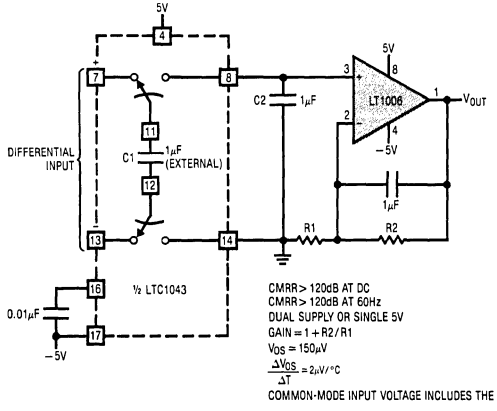
Micropower Thermocouple Signal Conditioner with Cold Junction Compensation



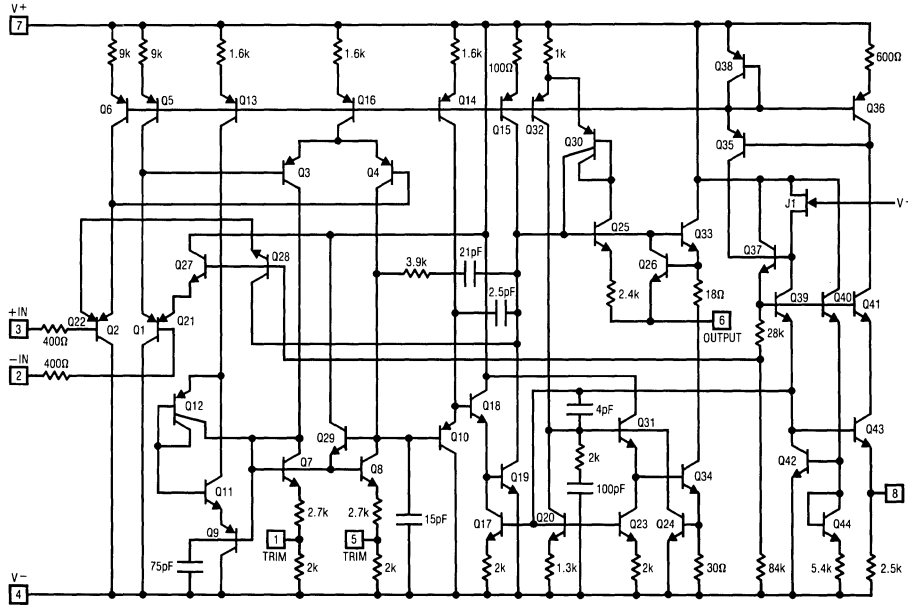
Linear Thermometer



± 5V Precision Instrumentation Amplifier



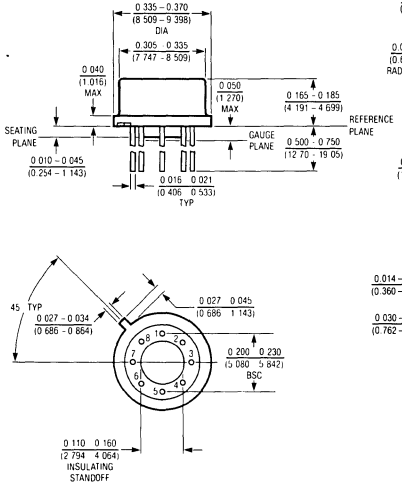
LT1006 SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

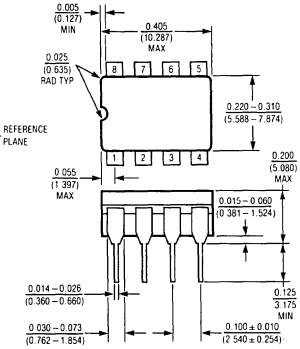
Dimensions in inches (millimeters) unless otherwise noted.

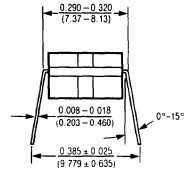
H8 Package
TO-5 Metal Can



T_{jmax} 150°C | θ_{ja} 150°C/W | θ_{jc} 45°C/W

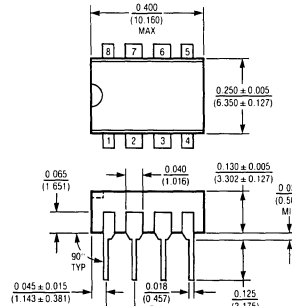
J8 Package
Hermetic DIP

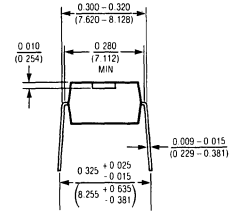




T_{jmax} 150°C | θ_{ja} 100°C/W

N8 Package
Plastic DIP





T_{jmax} 100°C | θ_{ja} 130°C/W

Ultra-Low Noise Precision High Speed Op Amp

FEATURES

- Voltage Noise — 1.1nV/√Hz Max. at 1kHz; 0.85nV/√Hz Typ. at 1kHz; 1.0nV/√Hz Typ. at 10Hz; 35nVp-p Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product — 50MHz Min.
- Slew Rate — 11V/μs Min.
- Offset Voltage — 40μV Max.
- Voltage Gain — 7 Million Min.
- Drift with Temperature — 0.8μV/°C Max.

APPLICATIONS

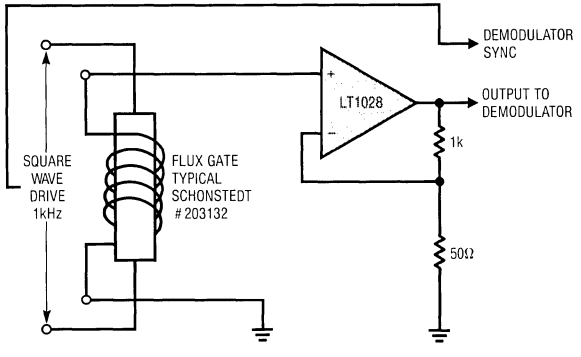
- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

DESCRIPTION

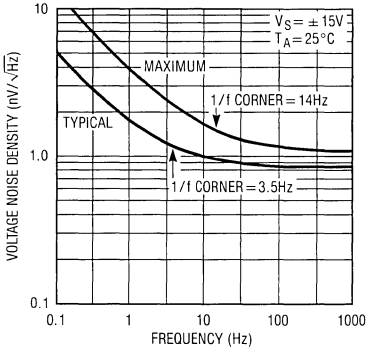
The LT1028 achieves a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz), distortion free output, and true precision parameters (0.1μV/°C drift, 10μV offset voltage, 30 million voltage gain). Although the LT1028 input stage operates at nearly 1mA of collector currents to achieve low voltage noise, input bias current is only 25nA.

The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

Flux Gate Amplifier



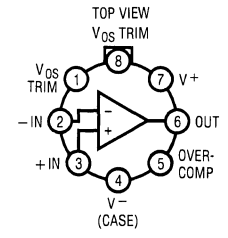
Voltage Noise vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
– 55°C to 105°C ..... ± 22V
105°C to 125°C ..... ± 16V
Differential Input Current (Note 8)..... ± 25mA
Input Voltage .....Equal to Supply Voltage
Output Short Circuit Duration .....Indefinite
Operating Temperature Range
LT1028AM, M..... – 55°C to 125°C
LT1028AC, C .....0°C to 70°C
Storage Temperature Range
All Devices..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....300°C

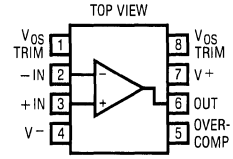
PACKAGE/ORDER INFORMATION



H8 PACKAGE TO-5 METAL CAN

ORDER PART NUMBER

LT1028AMH
LT1028MH
LT1028ACH
LT1028CH



J8 PACKAGE HERMETIC DIP
N8 PACKAGE PLASTIC DIP

LT1028AMJ8
LT1028MJ8
LT1028ACJ8
LT1028CJ8
LT1028ACN8
LT1028CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AM/AC MIN	LT1028AM/AC TYP	LT1028AM/AC MAX	LT1028M/C MIN	LT1028M/C TYP	LT1028M/C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	40		20	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3			0.3		μV/Mo
I_{OS}	Input Offset Current	$V_{CM} = 0V$		12	50		18	100	nA
I_B	Input Bias Current	$V_{CM} = 0V$		± 25	± 90		± 30	± 180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	75		35	90	nVp-p
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 4) $f_o = 1000Hz$, 100% tested		1.0 0.85	1.7 1.1		1.0 0.9	1.9 1.2	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	$f_o = 10Hz$ (Notes 3 and 5) $f_o = 1000Hz$, 100% tested		4.7 1.0	10.0 1.6		4.7 1.0	12.0 1.8	pA/√Hz pA/√Hz
	Input Resistance Common-Mode Differential Mode			 300 20			 300 20		 MΩ kΩ
	Input Capacitance			5			5		pF
	Input Voltage Range		± 11.0	± 12.2		± 11.0	± 12.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	117	133		110	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 12V$ $R_L \geq 1k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	7.0 5.0 3.0	30.0 20.0 15.0		5.0 3.5 2.0	30.0 20.0 15.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	± 12.3 ± 11.0	± 13.0 ± 12.2		± 12.0 ± 10.5	± 13.0 ± 12.2		V V
SR	Slew Rate	$A_{VCL} = -1$	11	15		11	15		V/μs
GBW	Gain-Bandwidth Product	$f_o = 20kHz$ (Note 6)	50	75		50	75		MHz
Z_o	Open Loop Output Impedance	$V_o = 0$, $I_o = 0$		80			80		Ω
I_S	Supply Current			7.4	9.5		7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AM MIN	LT1028AM TYP	LT1028AM MAX	LT1028M MIN	LT1028M TYP	LT1028M MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	120		45	180	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.8		0.25	1.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		25	90		30	180	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±40	±150		±50	±300	nA
	Input Voltage Range		●	±10.3	±11.7		±10.3	±11.7		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 16V$	●	110	130		104	130		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$ $R_L \ge 1k\Omega$, $V_O = \pm 10V$	●	3.0 2.0	14.0 10.0		2.0 1.5	14.0 10.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±10.3	±11.6		±10.3	±11.6		V
I_S	Supply Current		●		8.7	11.5		9.0	13.0	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AC MIN	LT1028AC TYP	LT1028AC MAX	LT1028C MIN	LT1028C TYP	LT1028C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		15	80		30	125	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.1	0.8		0.2	1.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		15	65		22	130	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±30	±120		±40	±240	nA
	Input Voltage Range		●	±10.5	±12.0		±10.5	±12.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	110	124		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	114	132		107	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$ $R_L \ge 1k\Omega$, $V_O = \pm 10V$	●	5.0 4.0	25.0 18.0		3.0 2.5	25.0 18.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$ $R_L \ge 600\Omega$ (Note 9)	●	±11.5 ±9.5	±12.7 ±11.0		±11.5 ±9.0	±12.7 ±10.5		V V
I_S	Supply Current		●		8.0	10.5		8.2	11.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25°C$, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

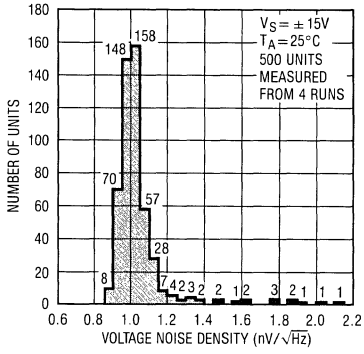
Note 7: This parameter is not 100% tested.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

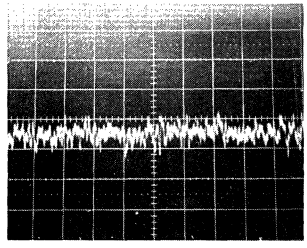
Note 9: This parameter guaranteed by design, fully warmed up at $T_A = 70°C$. It includes chip temperature increase due to supply and load currents.

TYPICAL PERFORMANCE CHARACTERISTICS

10Hz Voltage Noise Distribution

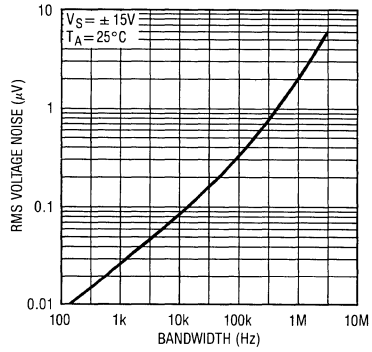


Wideband Noise, DC to 20kHz

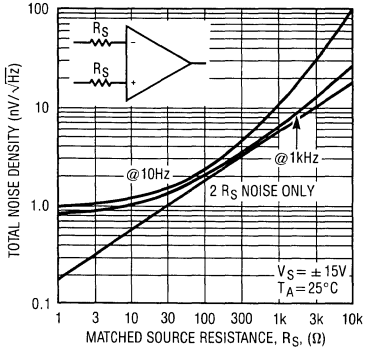


VERTICAL SCALE = 0.5μV/DIV
HORIZONTAL SCALE = 0.5ms/DIV

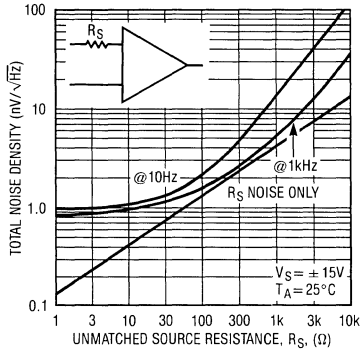
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



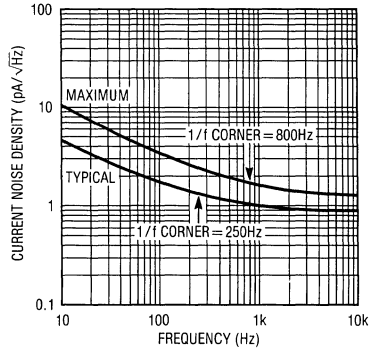
Total Noise vs Matched Source Resistance



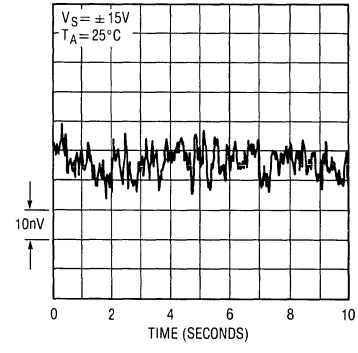
Total Noise vs Unmatched Source Resistance



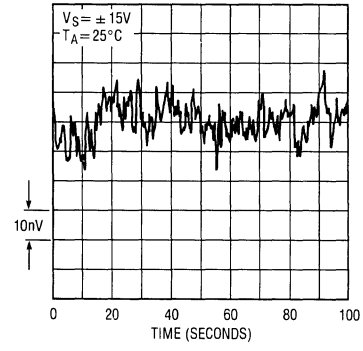
Current Noise Spectrum



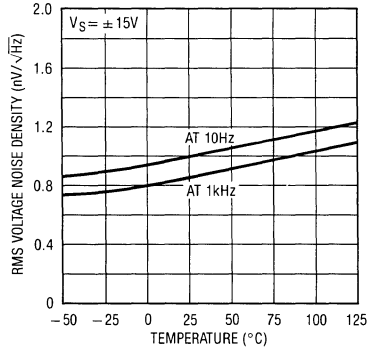
0.1Hz to 10Hz Voltage Noise



0.01Hz to 1Hz Voltage Noise

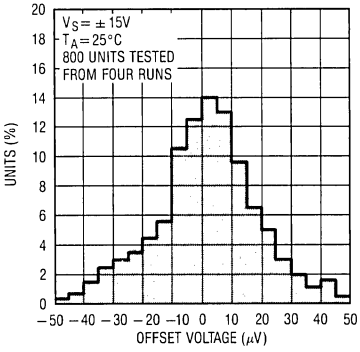


Voltage Noise vs Temperature

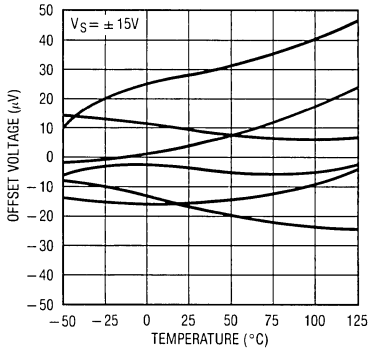


TYPICAL PERFORMANCE CHARACTERISTICS

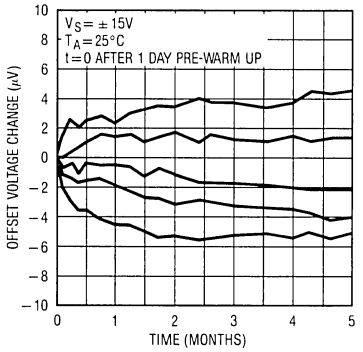
Distribution of Input Offset Voltage



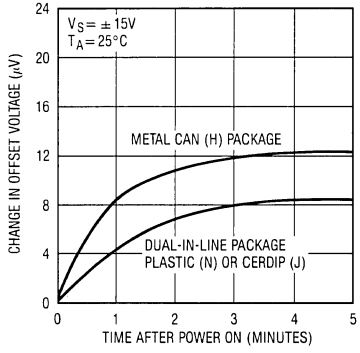
Offset Voltage Drift with Temperature of Representative Units



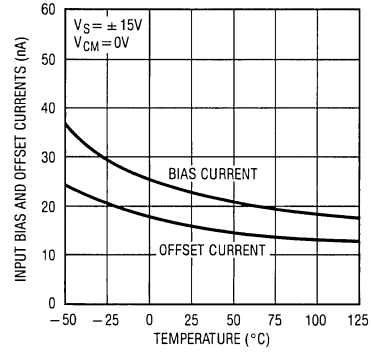
Long Term Stability of Five Representative Units



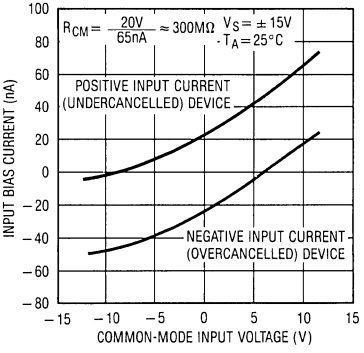
Warm-Up Drift



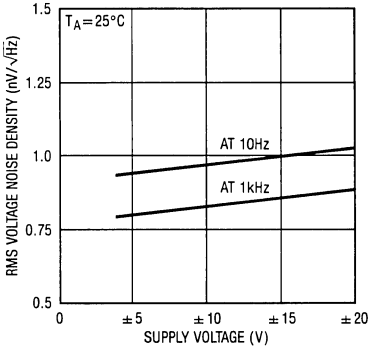
Input Bias and Offset Currents Over Temperature



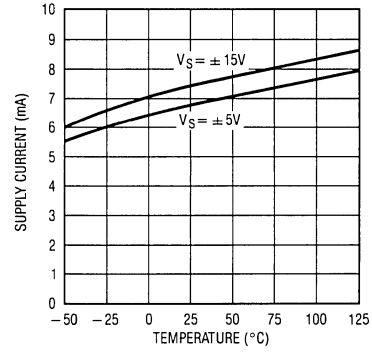
Bias Current Over the Common-Mode Range



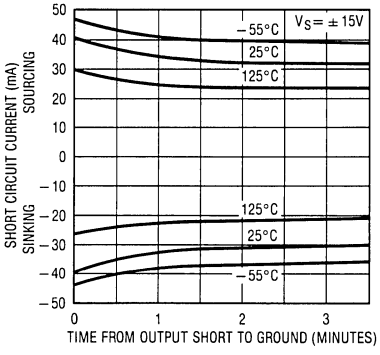
Voltage Noise vs Supply Voltage



Supply Current vs Temperature

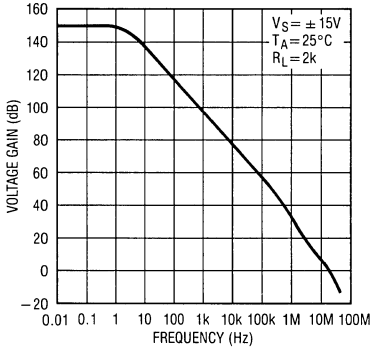


Output Short Circuit Current vs Time

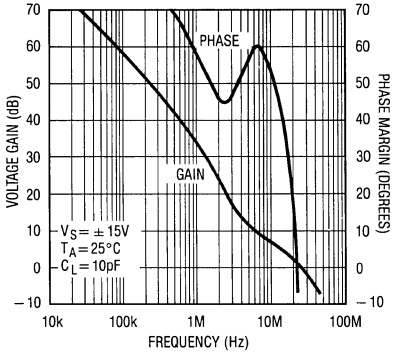


TYPICAL PERFORMANCE CHARACTERISTICS

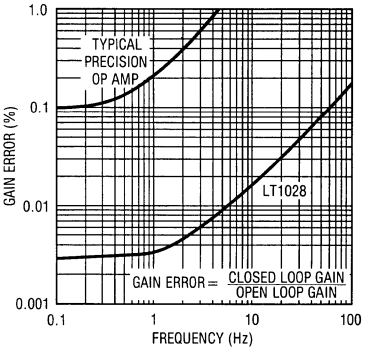
Voltage Gain vs Frequency



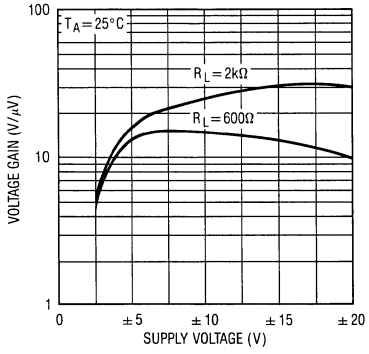
Gain, Phase vs Frequency



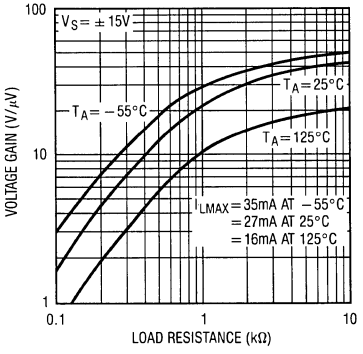
Gain Error vs Frequency Closed Loop Gain = 1000



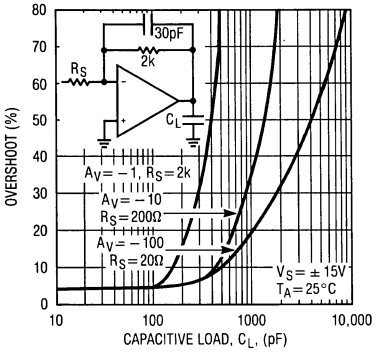
Voltage Gain vs Supply Voltage



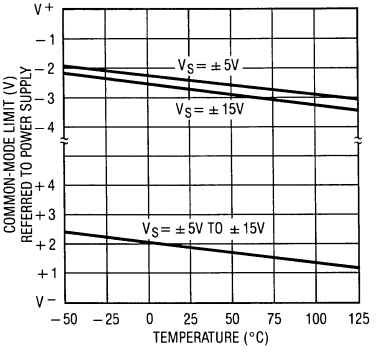
Voltage Gain vs Load Resistance



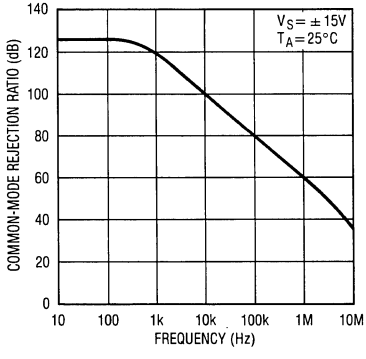
Capacitance Load Handling



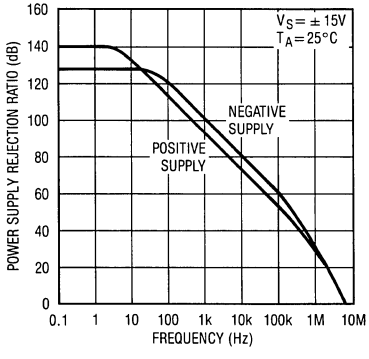
Common-Mode Limit Over Temperature



Common-Mode Rejection Ratio vs Frequency

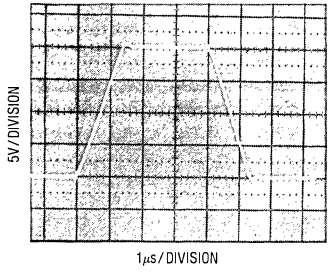


Power Supply Rejection Ratio vs Frequency



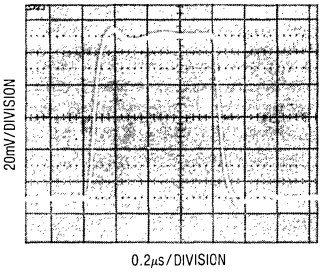
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Transient Response



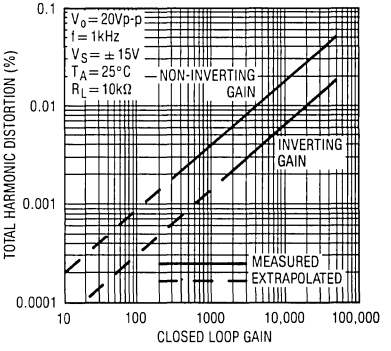
$A_V = -1$, $R_S = R_f = 2k$, $C_f = 30pF$

Small Signal Transient Response

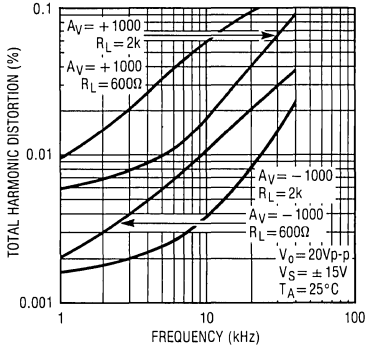


$A_V = -1$, $R_S = R_f = 2k\Omega$
$C_f = 30pF$, $C_L = 80pF$

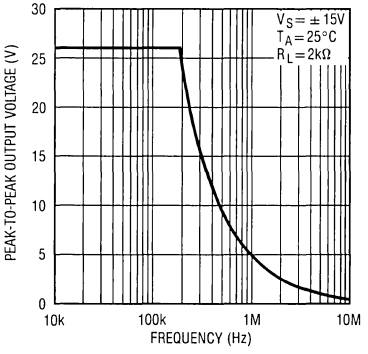
Total Harmonic Distortion vs Closed Loop Gain



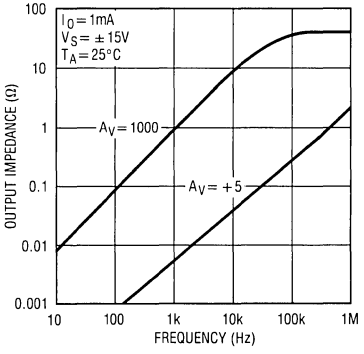
Total Harmonic Distortion vs Frequency and Load Resistance



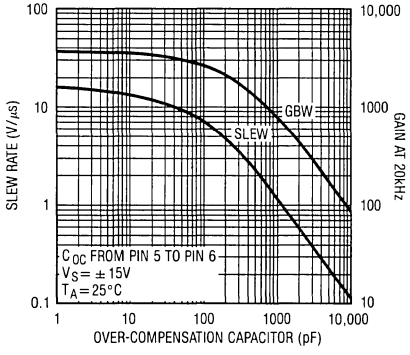
Maximum Undistorted Output vs Frequency



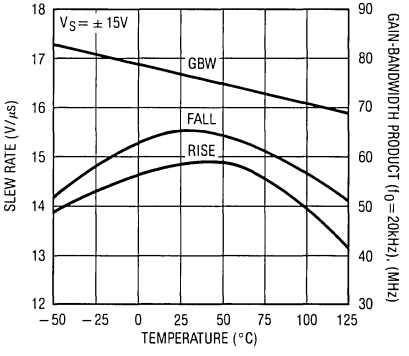
Closed Loop Output Impedance



Slew Rate, Gain-Bandwidth-Product vs Over-Compensation Capacitor



Slew Rate, Gain-Bandwidth Product Over Temperature



APPLICATIONS INFORMATION —NOISE

Voltage Noise vs Current Noise

The LT1028's less than $1nV/\sqrt{Hz}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise (e_n), current noise (i_n) and resistor noise (r_n).

Total Noise vs Source Resistance

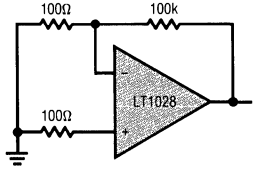
The total input referred noise of an op amp is given by

$$e_t = [e_n^2 + r_n^2 + (i_n R_{eq})^2]^{1/2}$$

where R_{eq} is the total equivalent source resistance at the two inputs

and $r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{R_{eq}}$ in $nV/\sqrt{Hz}$ at 25°C

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown below.



$R_{eq} = 100\Omega + 100\Omega \| 100k \approx 200\Omega$

$r_n = 0.13\sqrt{200} = 1.84nV/\sqrt{Hz}$

$e_n = 0.85nV/\sqrt{Hz}$

$i_n = 1.0pA/\sqrt{Hz}$

$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04nV/\sqrt{Hz}$

output noise = $1000\, e_t = 2.04\mu V/\sqrt{Hz}$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As R_{eq} is increased resistor noise becomes the largest term—as in the example above—and the LT1028's voltage noise becomes negligible. As R_{eq} is further increased, current noise becomes important. At 1kHz, when R_{eq} is in excess of 20kΩ, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k\Omega$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1kΩ because the resistor noise contribution is less. When $R_S > 1k\Omega$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1028 is the optimum amplifier for noise performance—provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise—as the source resistance is increased beyond the LT1028's level of usefulness.

Best Op Amp for Lowest Total Noise vs Source Resistance

SOURCE RESISTANCE (Note 1)	BEST OP AMP AT LOW FREQ (10Hz)	BEST OP AMP WIDEBAND (1kHz)
0 to 400Ω	LT1028	LT1028
400Ω to 4kΩ	LT1007/1037	LT1028
4kΩ to 40kΩ	LT1001	LT1007/1037
40kΩ to 500kΩ	LT1012	LT1001
500kΩ to 5MΩ	LT1012 or LT1055	LT1012
>5M	LT1055	LT1055

Note 1: Source resistance is defined as matched or unmatched, e.g., R_S = 1kΩ means: 1kΩ at each input, or 1kΩ at one input and zero at the other.

APPLICATIONS INFORMATION —NOISE

Noise Testing—Voltage Noise

The LT1028's RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed loop gain of 31 with a 60Ω source resistor and a 1.8kΩ feedback resistor. The noise of this resistor combination is $0.13\sqrt{58} = 1.0nV/\sqrt{Hz}$. An LT1028 with $0.85nV/\sqrt{Hz}$ noise will read $(0.85^2 + 1.0^2)^{1/2} = 1.31nV/\sqrt{Hz}$. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8-10% too high.

The 0.1Hz to 10Hz peak-to-peak noise of the LT1028 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028 requires special test precautions:

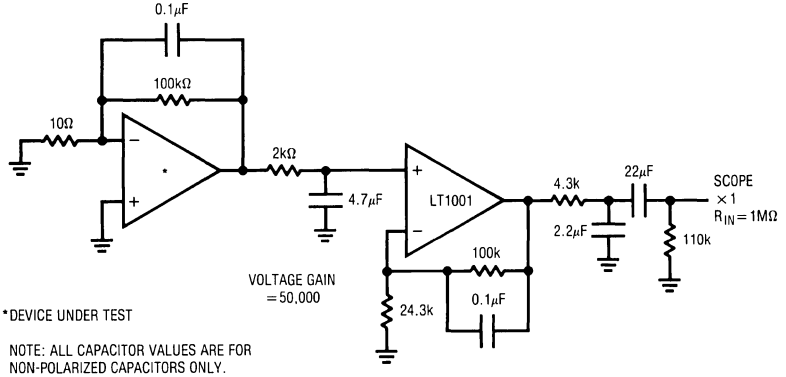
(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 10μV due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

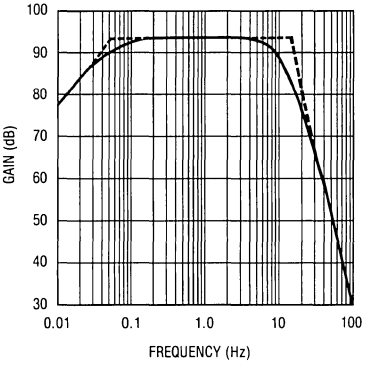
(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz p-p Noise Tester Frequency Response

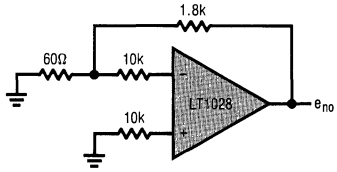


APPLICATIONS INFORMATION —NOISE

Noise Testing—Current Noise

Current noise density (i_n) is defined by the following formula, and can be measured in the circuit shown:

$$i_n = \frac{[e_{no}^2 - (31 \times 18.4nV/\sqrt{Hz})^2]^{1/2}}{20k \times 31}$$



If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

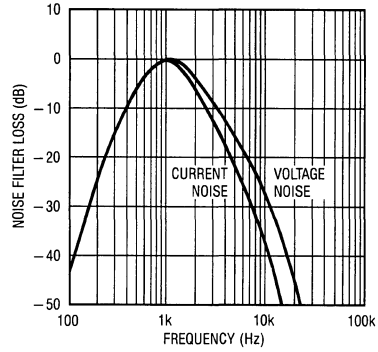
100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the guaranteed limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.

Automated Tester Noise Filter



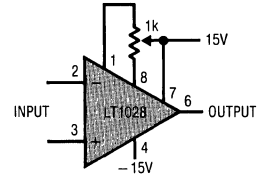
APPLICATIONS INFORMATION

General

The LT1028 series devices may be inserted directly into OP-07, OP-27, OP-37, LT1007 and LT1037 sockets with or without removal of external nulling components. In addition, the LT1028 may be fitted to 5534 sockets with the removal of external compensation components.

Offset Voltage Adjustment

The input offset voltage of the LT1028 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 1k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C.



The adjustment range with a 1k pot is approximately ±1.1mV.

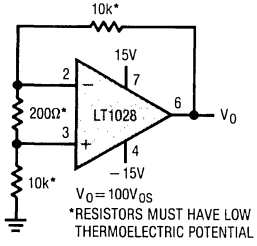
Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

APPLICATIONS INFORMATION

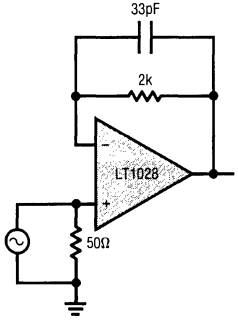
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1028.

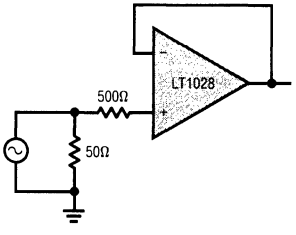
Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



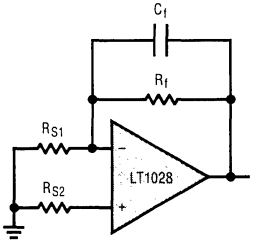
Frequency Response

The LT1028's Gain, Phase vs Frequency plot indicates that the device is stable in closed loop gains greater than +2 or –1 because phase margin is about 50° at an open loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the non-inverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided $C_f < 68pF$), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the non-inverting input has a similar effect. The following voltage follower configurations are stable:



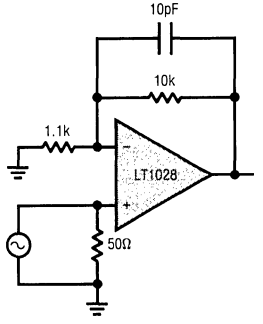


Another configuration which requires unity gain stability is shown below. When C_f is large enough to effectively short the output to the input at 15MHz, oscillations can occur. The insertion of $R_{S2} \geq 500\Omega$ will prevent the LT1028 from oscillating. When $R_{S1} \geq 500\Omega$, the additional noise contribution due to the presence of R_{S2} will be minimal. When $R_{S1} \leq 100\Omega$, R_{S2} is not necessary, because R_{S1} represents a heavy load on the output through the C_f short. When $100\Omega < R_{S1} < 500\Omega$, R_{S2} should match R_{S1}. For example, $R_{S1} = R_{S2} = 300\Omega$ will be stable. The noise increase due to R_{S2} is 40%.



If C_f is only used to cut noise bandwidth, a similar effect can be achieved using the over-compensation terminal.

The Gain, Phase plot also shows that phase margin is about 45° at a gain of 10 (20dB). The following configuration has a high (≈70%) overshoot without the 10pF capacitor because of additional phaseshift caused by the feedback resistor—input capacitance pole. The presence of the 10pF capacitor cancels this pole and reduces overshoot to 5%.

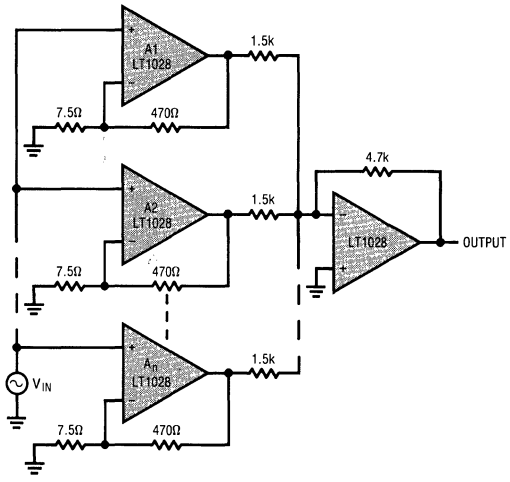


Over-Compensation

The LT1028 is equipped with a frequency over-compensation terminal (pin 5). A capacitor connected between pin 5 and the output will reduce noise bandwidth. Details are shown on the Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor plot. An additional benefit is increased capacitive load handling capability.

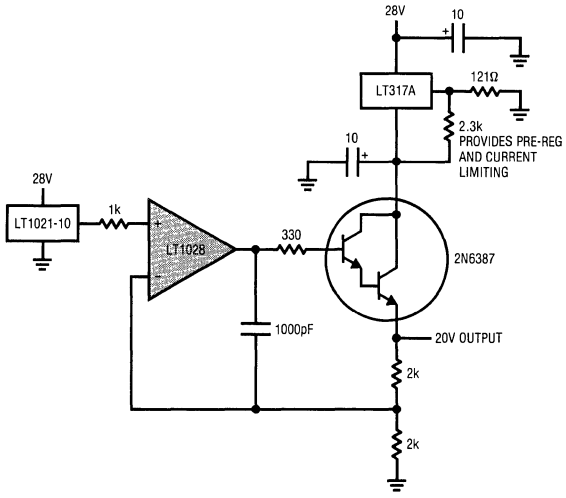
TYPICAL APPLICATIONS

Paralleling Amplifiers to Reduce Voltage Noise

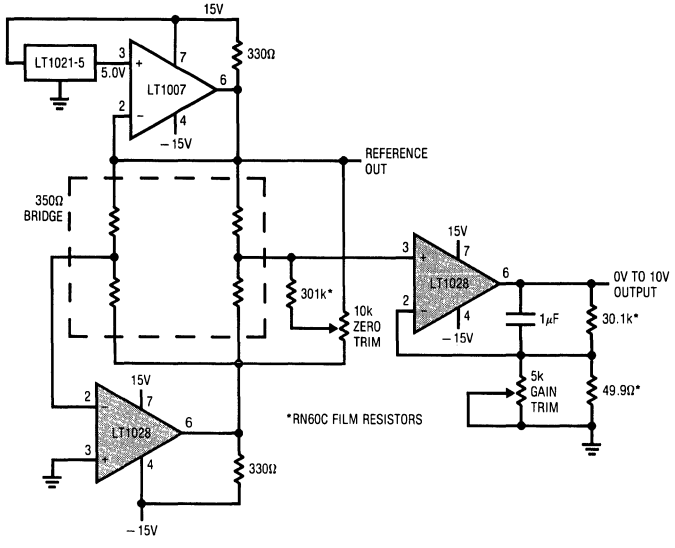


1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = 0.9nV/$\sqrt{Hz}$.
2. GAIN WITH n LT1028's IN PARALLEL = n × 200.
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 0.9nV/\sqrt{Hz}$.
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = \frac{0.9}{\sqrt{n}}$ nV/$\sqrt{Hz}$.
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES.
6. IF n = 5, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz, = $\frac{2\mu V}{\sqrt{5}} = 0.9\mu V$.

Low Noise Voltage Regulator



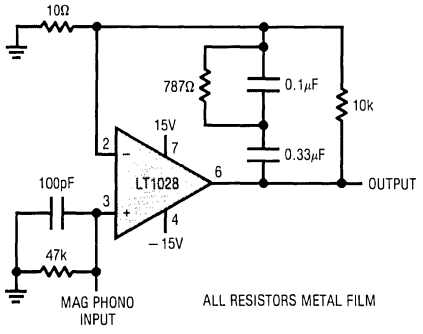
Strain Gauge Signal Conditioner with Bridge Excitation



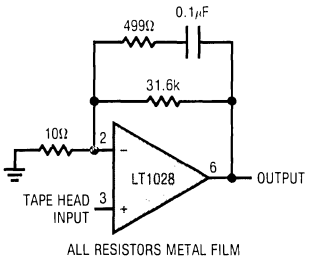
THE LT1028's NOISE CONTRIBUTION IS NEGLIGIBLE COMPARED TO THE BRIDGE NOISE.

TYPICAL APPLICATIONS

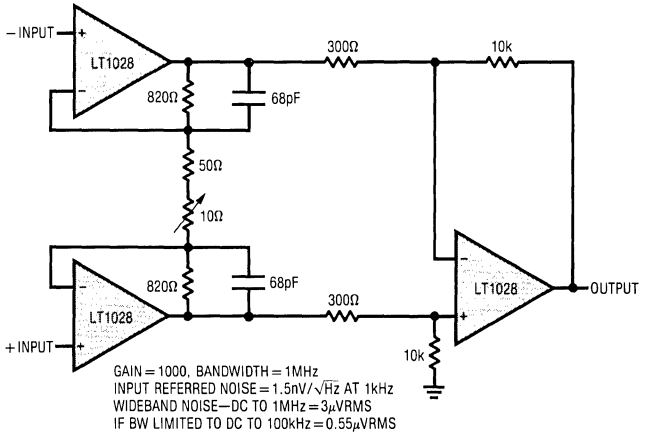
Phono Preamplifier



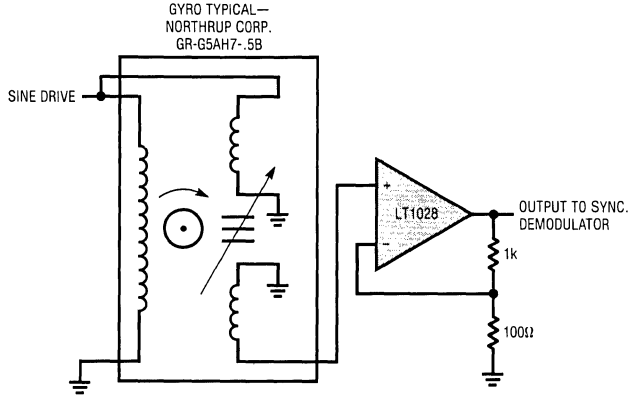
Tape Head Amplifier



Low Noise, Wide Bandwidth Instrumentation Amplifier

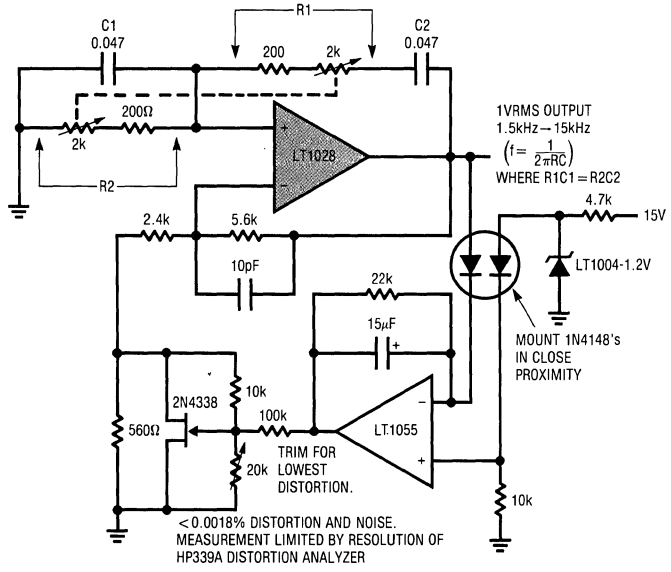


Gyro Pick-Off Amplifier

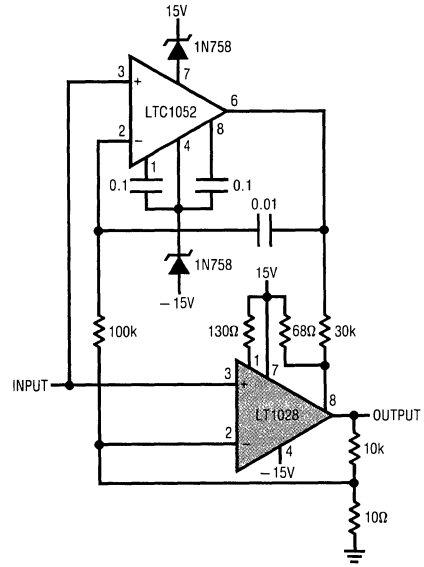


TYPICAL APPLICATIONS

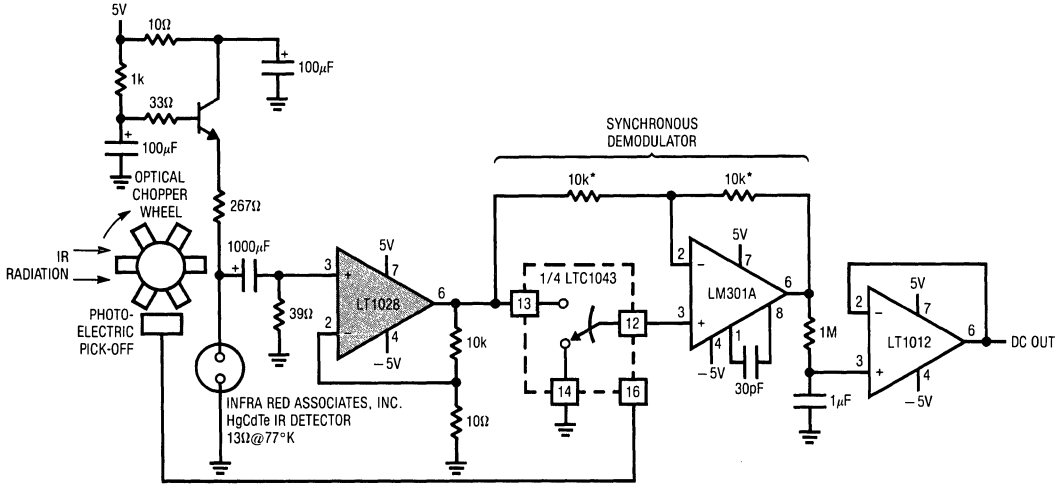
Super Low Distortion Variable Sine Wave Oscillator



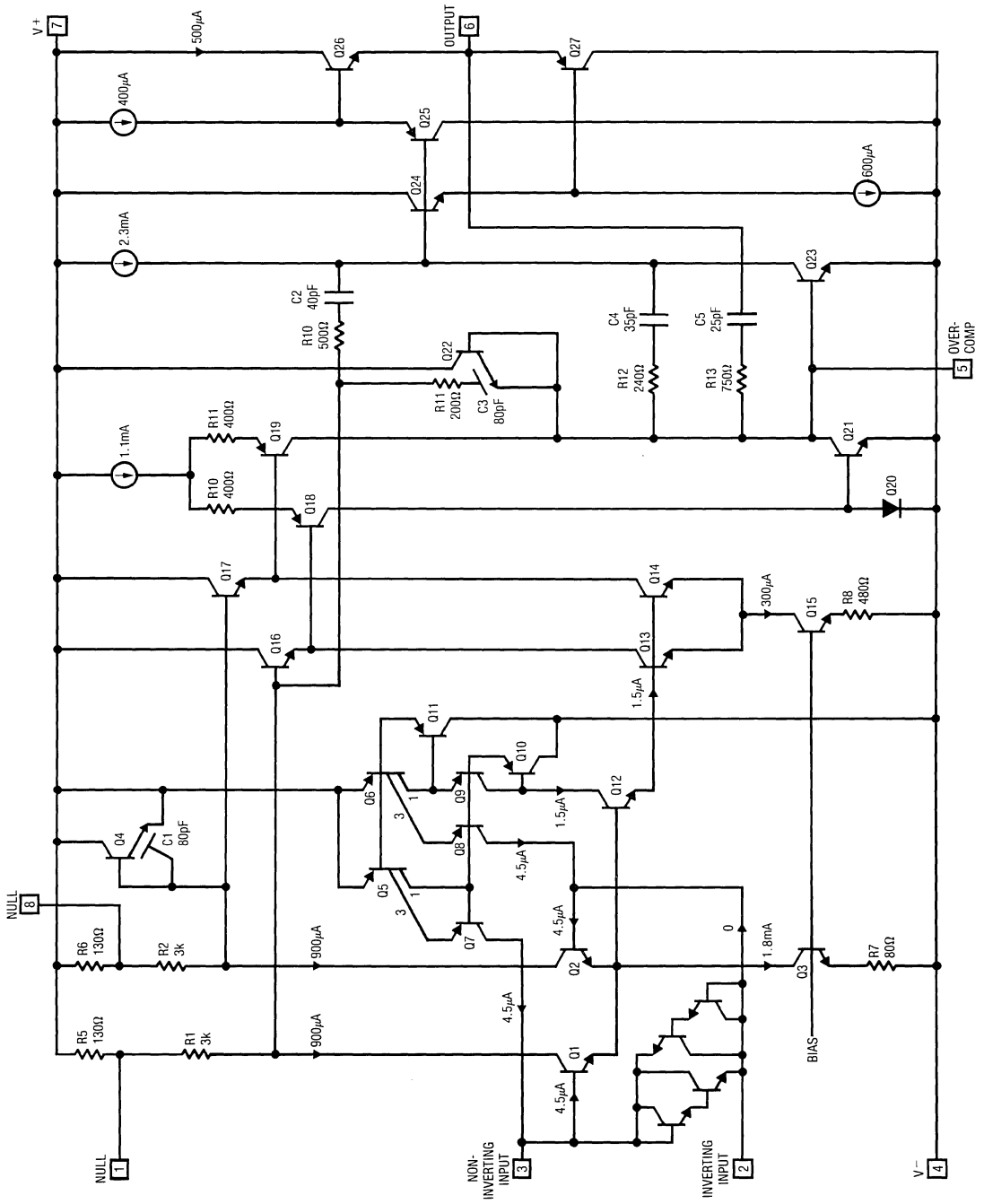
Chopper Stabilized Amplifier



Low Noise Infrared Detector

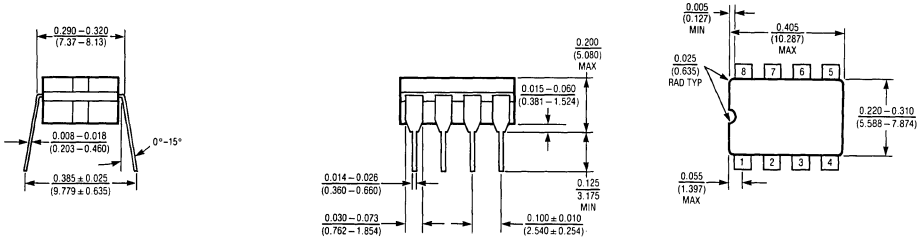


SCHEMATIC DIAGRAM



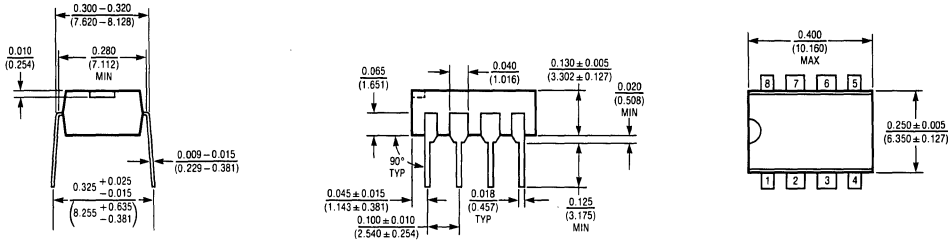
PACKAGE DESCRIPTIONS Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
Ceramic DIP



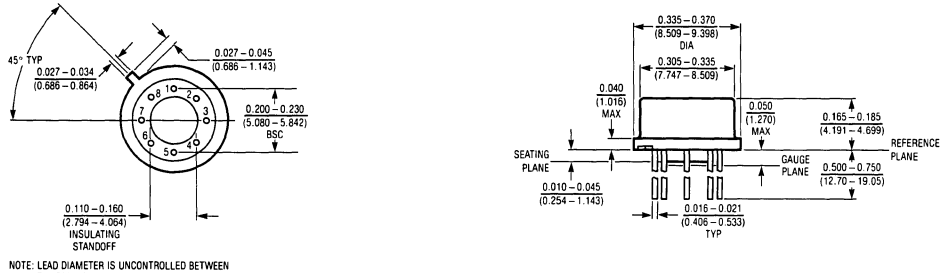
$T_j$max	θ_{ja}
165°C	100°C/W

N8 Package
Molded DIP



$T_j$max	θ_{ja}
115°C	130°C/W

H8 Package
TO-5 Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

$T_j$max	θ_{ja}	θ_{jc}
175°C	140°C/W	40°C/W

Dual and Quad, JFET Input Precision High Speed Op Amps

FEATURES

- 14V/μs Slew Rate — 10V/μs Min.
- 5MHz Gain-Bandwidth Product
- Fast Settling Time — 1.3μs to 0.02%
- 150μV Offset Voltage (LT1057) — 450μV Max.
- 180μV Offset Voltage (LT1058) — 600μV Max.
- 2μV/°C V_{OS} Drift — 7μV/°C Max.
- 50pA Bias Current at 70°C
- Low Voltage Noise — 13nV/√Hz @ 1kHz, 26nV/√Hz @ 10Hz

APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample and Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters

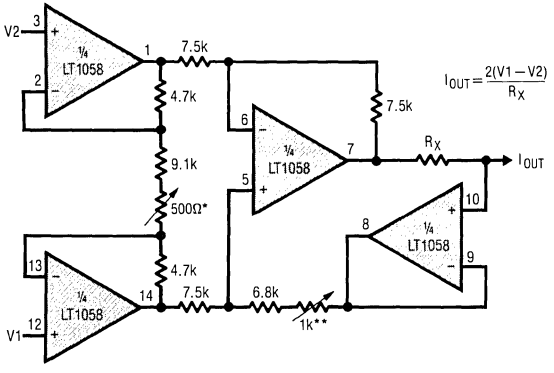
DESCRIPTION

The LT1057 is a matched JFET input dual op amp in the industry standard 8 pin configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

The LT1058 is the lowest offset quad JFET input operational amplifier in the standard 14 pin configuration. It offers significant accuracy improvement over presently available JFET input quad operational amplifiers. It can replace four single precision JFET input op amps, while saving board space, power dissipation and cost.

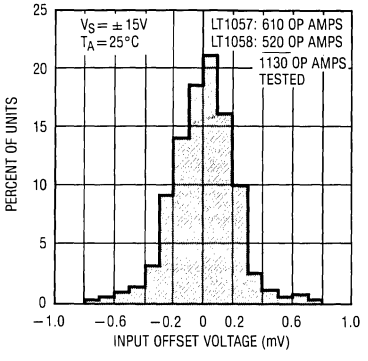
Both the LT1057 and LT1058 are available in all standard packages: plastic and hermetic DIP and (LT1057 only) metal can.

Current Output, High Speed, High Input Impedance Instrumentation Amplifier



*GAIN ADJUST
**COMMON-MODE REJECTION ADJUST
BANDWIDTH ≈ 2MHz

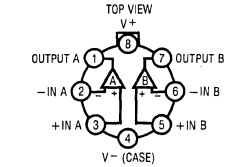
Distribution of Offset Voltage (All Packages, LT1057 and LT1058)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1057AM/LT1057M/
LT1058AM/LT1058M ..... –55°C to 125°C
LT1057AC/LT1057C/
LT1058AC/LT1058C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

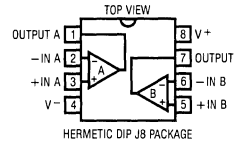
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE

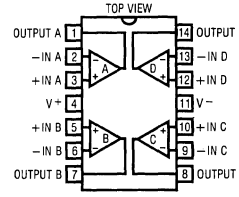
ORDER PART NO.

LT1057AMH
LT1057MH
LT1057ACH
LT1057CH



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE

LT1057AMJ8
LT1057MJ8
LT1057ACJ8
LT1057CJ8
LT1057ACN8
LT1057CN8



HERMETIC DIP J14 PACKAGE
PLASTIC DIP N14 PACKAGE

LT1058AMJ
LT1058MJ
LT1058ACJ
LT1058CJ
LT1058ACN
LT1058CN

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC MIN	TYP	MAX	LT1057M/LT1058M LT1057C/LT1058C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1057		150	450		200	800	μV
		LT1058		180	600		250	1000	μV
I_{OS}	Input Offset Current	Fully Warmed Up		3	40		4	50	pA
I_b	Input Bias Current	Fully Warmed Up		±5	±50		±7	±75	pA
	Input Resistance-Differential			10^{12}			10^{12}		Ω
	-Common-Mode	V_{CM} = –11V to 8V		10^{12}			10^{12}		Ω
		V_{CM} = 8V to 11V		10^{11}			10^{11}		Ω
	Input Capacitance			4			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1057		2.0			2.1		μVp-p
		0.1Hz to 10Hz LT1058		2.4			2.5		μVp-p
e_n	Input Noise Voltage Density	f_O = 10Hz		26			28		nV/√Hz
		f_O = 1kHz (Note 2)		13	22		14	24	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, 1kHz (Note 3)		1.5	4		1.8	6	fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, R_L = 2k	150	350		100	300		V/mV
		$V_O = \pm 10V$, R_L = 1k	120	250		80	220		V/mV
	Input Voltage Range		±10.5	14.3 –11.5		±10.5	14.3 –11.5		V
CMRR	Common-Mode Rejection Ratio	LT1057	86	100		82	98		dB
		LT1058	84	98		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to ±18V	88	103		86	102		dB
V_{OUT}	Output Voltage Swing	R_L = 2k	±12	±13		±12	±13		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC MIN	TYP	MAX	LT1057M/LT1058M LT1057C/LT1058C MIN	TYP	MAX	UNITS
SR	Slew Rate		10	14		8	13		V/μs
GBW	Gain-Bandwidth Product	f = 1MHz (Note 5)	3.5	5		3	5		MHz
I_S	Supply Current Per Amplifier			1.6	2.5		1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		132			130		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AC LT1058AC MIN	TYP	MAX	LT1057C LT1058C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1057	●		250	800		330	1400	μV
		LT1058	●		300	1200		400	1800	μV
	Average Temperature Coefficient of Input Offset Voltage	LT1057 H/J8 Package	●		1.8	7		2.3	12	μV/°C
		N8 Package	●		3	10		4	16	μV/°C
		LT1058 J Package (Note 4)	●		2.5	10		3	15	μV/°C
		N Package (Note 4)	●		4	15		5	22	μV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70°C$			18	150		20	250	pA
I_b	Input Bias Current	Warmed Up, $T_A = 70°C$			±50	±250		±60	±350	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	70	220		50	200		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	98		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	87	102		84	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.8		±12	±12.8		V
I_S	Supply Current Per Amplifier		●			2.8			3.2	mA
		$T_A = 70°C$			1.4			1.5		mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AM LT1058AM MIN	TYP	MAX	LT1057M LT1058M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1057	●		300	1100		400	2000	μV
		LT1058	●		380	1600		550	2500	μV
	Average Temperature Coefficient of Input Offset Voltage	LT1057	●		2.0	7		2.5	12	μV/°C
		LT1058 (Note 4)	●		2.5	10		3	15	μV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 125°C$			0.15	2		0.2	3	nA
I_b	Input Bias Current	Warmed Up, $T_A = 125°C$			±0.6	±4.5		±0.7	±6	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120		30	110		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	84	97		80	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	86	100		83	98		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.7		±12	±12.6		V
I_S	Supply Current Per Amplifier	$T_A = 125°C$			1.25	1.9		1.3	2.2	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; i.e., out of 100 LT1058s or (100 LT1057s), typically 240 op amps (or 120 for the LT1057) will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula:

$i_n = (2qI_b)^{1/2}$

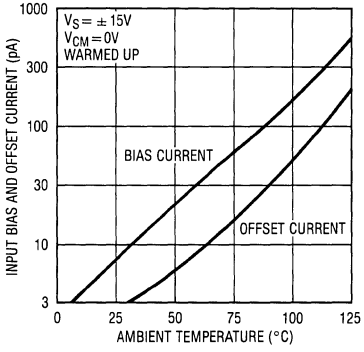
where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 4: This parameter is not 100% tested.

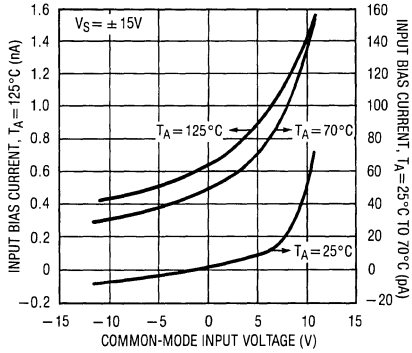
Note 5: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

TYPICAL PERFORMANCE CHARACTERISTICS

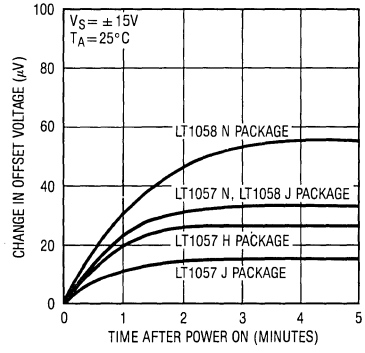
Input Bias and Offset Currents vs Temperature



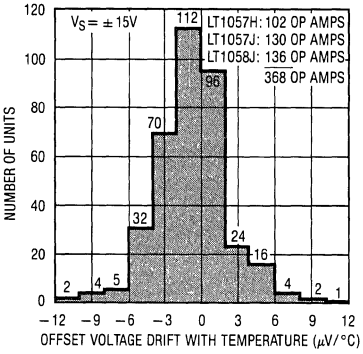
Input Bias Current Over the Common-Mode Range



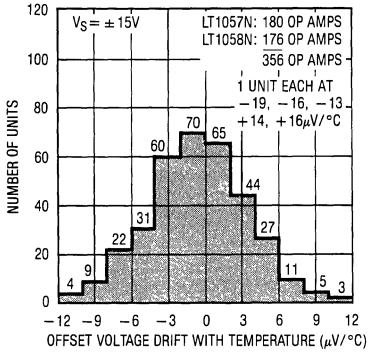
Warm-Up Drift



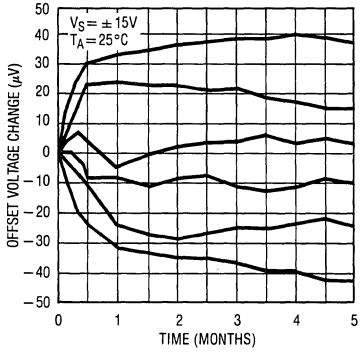
Distribution of Offset Voltage Drift with Temperature (H and J Package)



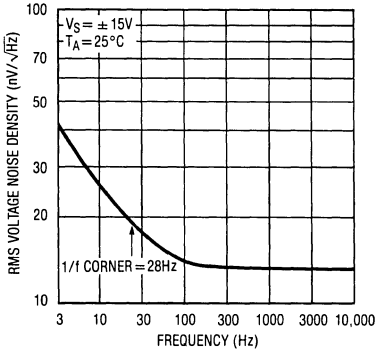
Distribution of Offset Voltage Drift with Temperature (Plastic N Package)



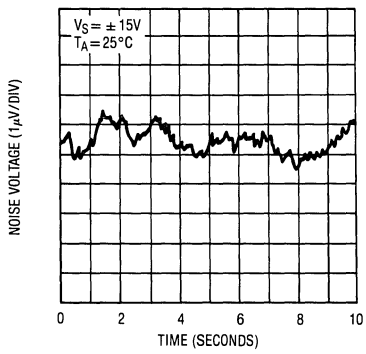
Long Term Drift of Representative Units



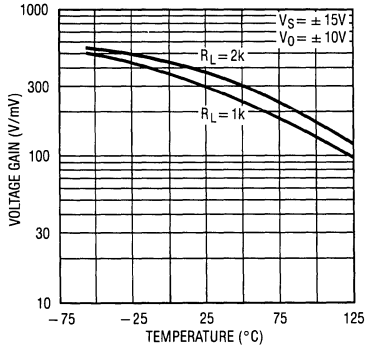
Voltage Noise vs Frequency



0.1Hz to 10Hz Noise

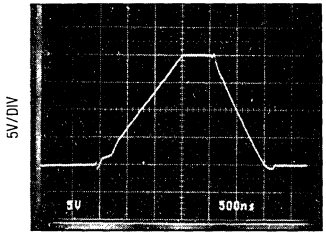


Voltage Gain vs Temperature



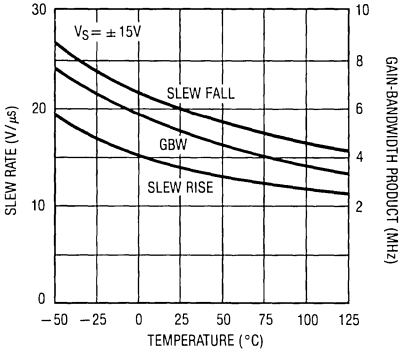
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Response

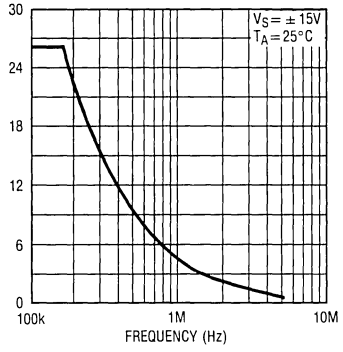


$A_V = +1$, $C_L = 100pF$, $0.5\mu s/DIV$

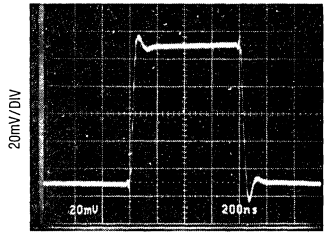
Slew Rate, Gain-Bandwidth Product vs Temperature



Undistorted Output Swing vs Frequency

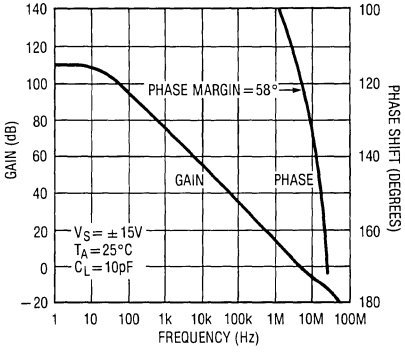


Small Signal Response

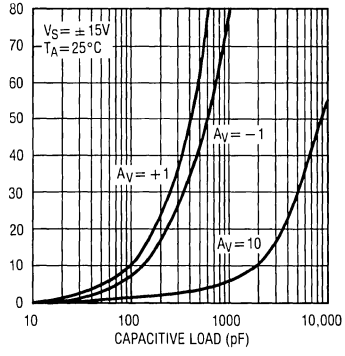


$A_V = +1$, $C_L = 100pF$, $0.2\mu s/DIV$

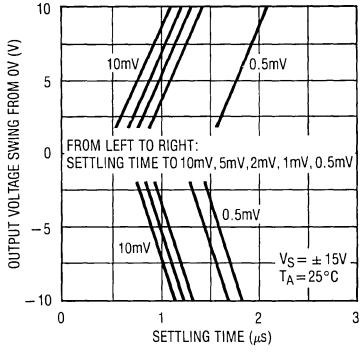
Gain, Phase Shift vs Frequency



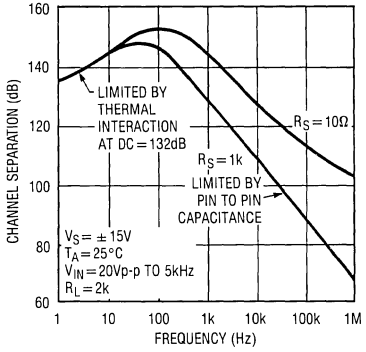
Capacitive Load Handling



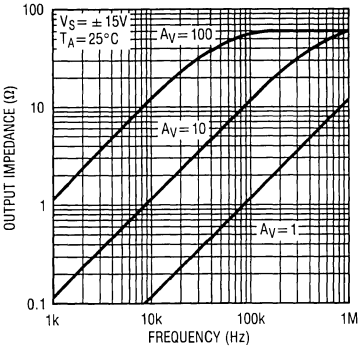
Settling Time



Channel Separation vs Frequency

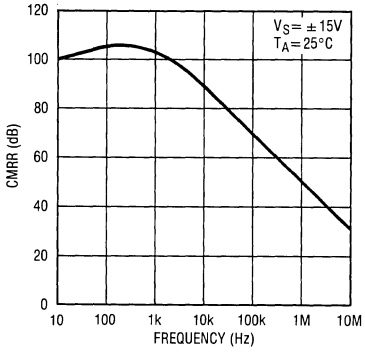


Output Impedance vs Frequency

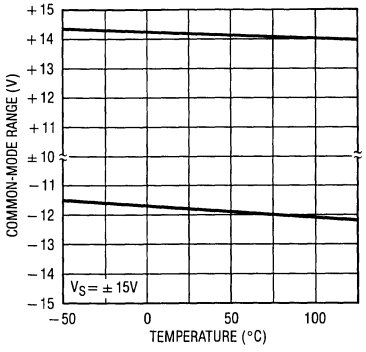


TYPICAL PERFORMANCE CHARACTERISTICS

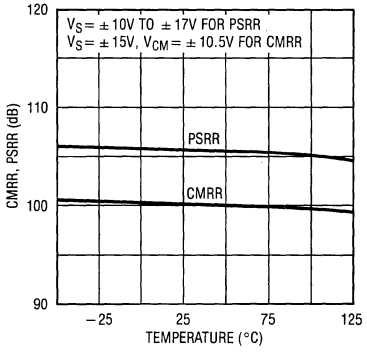
Common-Mode Rejection Ratio vs Frequency



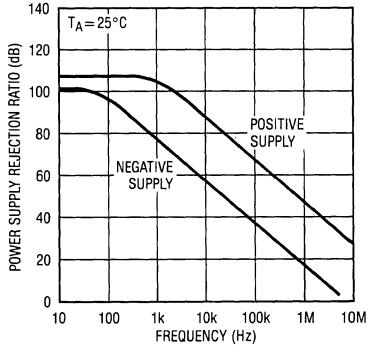
Common-Mode Range vs Temperature



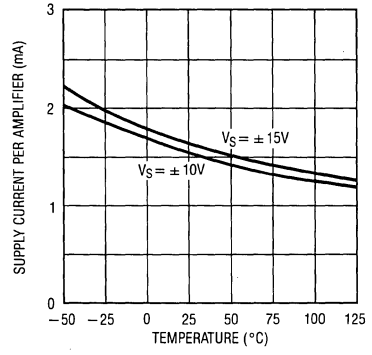
Common-Mode and Power Supply Rejections vs Temperature



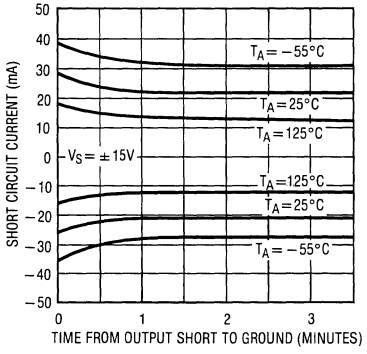
Power Supply Rejection Ratio vs Frequency



Supply Current vs Temperature



Short Circuit Current vs Time (One Output Shorted to Ground)

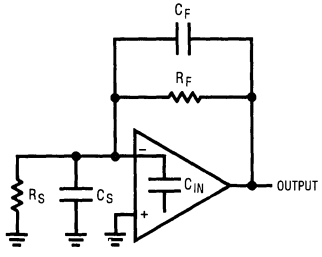


APPLICATIONS INFORMATION

The LT1057 may be inserted directly into LF353, LF412, LF442, TL072, TL082 and OP-215 sockets. The LT1058 plugs into LF347, LF444, TL074, TL084 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



APPLICATIONS INFORMATION

Settling time is measured in a test circuit which can be found in the LT1055/LT1056 data sheet and in Application Note 10.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1057/LT1058, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs; in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1057/LT1058 have the lowest offset voltage of any dual and quad JFET input op amps available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Teflon™ is a trademark of DuPont.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 40μV hysteresis (50μV on the M grades) when cycled over the −55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than 20μV) hysteresis effect.

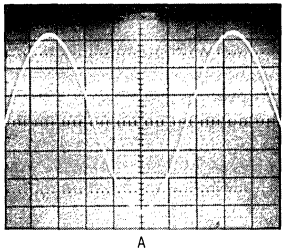
The offset voltage and drift performance are also affected by packaging. In the plastic N package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device drift is degraded. Consequently, for best drift performance, as shown in the typical performance distribution plots, the J or H packages are recommended.

In applications where speed and picoampere bias currents are not necessary, Linear Technology offers the bipolar input, pin compatible LT1013 and LT1014 dual and quad op amps. These devices have significantly better DC specifications than any JFET input device.

Phase Reversal Protection

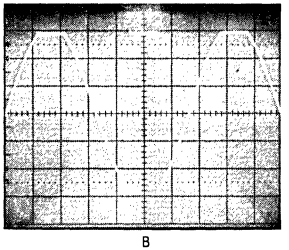
Most industry standard JFET input single, dual and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, TL084) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., below −12V with ±15V supplies). The photos show a ±16V sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1057/LT1058 (C).

The phase reversal of photo (B) can cause lock-up in servo systems. The LT1057/LT1058 does not phase-reverse due to a unique phase reversal protection circuit.



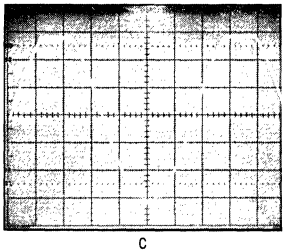
A

(A) ±16V Sine Wave Input



B

(B) LF412A Output



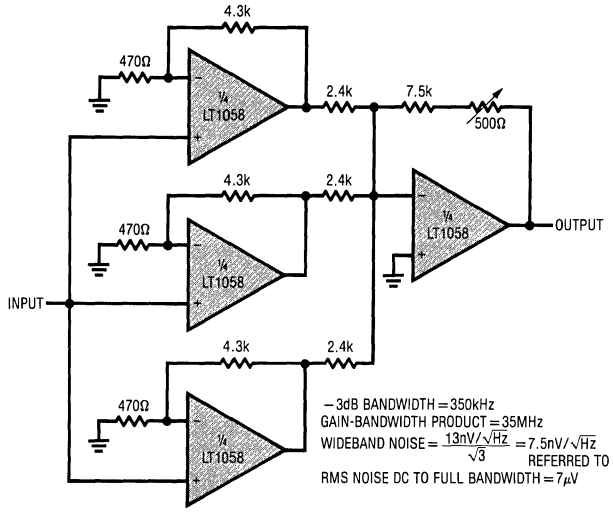
C

(C) LT1057/LT1058 Output

All Photos 5V/Div Vertical Scale, 50μs/Div Horizontal Scale

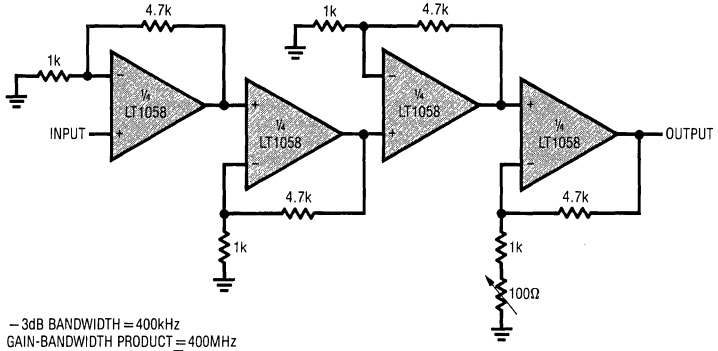
APPLICATIONS

Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



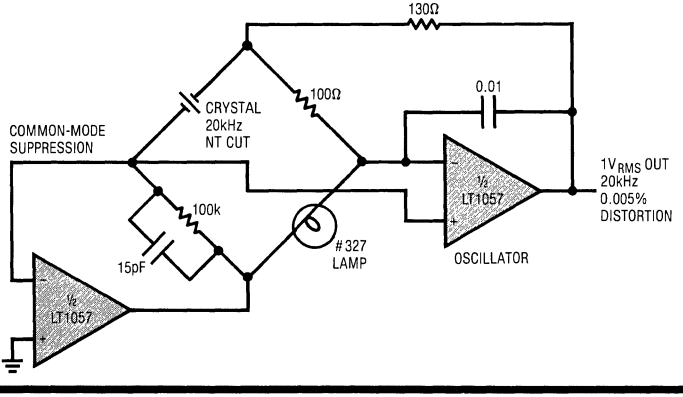
–3dB BANDWIDTH = 350kHz
GAIN-BANDWIDTH PRODUCT = 35MHz
WIDEBAND NOISE = $\frac{13nV/\sqrt{Hz}}{\sqrt{3}}$ = 7.5nV/$\sqrt{Hz}$ REFERRED TO INPUT
RMS NOISE DC TO FULL BANDWIDTH = 7μV

Wideband, High Input Impedance, Gain = 1000 Amplifier



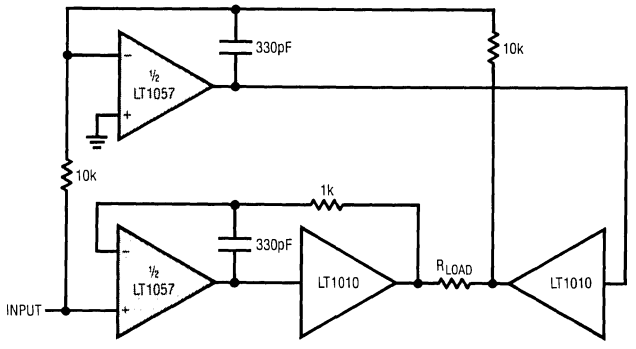
–3dB BANDWIDTH = 400kHz
GAIN-BANDWIDTH PRODUCT = 400MHz
WIDEBAND NOISE = 13nV/$\sqrt{Hz}$ REFERRED TO INPUT

Low Distortion, Crystal Stabilized Oscillator



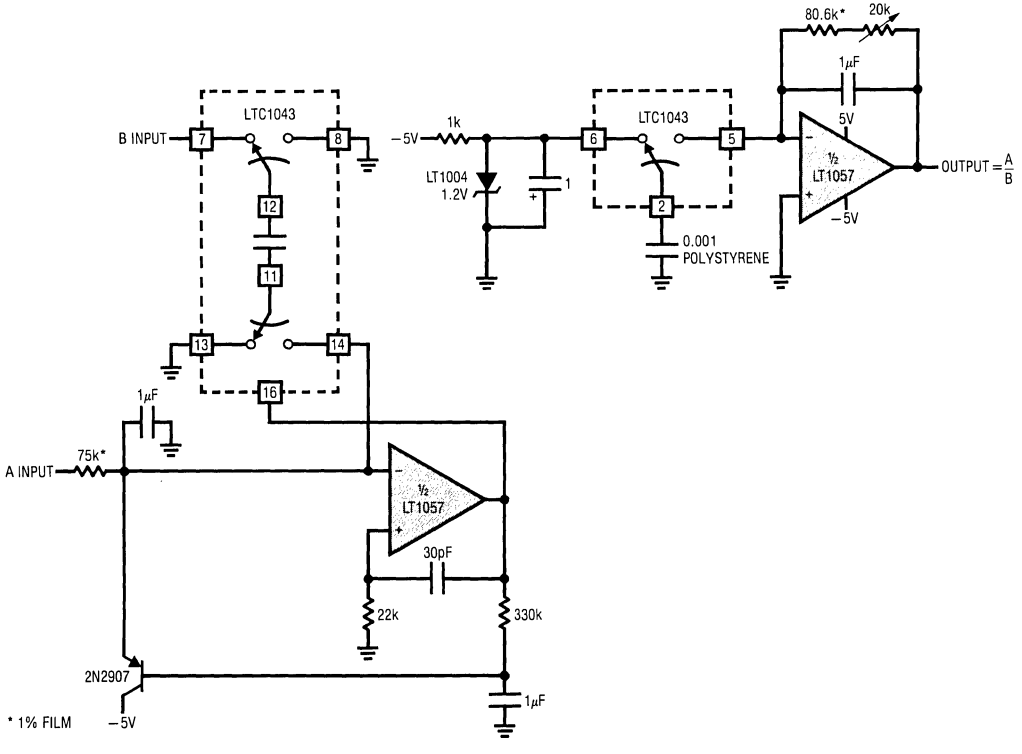
APPLICATIONS

Fast, Precision Bridge Amplifier



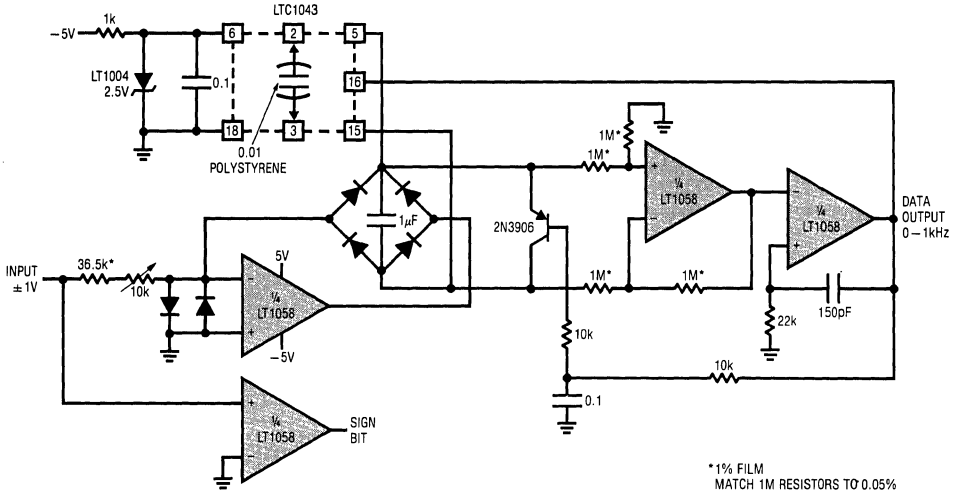
SLEW RATE = 14V/μs
OUTPUT CURRENT TO LOAD = 150mA
LOAD CAPACITANCE: UP TO 1μF

Analog Divider

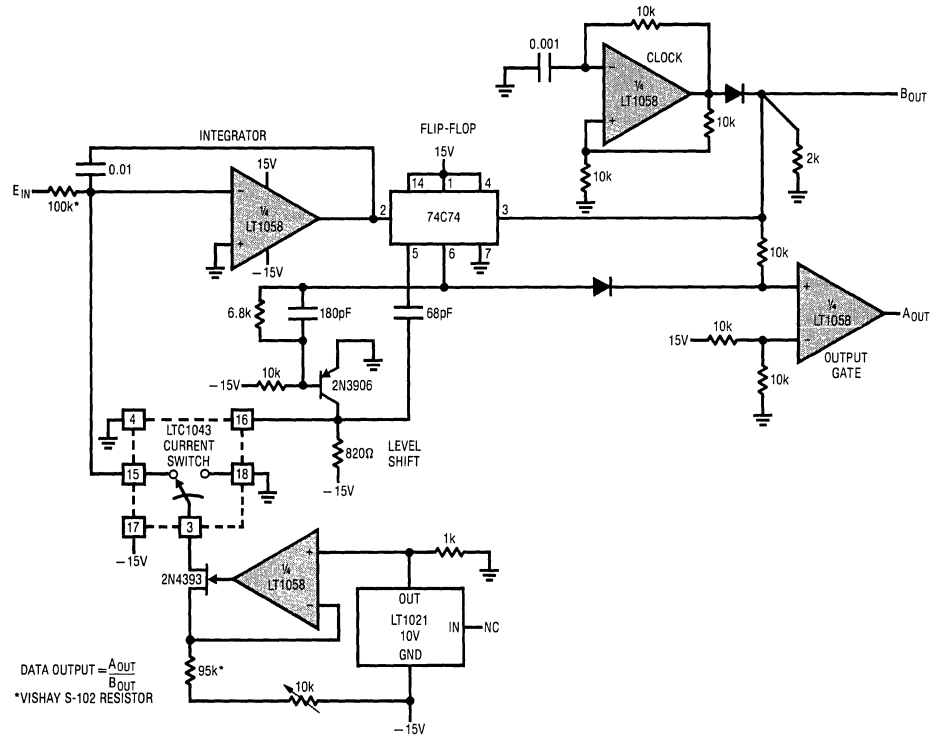


APPLICATIONS

Bipolar Input (AC) V→F Converter

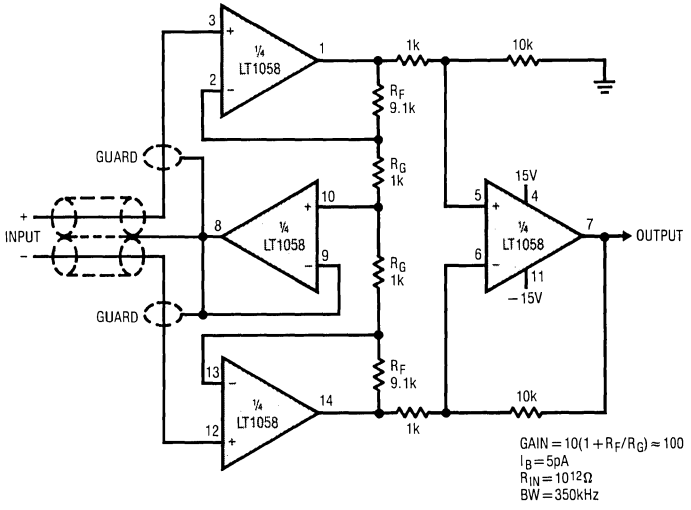


12 Bit A→D Converter

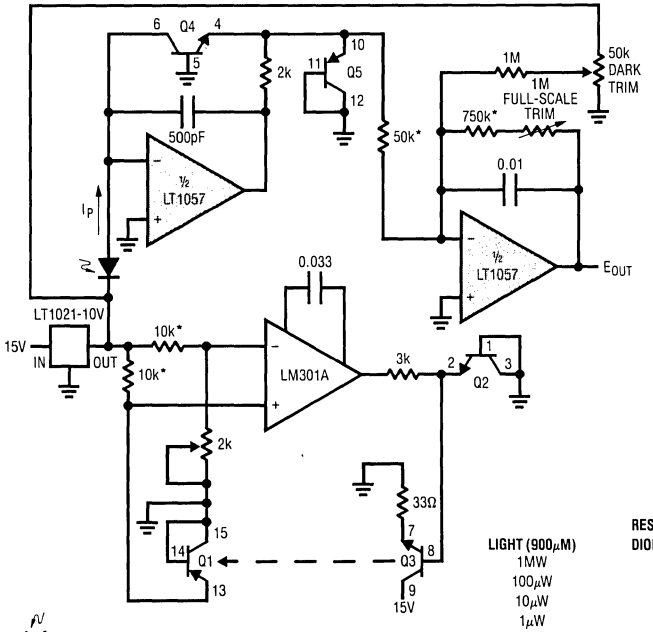


APPLICATIONS

Instrumentation Amplifier with Shield Driver



100dB Range Logarithmic Photodiode Amplifier



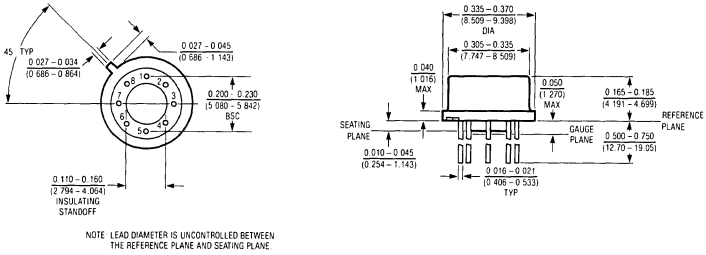
= HP-5082-4204 PIN PHOTODIODE.

Q1–Q5 = CA3096.
CONNECT SUBSTRATE OF CA3096 ARRAY TO Q4'S EMITTER.
*1% RESISTOR
100dB RANGE LOGARITHMIC PHOTODIODE AMPLIFIER

LIGHT (900μM)	RESPONSE DATA DIODE CURRENT	CIRCUIT OUTPUT
1MW	350μA	10.0V
100μW	35μA	7.85V
10μW	3.5μA	5.70V
1μW	350nA	3.55V
100nW	35nA	1.40V
10nW	3.5nA	−0.75V

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

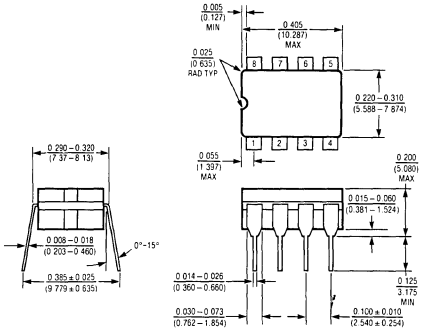
H Package
Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

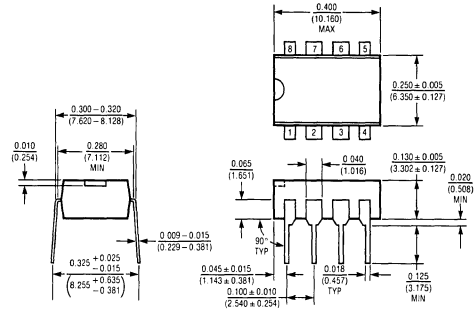
T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

J8 Package
8 Lead Hermetic Dip



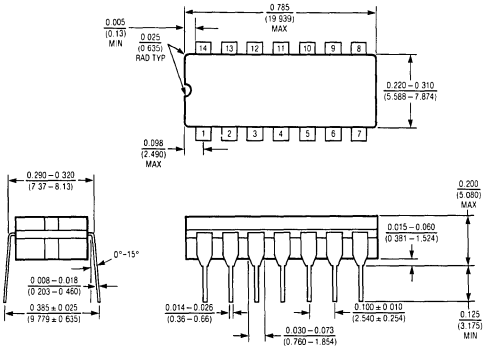
T_{jmax}	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



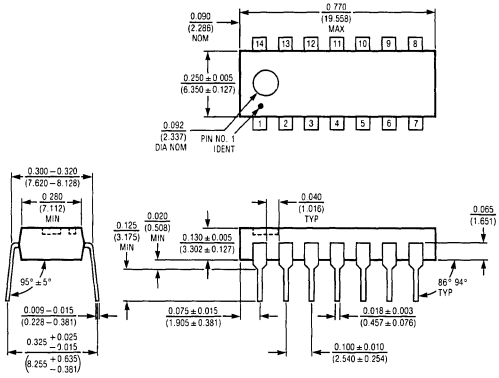
T_{jmax}	θ_{ja}
100°C	130°C/W

J Package
14-Lead Hermetic DIP



T_{jmax}	θ_{ja}
150°C	100°C/W

N Package
14-Lead Plastic



T_{jmax}	θ_{ja}
110°C	130°C/W

Dual Precision JFET Input Operational Amplifiers

FEATURES

- Internally Trimmed Offset Voltage — 1mV Max.
- Offset Voltage Drift — 10μV/°C Max.
- High Slew Rate — 10V/μs Min.
- Wide Bandwidth — 3.5MHz Min.
- Low Supply Current per Amplifier — 1.8mA Typ.
- Low Input Bias Current — 10pA Typ.
- Standard 8-Pin Configuration
- All Packages Available: Metal Can, Hermetic DIP, Plastic DIP

APPLICATIONS

- Sample and Hold Amplifiers
- Output Amplifier for Dual Current Output DACs
- High Speed Integrators
- Photocell Amplifiers
- High Input Impedance Instrumentation Amplifiers

DESCRIPTION

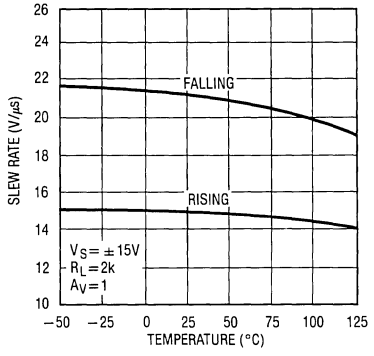
Linear Technology's LF412A and OP-215 series of dual JFET input op amps feature several improvements compared to similar types from other manufacturers.

Both devices have lower input bias and offset currents over the entire temperature range, and are available in all standard 8-pin packages.

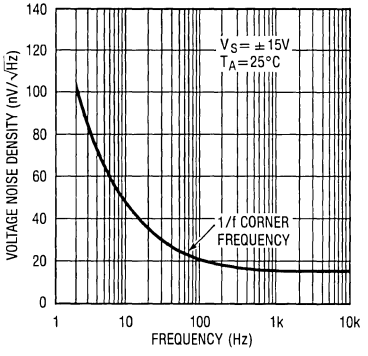
In addition, Linear's LF412A has lower voltage noise and higher voltage gain. Linear's OP-215 supply currents are nearly halved.

Please see the LT1057/LT1058 data sheet for applications requiring higher performance. The LT1057 is a pin compatible JFET input dual, the LT1058 is a JFET input quad op amp in the standard 14-pin DIP configuration.

Slew Rate



Voltage Noise Density vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LF412AM/AC, OP-215A/E..... ±22V
- LF412M/C, OP-215C/G ..... ±18V

Internal Power Dissipation 670mW

Operating Temperature Range
- LF412AM/M, OP-215A/C..... –55°C to 125°C
- LF412AC/C, OP-215E/G .....0°C to 70°C

Differential Input Voltage
- LF412AM/AC, OP-215A/E..... ±40V
- LF412M/C, OP-215C/G.....±30V

Input Voltage (Note A)
- LF412AM/AC, OP-215A/E..... ±20V
- LF412M/C, OP-215C/G ..... ±16V

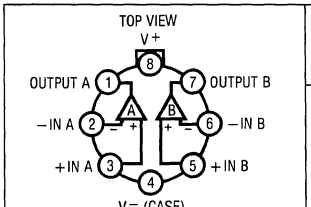
Output Short Circuit Duration .....Indefinite

Storage Temperature Range..... –65°C to 150°C

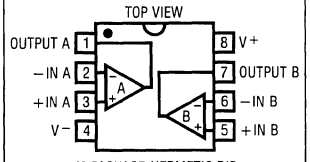
Lead Temperature (Soldering, 10 sec).....300°C

Note A: Maximum negative input voltage is equal to the negative supply voltage.

PACKAGE/ORDER INFORMATION



H PACKAGE METAL CAN



J8 PACKAGE HERMETIC DIP
N8 PACKAGE PLASTIC DIP

ORDER PART NUMBER	
LF412AMH	OP-215AH
LF412MH	OP-215CH
LF412ACH	OP-215EH
LF412CH	OP-215GH
LF412AMJ8	OP-215AJ8
LF412MJ8	OP-215CJ8
LF412ACJ8	OP-215EJ8
LF412CJ8	OP-215GJ8
LF412ACN8	OP-215EN8
LF412CN8	OP-215GN8

ELECTRICAL CHARACTERISTICS

V_S = ±20V for LF412A, V_S = ±15V for all other grades. V_{CM} = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-215A/E MIN	OP-215A/E TYP	OP-215A/E MAX	LF412AM/AC MIN	LF412AM/AC TYP	LF412AM/AC MAX	LF412, OP-215C/G MIN	LF412, OP-215C/G TYP	LF412, OP-215C/G MAX	UNITS
V_{OS}	Input Offset Voltage		—	0.2	1.0	—	0.3	1.0	—	0.5	3.0	mV
I_{OS}	Input Offset Current	T_j = 25°C (Note 1) Warmed-Up V_S = ±15V	— —	6 10	50 100	— —	6 10	50 100	— —	10 15	100 200	pA pA
I_B	Input Bias Current	T_j = 25°C (Note 1) Warmed-Up V_S = ±15V	— —	±10 ±15	±100 ±300	— —	±10 ±15	±100 ±300	— —	±15 ±20	±200 ±400	pA pA
R_{IN}	Input Resistance		—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V V_S = ±15V	150	400	—	100	300	—	50	250	—	V/mV
V_O	Output Voltage Swing	R_L = 10kΩ, V_S = ±15V R_L = 2kΩ, V_S = ±15V	±12 ±11	±13 ±12.7	— —	±12 ±11	±13 ±12.7	— —	±12 ±11	±13 ±12.7	— —	V V
I_S	Supply Current		—	3.8	6.0	—	3.6	5.6	—	3.8	6.8	mA
SR	Slew Rate	V_S = ±15V	10	15	—	10	15	—	8	13	—	V/μs
GBW	Gain Bandwidth Product	V_S = ±15V (Note 2)	3.5	5.7	—	3.5	5.7	—	3.0	5.5	—	MHz
	Settling Time	to 0.01% to 0.10%	— —	2.3 1.1	— —	— —	2.3 1.1	— —	— —	2.4 1.2	— —	μs μs
	Input Voltage Range		±11	+14.5 –11.5	—	±16	+19.5 –16.5	—	±11	+14.5 –11.5	—	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±16V V_{CM} = ±11V V_{CM} = ±10.5V	— 78 86	— 100 100	— — —	80 — —	100 — —	— — —	— 72 82	— 100 100	— — —	dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±20V V_S = ±10V to ±18V	— 86	— 100	— —	80 —	100 —	— —	— 80	— 100	— —	dB dB
e_n	Input Noise Voltage Density	f_o = 100Hz f_o = 1000Hz	— —	20 15	— —	— —	20 15	— —	— —	20 15	— —	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_o = 100Hz f_o = 1000Hz	— —	0.01 0.01	— —	— —	0.01 0.01	— —	— —	0.01 0.01	— —	pA/√Hz pA/√Hz
	Channel Separation	f = 1Hz to 20kHz	—	120	—	—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 20V$ for LF412A, $V_S = \pm 15V$ for all other grades. $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-215A MIN	OP-215A TYP	OP-215A MAX	LF412AM MIN	LF412AM TYP	LF412AM MAX	LF412M, OP-215C MIN	LF412M, OP-215C TYP	LF412M, OP-215C MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	0.5	2.0	—	0.7	2.0	—	1.0	5.0	mV
	Average Input Offset Voltage Drift		●	—	3 (Note 3)	10	—	4	10	—	5 (Note 3)	20	µV/°C
I_{OS}	Input Offset Current	$T_j = 125°C$ (Note 1) $T_A = 125°C$, Warmed-Up $V_S = \pm 15V$	● ●	— —	0.8 1.2	8 14	— —	0.8 1.2	8 14	— —	1.0 1.5	12 22	nA nA
I_B	Input Bias Current	$T_j = 125°C$ (Note 1) $T_A = 125°C$, Warmed-Up $V_S = \pm 15V$	● ●	— —	±1.5 ±2.2	±10 ±18	— —	±1.5 ±2.2	±10 ±18	— —	±1.8 ±2.7	±15 ±28	nA nA
	Input Voltage Range	OP-215	●	±10.3	+14.5 −11.5	—	—	—	—	±10.3	+14.5 −11.5	—	V
		LF412	●	—	—	—	±16	+19.5 −16.5	—	±11	+14.5 −11.5	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 16V$ $V_{CM} = \pm 11V$ $V_{CM} = \pm 10.3V$	● ● ●	— — 82	— — 100	— — —	80 — —	100 — —	— — —	— 70 80	— 100 100	— — —	dB dB dB
I_S	Supply Current		●	—	4.2	6.8	—	4.0	5.6	—	4.2	6.8	mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$ $V_S = \pm 10V$ to $\pm 16V$	● ●	— 80	— 100	— —	80 —	100 —	— —	— 78	— 100	— —	dB dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	●	30	150	—	30	150	—	25	150	—	V/mV
V_O	Output Voltage Swing	$R_L \ge 10k\Omega$, $V_S = \pm 15V$	●	±12	±13	—	±12	±13	—	±12	±13	—	V

ELECTRICAL CHARACTERISTICS

$V_S = \pm 20V$ for LF412A, $V_S = \pm 15V$ for all other grades. $V_{CM} = 0V$, $0°C \le T_A \le 70°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-215E MIN	OP-215E TYP	OP-215E MAX	LF412AC MIN	LF412AC TYP	LF412AC MAX	LF412C, OP-215G MIN	LF412C, OP-215G TYP	LF412C, OP-215G MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	0.4	1.65	—	0.5	1.45	—	0.7	3.9	mV
	Average Input Offset Voltage Drift		●	—	3 (Note 3)	15	—	4	10	—	5 (Note 3)	20	µV/°C
I_{OS}	Input Offset Current	$T_j = 70°C$ (Note 1) $T_A = 70°C$, Warmed-Up $V_S = \pm 15V$	● ●	— —	0.06 0.08	0.45 0.8	— —	0.06 0.08	0.45 0.8	— —	0.08 0.10	0.65 1.2	nA nA
I_B	Input Bias Current	$T_j = 70°C$ (Note 1) $T_A = 70°C$, Warmed-Up $V_S = \pm 15V$	● ●	— —	±0.12 ±0.16	±0.7 ±1.4	— —	±0.12 ±0.16	±0.7 ±1.4	— —	±0.14 ±0.19	±0.9 ±1.8	nA nA
	Input Voltage Range	OP-215	●	±10.3	+14.5 −11.5	—	—	—	—	±10.3	+14.5 −11.5	—	V
		LF412	●	—	—	—	±16	+19.5 −11.5	—	±11	+14.5 −11.5	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 16V$ $V_{CM} = \pm 11V$ $V_{CM} = \pm 10.3V$	● ● ●	— — 80	— — 100	— — —	80 — —	100 — —	— — —	— 70 76	— 100 100	— — —	dB dB dB
I_S	Supply Current		●	—	4.0	6.8	—	3.8	5.6	—	4.0	6.8	mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$ $V_S = \pm 10V$ to $\pm 16V$	● ●	— 80	— 100	— —	80 —	100 —	— —	— 76	— 100	— —	dB dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	●	50	180	—	50	180	—	35	180	—	V/mV
V_O	Output Voltage Swing	$R_L \ge 10k\Omega$, $V_S = \pm 15V$	●	±12	±13	—	±12	±13	—	±12	±13	—	V

The ● denotes the specifications which apply over the full operating temperature range. The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

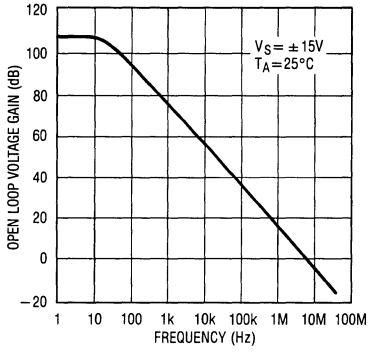
Note 1: Input bias and offset currents are specified for two different conditions. The T_j specification is with the junction at ambient temperature; the warmed-up specification is with the device operating in a warmed-up condition at the ambient temperature specified.

Note 2: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

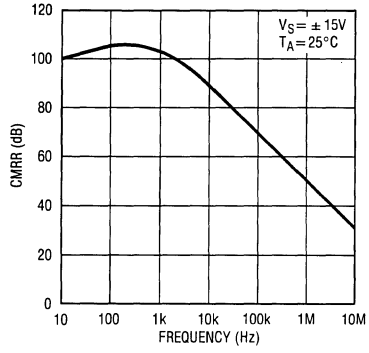
Note 3: The LF412A is 100% tested to this specification. All other grades are sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

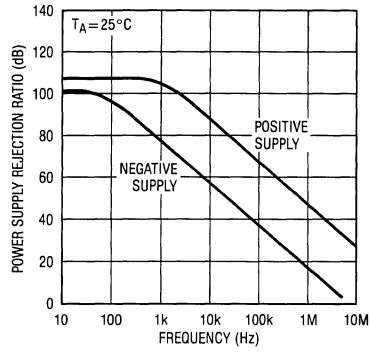
Open-Loop Frequency Response



Common-Mode Rejection Ratio vs Frequency



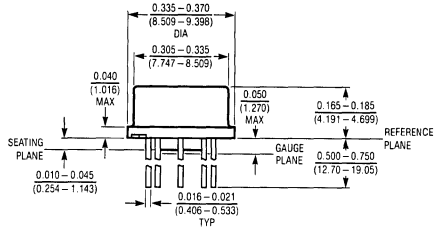
Power Supply Rejection Ratio vs Frequency

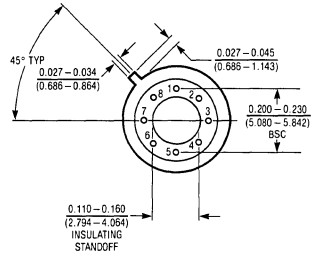


PACKAGE DESCRIPTIONS

Dimensions in inches (millimeters) unless otherwise noted.

H Package
TO-5 Metal Can

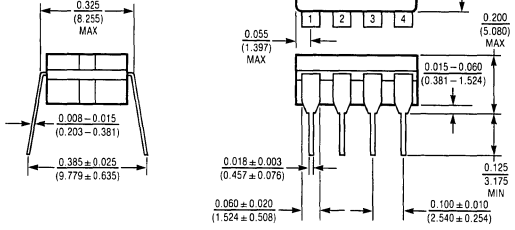




NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

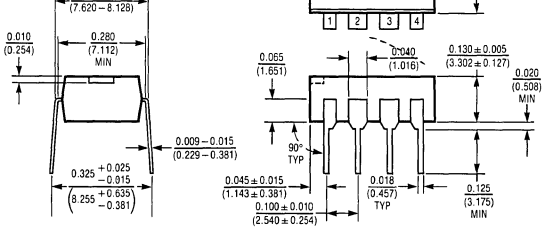
$T_j$max	θ_{ja}	θ_{jc}
165°C	140°C/W	40°C/W

J Package
8 Lead Cerdip



$T_j$max	θ_{ja}
155°C	100°C/W

N Package
8 Lead Molded Dip



$T_j$max	θ_{ja}
115°C	130°C/W

SECTION 3—VOLTAGE REGULATORS

SECTION 3—VOLTAGE REGULATORS

MILITARY

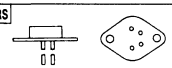
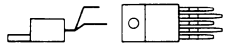
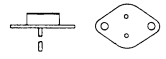
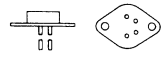
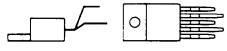
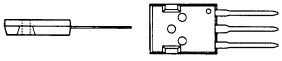
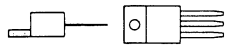
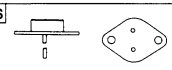
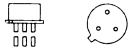
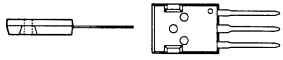
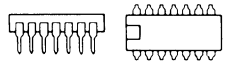
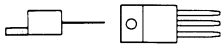
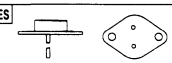
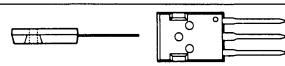
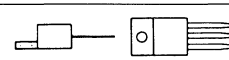
I_O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V_{IN} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURES/COMMENTS
10.0	Pos. Adj.	LT1038MK	Steel TO-3	35	1.2 to 33	0.8% V_{OUT} Tol., Plug In Compatible with 117, 150, 138.
7.5	Pos. Adj.	LT1083MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V_{REF} Tol. Pin Compatible with 117, 150, 138 Types
5.0	Pos. Fixed	LT1003MK	Steel TO-3	20	5	2% V_{OUT} Tol.
	Pos. Adj.	LT138AK LM138K LT1084MK	Steel TO-3 Steel TO-3	35 35	1.2 to 33 1.2 to 34	LT138A Has 1% V_{REF} Tol. Low Dropout (1.2V), 1% V_{REF} Tol. Pin Compatible with 117, 150, 138 Types
	Switching	LT1070MK LT1070HVMK	Steel TO-3 Steel TO-3	40 60	* *	Self Contained PWM and 5 Amp Switch in a 5-Pin Package
3.0	Pos. Fixed	LT123AK LM123K	Steel TO-3	20	5	LT123A Has 1% V_{OUT} Tol.
	Pos. Adj.	LT150AK LM150K LT1085MK	Steel TO-3 Steel TO-3	35 35	1.2 to 33 1.2 to 34	LT150A Has 1% V_{REF} Tol. Low Dropout (1.2V), 1% V_{REF} Tol. Pin Compatible with 138 Types
	Neg. Adj.	LT1033MK	Steel TO-3	40	−1.2 to −37	2% V_{REF} Tol.
	Dual Pos. Fixed	LT1035MK	Steel TO-3	20	Two 5V Outputs	Logic Controlled Main Output Voltage, 75mA
	Positive	LT1036MK	Steel TO-3	30	12, 5	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output
2.5	Switching	LT1071MK LT1071HVMK	Steel TO-3 Steel TO-3	40 60	* *	Self Contained PWM and 2.5 Amp Switch in a 5-Pin Package
0.5 to 1.5	Pos. Adj.	LT117AK LM117K LT117AH LM117H	Steel TO-3 TO-39	40 40	1.2 to 37	LT117A Has 1% V_{REF} Tol.
	Neg. Adj.	LT137AK LM137K LT137AH LM137H	Steel TO-3 TO-39	40 40	−1.2 to −37	LT137A Has 1% V_{REF} Tol.
	Pos. Adj. High Voltage	LT117AHVK LM117HVK LT117AHVH LM117HVH	Steel TO-3 TO-39	60 60	1.2 to 57	LT117AHV Has 1% V_{REF} Tol.
	Neg. Adj. High Voltage	LT137AHVK LM137HVK LT137AHVH LM137HVH	Steel TO-3 TO-39	50 50	−1.2 to −47	LT137AHV Has 1% V_{REF} Tol.
1.25	Switching	LT1072MK LT1072HVMK	Steel TO-3 Steel TO-3	40 60	* *	Self Contained PWM and 1.25 Amp Switch in a 5-Pin Package
1.0	Dual Pos. Fixed	LT1005MK	Steel TO-3	20	Two 5V Outputs	Logic Controlled 1 Amp Main Output Voltage, 35mA Auxiliary Output
125mA	Positive	LT1020MJ	14 Pin CERDIP	36	4 to 30	Dropout Voltage = 0.5V, 40μA I_O, Reference and Comparator

COMMERCIAL

I_O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V_{IN} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURES/COMMENTS
10.0	Pos. Adj.	LT1038CK	Steel TO-3	35	1.2 to 33	2% V_{OUT} Tol., Plug In Compatible with 117, 150, 138.
7.5	Pos. Adj.	LT1083CK LT1083CP	Steel TO-3 Plastic TO-247	30 30	1.2 to 29 1.2 to 29	Low Dropout (1.2V) Pin Compatible with 317, 350, 338 Types
5.0	Pos. Fixed	LT1003CK	Steel TO-3	20	5	2% V_{OUT} Tol.
	Pos. Adj.	LT338AK LM338K LT1084CK LT1084CP	Steel TO-3 Steel TO-3 Plastic TO-247	35 30 30	1.2 to 33 1.2 to 29 1.2 to 29	LT338A Has 1% V_{REF} Tol. Low Dropout (1.2V) Pin Compatible with 317, 350, 338 Types Low Dropout (1.2V) Pin Compatible with 317, 350, 338 Types
	Switching	LT1070CK LT1070CT LT1070HVCK LT1070HVCT	Steel TO-3 TO-220 Steel TO-3 TO-220	40 40 60 60	* * * *	Self Contained PWM and 5 Amp Switch in a 5-Pin Package.
3.0	Pos. Fixed	LT323AK LM323K LT323AT	Steel TO-3 TO-220	20 20	5	LT323A Has 1% V_{OUT} Tol.
	Pos. Adj.	LT350AK LM350K LT350AT LM350T LT1085CK LT1058CT	Steel TO-3 TO-220 Steel TO-3 Plastic TO-220	35 35 30 30	1.2 to 33 1.2 to 33 1.2 to 29 1.2 to 29	LT350A Has 1% V_{REF} Tol. Low Dropout (1.2V) Pin Compatible with 338 Types
	Neg. Adj.	LT1033CK LT1033CT	Steel TO-3 TO-220	40 40	−1.2 to −37	2% V_{REF} Tol.
	Dual Pos. Fixed	LT1035CK LT1035CT	Steel TO-3 TO-220	20 20	Two 5V Outputs	Logic Controlled Main Output Voltage, 75mA Auxiliary Output
	Positive	LT1036CK LT1036CT	Steel TO-3 TO-220	30 30	12, 5 12, 5	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output
2.5	Switching	LT1071CK LT1071CT LT1071HVCK LT1071HVCT	Steel TO-3 TO-220 Steel TO-3 TO-220	40 40 60 60	* * * *	Self Contained PWM and 2.5 Amp Switch in a 5-Pin Package
0.5 to 1.5	Pos. Adj.	LT317AK LM317K LT317AH LM317H LT317AT LM317T	Steel TO-3 TO-39 TO-220	40 40 40	1.2 to 37	LT317A Has 1% V_{REF} Tol.
	Neg. Adj.	LT337AK LM337K LT337AH LM337H LT337AT LM337H	Steel TO-3 TO-39 TO-220	40 40 40	−1.2 to −37	LT337A Has 1% V_{REF} Tol.
	Pos. Adj. High Voltage	LT317AHVK LM317HVK LT317AHVH LM317HVH	Steel TO-3 TO-39	60 60	1.2 to 57	LT317HV Has 1% V_{REF} Tol.
	Neg. Adj. High Voltage	LT337AHVK LM337HVK LT337AHVH LM337HVH	Steel TO-3 TO-39	50 50	−1.2 to −47	LT337HV Has 1% V_{REF} Tol.
1.25	Switching	LT1072CK LT1072CT LT1072HVCK LT1072HVCT	Steel TO-3 Plastic TO-220 Steel TO-3 Plastic TO-220	40 40 60 60	* * * *	Self Contained PWM and 1.25 Amp Switch in a 5-Pin Package
1.0	Dual Pos. Fixed	LT1005CK LT1005CT	Steel TO-3 TO-220	20 20	Two 5V Outputs	Logic Controlled Main Output Voltage
125mA	Positive	LT1020CJ LT1020CN	14 Pin CERDIP 14 Pin Plastic	36	4 to 30 4 to 30	Dropout Voltage = 0.5V, 40μA I_O, Reference and Comparator

*The I_O values for the LT1070 and LT1071 are switch current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

REGULATOR SELECTION GUIDE

	MILITARY	COMMERCIAL	FEATURES
SWITCHING REGULATORS 	LT1070MK LT1070HVMK	LT1070CK LT1070HVCK	Current Mode PWM with Self-Protected 5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
	LT1071MK LT1071HVMK	LT1071CK LT1071HVCK	Current Mode PWM with Self-Protected 2.5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
	LT1072MK LT1072HVMK	LT1072CK LT1072HVCK	Current Mode PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
		LT1070CT LT1070HVCT	Current Mode PWM with Self-Protected 5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
		LT1071CT LT1071HVCT	Current Mode PWM with Self-Protected 2.5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
		LT1072CT LT1072HVCT	Current Mode PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
POSITIVE FIXED 	LT1003MK LT123AK LM123K	LT1003CK LT323AK LT323K	5V ± 2%, 5 Amp 5V ± 1%, 3 Amp 5V ± 3%, 3 Amp
	LT1005MK	LT1005CK	Dual Output Regulator with 5V 1 Amp Logic Switchable Output and Auxiliary 5V 35mA Output
	LT1035MK	LT1035CK	Dual Output Regulator with 5V 3 Amp Logic Switchable Output and Auxiliary 5 75mA Output
	LT1036MK	LT1036CK	Dual Output Regulator with 12V 3 Amp Logic Switchable Output and Auxiliary 5V 75mA Output
		LT1005CT	Dual Output Regulator with 5V 1 Amp Logic Switchable Output and Auxiliary 5V 35mA Output
		LT1035CT	Dual Output Regulator with 5V 3 Amp Logic Switchable Output and Auxiliary 5V 75mA Output
		LT1036CT	Dual Output Regulator with 12V 3 Amp Logic Switchable Output and Auxiliary 5V 75mA Output
		LT1003CP LT323AP LM323P	5V ± 2%, 5 Amp 5V ± 1%, 3 Amp 5V ± 3%, 3 Amp
		LT323AT	5V ± 1%, 3 Amp
POSITIVE ADJUSTABLES 	LT1038MK LT1083MK LT1084MK LT138AK LM138K LT1085MK LT150AK LM150K LM117AK LM117K LT117AHVK LM117AHVK	LT1038CK LT1083CK LT1084CK LT338AK LM338K LT1085CK LT350AK LM350K LT317AK LM317K LT317AHVK LM317AHVK	To Amp 7.5 Amp Low Dropout 5 Amp Low Dropout 5 Amp 1% Reference 5 Amp 3 Amp Low Dropout 3 Amp 1% Reference 3 Amp 1.5 Amp 1% Reference 1.5 Amp 1.5 Amp 1% Reference, Hi Voltage 1.5 Amp, Hi Voltage
	LT117AH LM117H LM117AHVH LM117HVH	LT317AH LM317H LT317AHVH LM317HVH	0.5 Amp 1% Reference 0.5 Amp 0.5 Amp 1% Reference, Hi Voltage 0.5 Amp, Hi Voltage
		LT1083CP LT1084CP LT338AP LM338P LT350AP LM350P	7.5 Amp Low Dropout 5 Amp Low Dropout 5 Amp 1% Reference 5 Amp 3 Amp 1% Reference 3 Amp
	LT1020MJ	LT1020CJ LT1020CN	Very Low Dropout Voltage, 40μA Supply Current, 2.5V Independent Reference, and Voltage Comparator on Same Chip.
		LT1085CT LT350AT LM350T LT317AT LM317T	3 Amp Low Dropout 3 Amp 1% Reference 3 Amp 1.5 Amp 1% Reference 1.5 Amp
NEGATIVE ADJUSTABLES 	LT137AK LM137K LT137AHVK LM137HVK LT1033MK	LT337K LM337K LT337AHVK LT337HVK LT1033CK	1.5 Amp 1% Reference 1.5 Amp 1.5 Amp 1% Reference, Hi Voltage 1.5 Amp, Hi Voltage 3 Amp 2% Reference
	LT137AH LM137H LT137AHVH LM137HVH	LT337AH LM337H LT337AHVH LM337HVH	0.5 Amp 1% Reference 0.5 Amp 0.5 Amp 1% Reference, Hi Voltage 0.5 Amp, Hi Voltage
		LT1033CP	3 Amp 2% Reference
		LT337AT LM337T LT1033CT	1.5 Amp 1% Reference 1.5 Amp 3 Amp 2% Reference

Micropower Regulator and Comparator

FEATURES

- 40μA Supply Current
- 125mA Output Current
- 2.5V Reference Voltage
- Reference Output Sources 1mA and Sinks 0.5mA
- Dual Output Comparator
- Comparator Sinks 10mA
- Dropout Detector
- 0.2V Dropout Voltage
- Thermal Limiting
- Available in SO Package

APPLICATIONS

- Battery Systems
- Battery Backup System
- Portable Terminals
- Portable Instruments

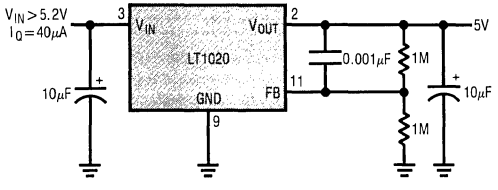
DESCRIPTION

The LT1020 is a combination micropower positive regulator and free collector comparator on a single monolithic chip. With only 40μA supply current, the LT1020 can supply over 125mA of output current. Input voltage range is from 4.5V to 36V and dropout voltage is 0.6V at 125mA. Dropout voltage decreases with lower load currents. Also included on the chip is a class B output 2.5V reference that can either source or sink current. A dropout detector provides an output current to indicate when the regulator is about to drop out of regulation.

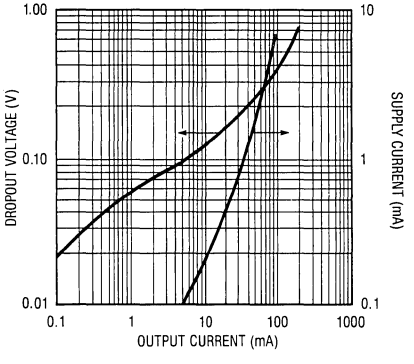
The dual output comparator can be used as a comparator for system or battery monitoring. For example, the comparator can be used to warn of low system voltage while the dropout detector shuts down the system to prevent abnormal operation. Frequency compensation of the comparator for amplifier applications can be obtained by adding external output capacitance. Dual output or positive and negative regulators can also be made.

The 2.5V reference will source or sink current. This allows it to be used as a supply splitter or auxiliary output.

5V Regulator



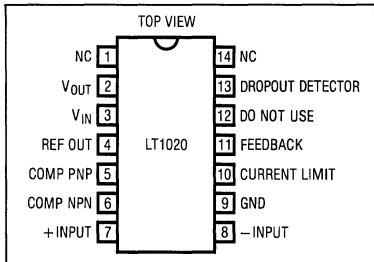
Dropout Voltage and Supply Current



ABSOLUTE MAXIMUM RATINGS

Input Voltage 36V
NPN Collector Voltage 36V
PNP Collector Voltage ..... Supply – 36V
Output Short Circuit Duration ..... Indefinite
Power Dissipation ..... Internally Limited
Operating Temperature Range
LT1020C ..... 0°C to 100°C
LT1020M ..... – 55°C to 125°C
Storage Temperature Range
LT1020C,M ..... – 65°C to 150°C

PACKAGE/ORDER INFORMATION



J14 PACKAGE HERMETIC DIP
N14 PACKAGE PLASTIC DIP

ORDER PART NUMBER

LT1020MJ
LT1020CJ
LT1020CN

(ALSO AVAILABLE IN SO PACKAGE)

ELECTRICAL CHARACTERISTICS T_j = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
Reference Voltage	$4.5V \le V_{IN} \le 36V$	2.46	2.50	2.54	V
Line Regulation	$4.5V \le V_{IN} \le 36V$		0.01	0.015	%/V
Load Regulation	$-0.5mA \le I_{REF} \le 1mA$, $V_{IN} = 12V$		0.2	0.3	%
Output Source Current	$V_{IN} = 5V$	1	4		mA
Output Sink Current	$V_{IN} = 5V$	0.5	2		mA
Temperature Stability			1		%
Regulator					
Supply Current	$V_{IN} = 6V$, $I_{OUT} \le 100\mu A$ $V_{IN} = 36V$, $I_{OUT} \le 100\ \mu A$ $V_{IN} = 12V$, $I_{OUT} = 125mA$		45 75 11	80 120 20	μA μA mA
Output Current	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$	125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$		0.2	0.5	%
Line Regulation	$6V \le V_{IN} \le 36V$		0.01	0.015	%/V
Dropout Voltage	$I_{OUT} = 100\mu A$ $I_{OUT} = 125mA$		0.02 0.4	0.05 0.65	V V
Feedback Sense Voltage	$V_{IN} = 12V$	2.44	2.5	2.56	V
Dropout Detector Current	$\Delta V_{OUT} = -0.05V$	3	20		μA
Feedback Bias Current			15	40	nA
Minimum Load Current	$V_{IN} = 36V$		1	5	μA
Short Circuit Current	$V_{IN} = 36V$ Pin 9 and Pin 10 shorted, $V_{IN} = 4.5V$	 3	250 30	360	mA mA
Comparator					
Offset Voltage	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$		3	7	mV
Bias Current	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$		15	40	nA
Offset Current	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$		4	15	nA
Gain-NPN Pulldown	$\Delta V_{OUT} = 29V$, $R_L = 20k$	2000	10000		V/V
Common Mode Rejection	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$	80	94		dB

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator					
Power Supply Rejection	$4.5V \le V_S \le 36V$	80	96		dB
Output Sink Current	$V_{IN} = 4.5V$	10	18		mA
NPN Saturation Voltage	$I_{OUT} = 1mA$		0.4	0.6	V
Output Source Current		60	200		μA
Input Voltage Range		0		$V_{IN} - 1$	V
Response Time			5		μs
Leakage Current (NPN)				2	μA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference						
Reference Voltage	$4.5V \le V_{IN} \le 36V$	●	2.40	2.50	2.55	V
Line Regulation	$4.5V \le V_{IN} \le 36V$	●		0.01	0.02	%/V
Load Regulation	$-0.5mA \le I_{REF} \le 1mA$, $V_{IN} = 12V$	●		0.3	0.4	%
Output Source Current	$V_{IN} = 5V$	●	1			mA
Output Sink Current	$V_{IN} = 5V$	●	0.5			mA
Regulator						
Supply Current	$V_{IN} = 6V$, $I_{OUT} \le 100\mu A$	●		65	95	μA
	$V_{IN} = 36V$, $I_{OUT} \le 100\mu A$	●		85	120	μA
	$V_{IN} = 12V$, $I_{OUT} = 125mA$	●		11	20	mA
Output Current	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$	●	125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \ge 1V$, $V_{IN} \ge 6V$	●			1	%
Line Regulation	$6V \le V_{IN} \le 36V$	●			0.02	%/V
Dropout Voltage	$I_{OUT} = 100\mu A$	●			0.06	V
	$I_{OUT} = 125mA$	●			0.85	V
Feedback Sense Voltage	$V_{IN} = 12V$	●	2.38	2.5	2.57	V
Dropout Detector Current	$\Delta V_{OUT} = -0.05V$	●	3			μA
Feedback Bias Current		●			50	nA
Minimum Load Current	$V_{IN} = 36V$	●			50	μA
Short Circuit Current	$V_{IN} = 36V$	●		240	360	mA
	Pin 9 and Pin 10 shorted, $V_{IN} = 4.5V$	●	2.5	30		mA
Comparator						
Offset Voltage	$0V \le = V_{CM} \le 35V$, $V_{IN} = 36V$	●			10	mV
Bias Current	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$ (Note 1)	●		15	60	nA
Offset Current	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$	●			20	nA
Gain-NPN Pulldown	$\Delta V_{OUT} = 29V$, $R_L = 20k$	●	1000			V/V
Common Mode Rejection	$0V \le V_{CM} \le 35V$, $V_{IN} = 36V$	●	80			dB
Power Supply Rejection	$4.5V \le V_S \le 36V$	●	80			dB
Output Sink Current	$V_{IN} = 4.5V$ (Note 2)	●	5	10		mA
Output Source Current		●	40	120		μA
Input Voltage Range		●	0		$V_{IN} - 1$	V
Leakage Current (NPN)	$V_{IN} = 36V$	●			8	μA

The ● denotes the specifications which apply over full operating temperature range.

Note 1: For $0V \le V_{CM} \le 0.1V$ and $T > 85°C$ I bias max is 100nA.

Note 2: For $T_A \le -40°C$ output sink current min is 2.5mA.

PIN FUNCTIONS

Pins 1, 12, 14—No internal connection.

Pin 2—**Regulator Output.** Main output, requires 10μF output capacitor. Can be shorted to V_{IN} or ground without damaging device.

Pin 3—**Input Supply.** Bypass with 10μF cap. Must always be more positive than ground.

Pin 4—**Reference.** 2.5V can source or sink current. May be shorted to ground or up to 5V. Voltages in excess of 5V can damage the device.

Pin 5—**Comparator PNP Output.** Pull up current source for the comparator. May be connected to any voltage from V_{IN} to 36V more negative than V_{IN} (operates below ground). Short circuit protected. For example, if V_{IN} is 6V then pin 5 will operate to −30V.

Pin 6—**Comparator NPN Output.** May be connected to any voltage from ground to 36V more positive than ground (operates above V_{IN}). Short circuit protected.

Pins 7, 8—**Comparator Inputs.** Operates from ground to V_{IN} − 1V. Comparator inputs will withstand 36V even with V_{IN} of 0V.

Pin 9—**Ground.**

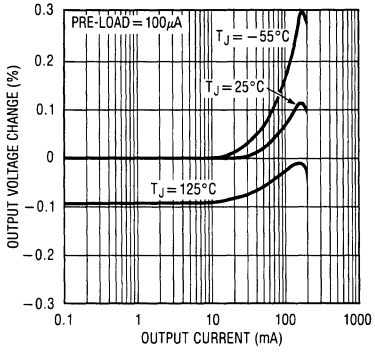
Pin 10—**Current Limit.** Connecting this pin to ground decreases the regulator current limit to 3mA min. Leave open when not used.

Pin 11—**Feedback.** This is the feedback point of the regulator. When operating, it is nominally at 2.5V. Optimum source resistance is 200k to 500k. The feedback pin should not be driven below ground or more positive than 5V.

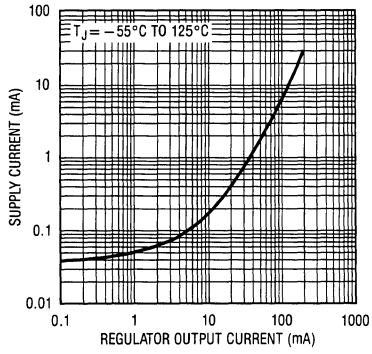
Pin 13—**Dropout Detector.** This pin acts like a current source from V_{IN} which turns on when the output transistor goes into saturation. The magnitude of the current depends on the magnitude of the output current and the input-output voltage differential. Pin current ranges from 5μA to about 300μA.

TYPICAL PERFORMANCE CHARACTERISTICS

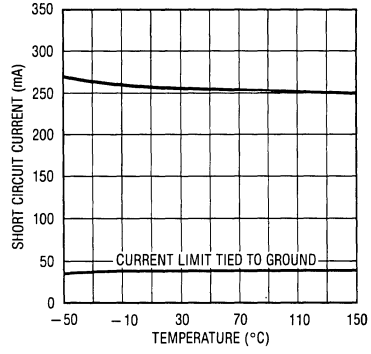
Regulator Load Regulation



Supply Current

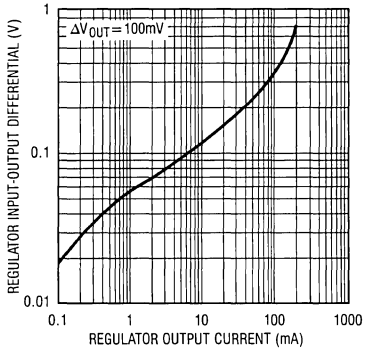


Regulator Short Circuit Current

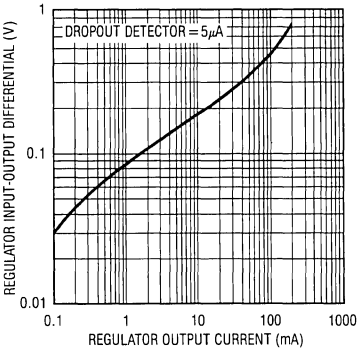


TYPICAL PERFORMANCE CHARACTERISTICS

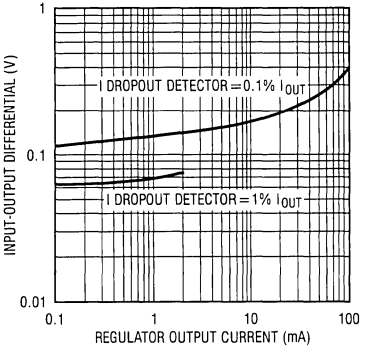
Dropout Voltage



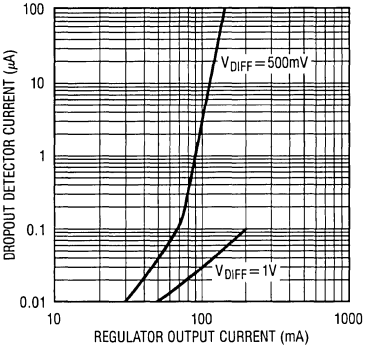
Dropout Voltage



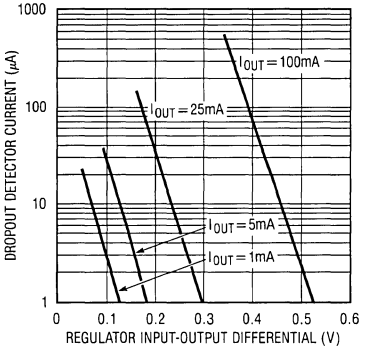
Dropout Voltage



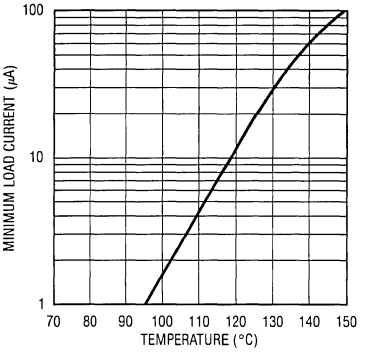
Dropout Detector Current



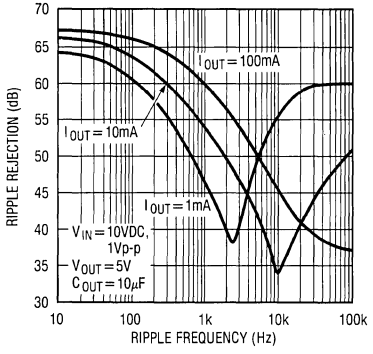
Dropout Detector Current



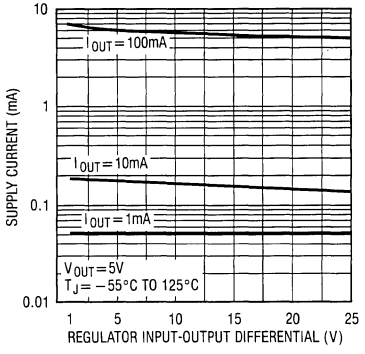
Regulator Minimum Load Current



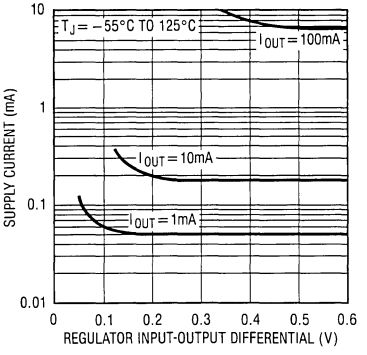
Regulator Ripple Rejection



Supply Current

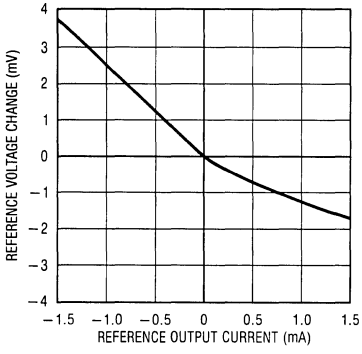


Supply Current at Dropout

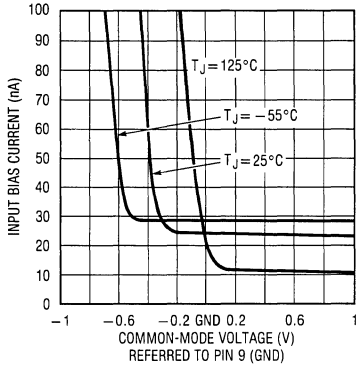


TYPICAL PERFORMANCE CHARACTERISTICS

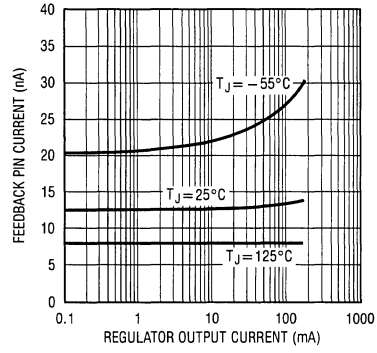
Reference Regulation



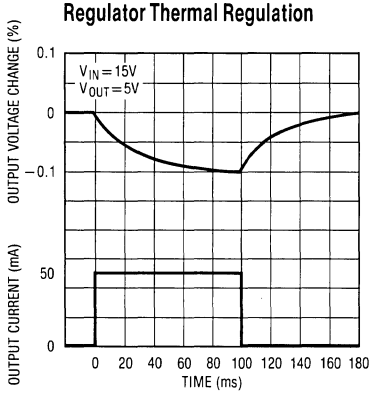
Comparator Input Bias Current



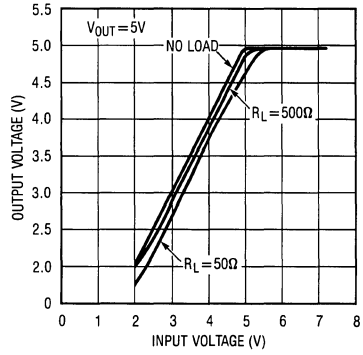
Feedback Pin Current



Regulator Thermal Regulation



LT1020 Turn-On Characteristic



APPLICATION HINTS

The LT1020 is especially suited for micropower system applications. For example, the comparator section of the LT1020 may be used as a battery checker to provide an indication of low battery. The dropout detector can shutdown the system when the battery voltage becomes too low to regulate. Another type of system application for the LT1020 would be to generate the equivalent of split supplies off of a single power input. The regulator section provides regulated output voltage and the reference, which can both source and sink current is then an artificial system ground providing a split supply for the system.

For many applications the comparator can be frequency compensated to operate as an amplifier. Compensation values for various gains are given in the datasheet. The comparator gain is purposely low to make it easier to frequency compensate as an amplifier. Two outputs are available on the comparator, the NPN output is capable of sinking 10mA and can drive loads connected to voltages in excess of the positive power supply. This is useful for driving switches or linear regulators off of a higher input voltage. The PNP output, which is capable of sourcing 100μA can drive loads below ground. It can be used to make negative regulators with the addition of an external pass transistor. Both outputs can be tied together to provide an output that swings from rail-to-rail for comparator or amplifier applications. Although it is not specified, the gain for the PNP output is about 500-1000.

APPLICATION HINTS

If the PNP output is being used, to maximize the gain, a 1-5μA load should be placed upon the NPN output collector. This is easily done by connecting a resistor between the NPN collector and the reference output. (Providing this operating current to the NPN side increases the internal emitter base voltages and maximizes the gain of the PNP stage.) Without this loading on the NPN collector, at temperatures in excess of 75°C, the gain of the PNP collector can decrease by a factor of 2 or 3.

Reference

Internal to the LT1020 is a 2.5V trimmed class B output reference. The reference was designed to be able to source or sink current so it could be used in supply splitting applications as well as a general purpose reference for external circuitry. The design of the reference allows it to source typically 4 or 5mA and sink 2mA. The available source and sink current decreases as temperature increases. It is sometimes desirable to decrease the AC output impedance by placing an output capacitor on them. The reference in the LT1020 becomes unstable with large capacitive loads placed directly on it. When using an output capacitor, about 20Ω should be used to isolate the capacitor from the reference pin. This 20Ω resistor can be placed directly in series with the capacitor or alternatively the reference line can have 20Ω placed in series with it and then a capacitor to ground. This is shown in Figure 1. Other than placing large capacitive loads on the reference, no other precautions are necessary and the reference is stable with nominal stray capacitances.

Overload Protection

The main regulator in the LT1020 is current limited at approximately 250mA. The current limit is stable with both input voltage and temperature. A current limit pin, when strapped to ground, decreases the output current. This allows the output current to be set to a lower value than 250mA. The output current available with the current limit pin strapped to ground is not well controlled so if precise current limiting is desired it should be provided externally as is shown in some of the application circuits.

If the device is overloaded for long periods of time, thermal shutdown turns the output off. In thermal shutdown, there may be some oscillations which can disturb external circuitry. A diode connected between the reference and feedback terminal provides hysteresis under thermal shutdown, so that the device turns on and off with about a 5 second period and there are no higher frequency oscillations. This is shown in Figure 2. This diode is recommended for most applications. Thermal shutdown temperature is set at approximately 145°.

Like most other IC regulators, a minimum load is required on the output of the LT1020 to maintain regulation. For most standard regulators this is normally specified at 5mA. Of course, for a micropower regulator this would be a tremendously large current. The output current must be large enough to absorb all the leakage current of the pass transistor at the maximum operating temperature. It also affects the transient response; low output currents have long recovery times from load transients. At high operating temperatures the minimum load current increases and

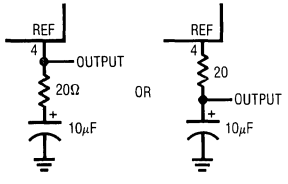


Figure 1. Bypassing Reference

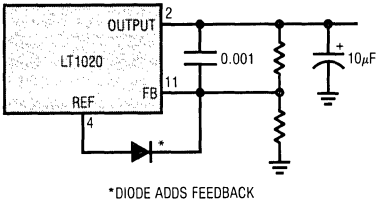


Figure 2. Minimizing Oscillation In Thermal Shutdown

APPLICATION HINTS

having too low of a load current may cause the output to go unregulated. Devices are tested for minimum load current at high temperature. The output voltage setting resistors to the feedback terminal can usually be used to provide the minimum load current.

Frequency Compensation

The LT1020 is frequency compensated by a dominant pole on the output. An output capacitor of 10μF is usually large enough to provide good stability. Increasing the output capacitor above 10μF further improves stability. In order to insure stability, a feedback capacitor is needed between the output pin and the feedback pin. This is because stray capacitance can form another pole with the large value of feedback resistors used with the LT1020. Also, a feedback capacitor minimizes noise pickup and improves ripple rejection.

With the large dynamic operating range of the output current, 10000:1, frequency response changes widely. Low AC impedance capacitors are needed to insure stability. While solid tantalum are best, aluminum electrolytics can be used but larger capacitor values may be needed.

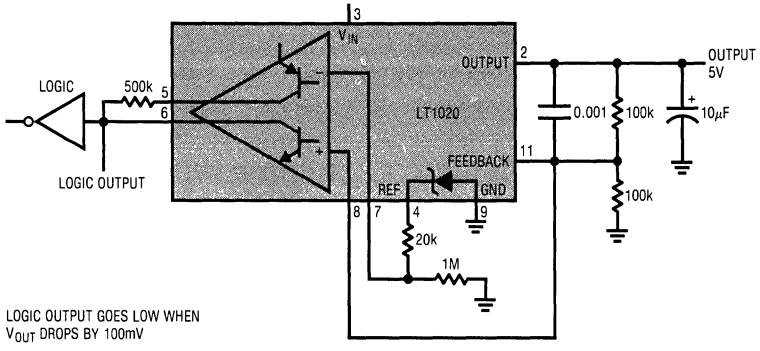
The CURRENT LIMIT pin allows one of the internal nodes to be rolled off with a 0.05μF capacitor to ground. With this capacitor, lower values of regulator output capacitance can be used (down to 1μF) for low (<20mA) output currents. Values of capacitance greater than 0.05μF degrade the transient response, so are not recommended.

If the CURRENT LIMIT pin is connected to GND, the current limit is decreased and only a 1μF output capacitor is needed.

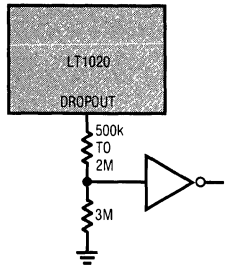
When bypassing the reference, a 20Ω resistor must be connected in series with the capacitor.

TYPICAL APPLICATIONS

Regulator With Output Voltage Monitor

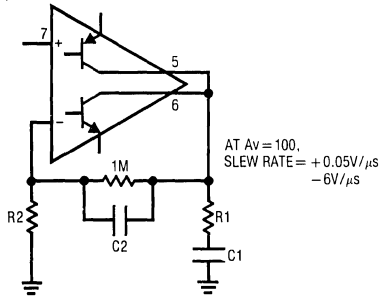


Driving Logic With Dropout Detector



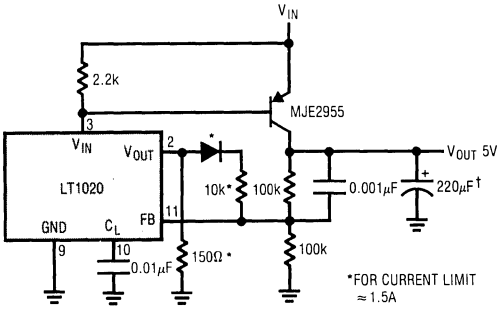
TYPICAL APPLICATIONS

Compensating the Comparator as an Op Amp

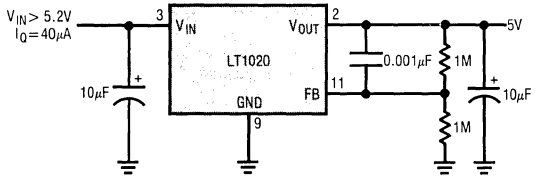


Av	R1	C1	C2	R2
1	33Ω	0.1μF	0.001μF	—
10	100Ω	0.047μF	—	100k
100	10k	0.002μF	—	10k

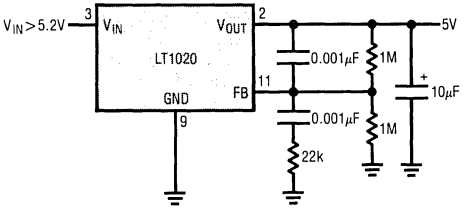
1 Amp Low Dropout Regulator



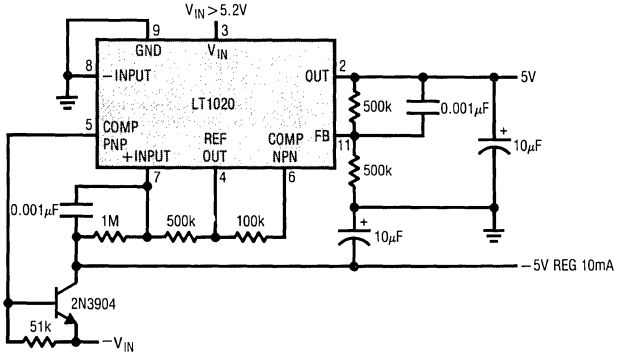
5V Regulator



Regulator with Improved Transient Response

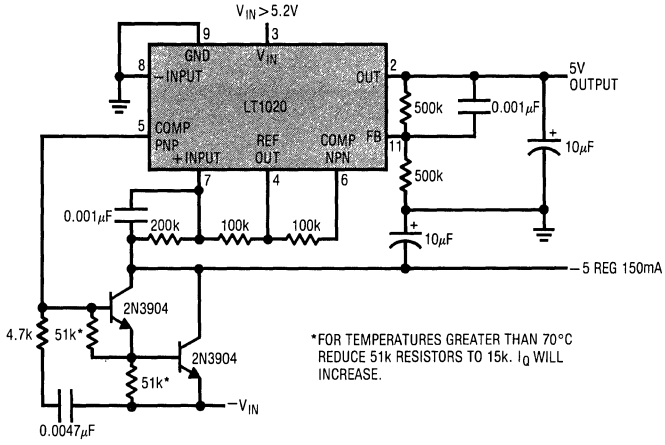


Dual Output Regulator



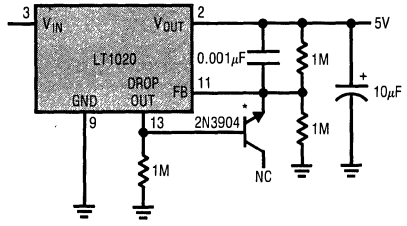
TYPICAL APPLICATIONS

Dual Output 150mA Regulator



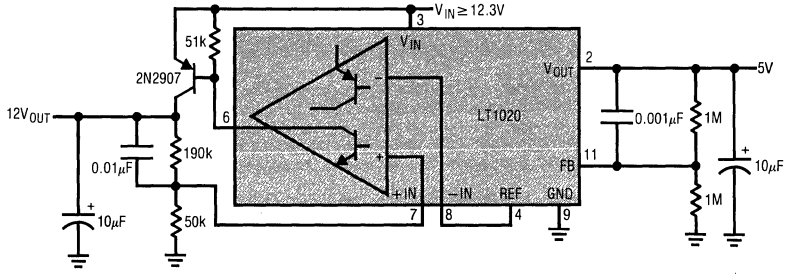
*FOR TEMPERATURES GREATER THAN 70°C REDUCE 51k RESISTORS TO 15k. I_Q WILL INCREASE.

Maintaining Lowest I_Q at Dropout

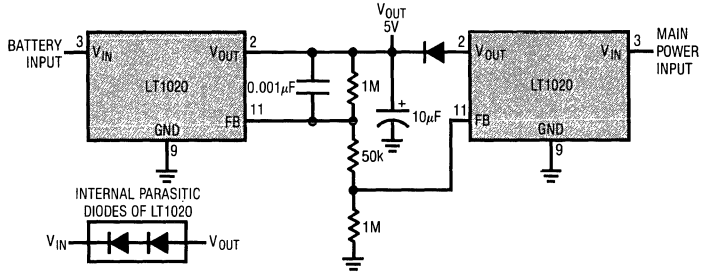


*TRANSISTOR USED BECAUSE OF LOW LEAKAGE CHARACTERISTICS

Dual Output Positive Regulator

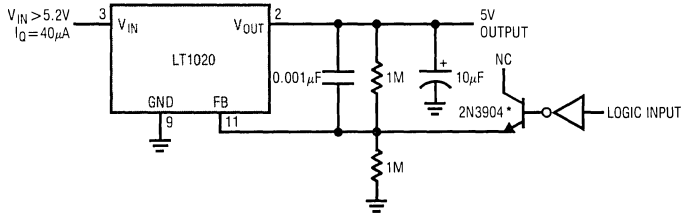


Battery Backup Regulator



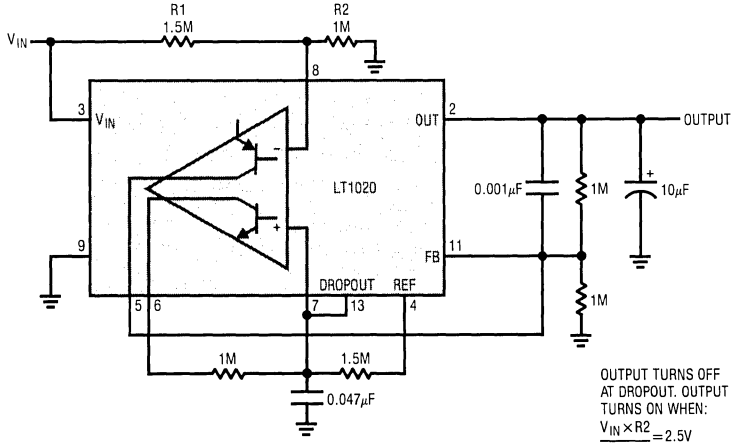
TYPICAL APPLICATIONS

5V Regulator with Shutdown



*TRANSISTOR USED BECAUSE OF LOW LEAKAGE CHARACTERISTICS. TO TURN OFF THE OUTPUT OF THE LT1020 FORCE FB (PIN 11) > 2.5V.

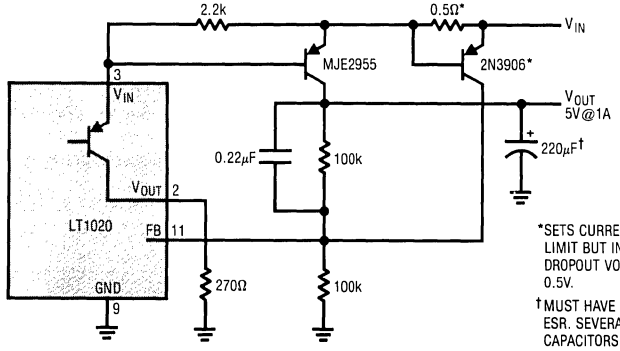
Turn Off at Dropout



OUTPUT TURNS OFF AT DROPOUT. OUTPUT TURNS ON WHEN:

$$\frac{V_{IN} \times R2}{R1 + R2} = 2.5V$$

Current Limited 1 Amp Regulator

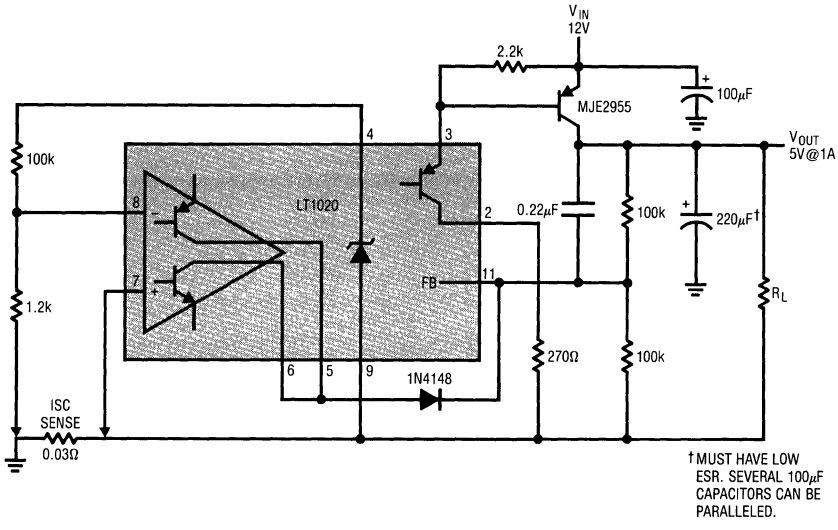


*SETS CURRENT LIMIT BUT INCREASES DROPOUT VOLTAGE BY 0.5V.

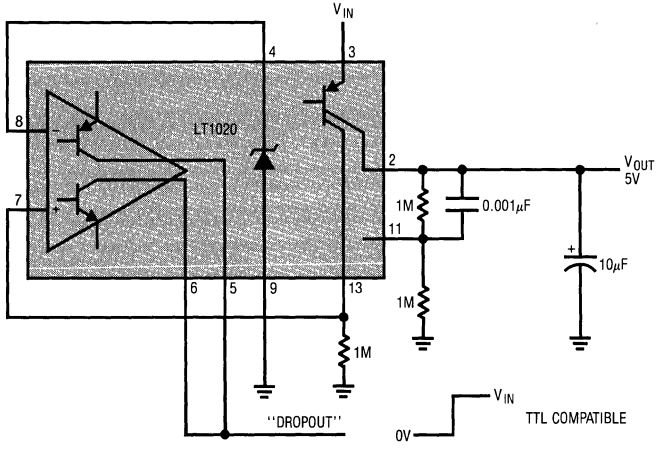
†MUST HAVE LOW ESR. SEVERAL 100μF CAPACITORS CAN BE PARALLELED.

TYPICAL APPLICATIONS

1 Amp Regulator with Current Limit

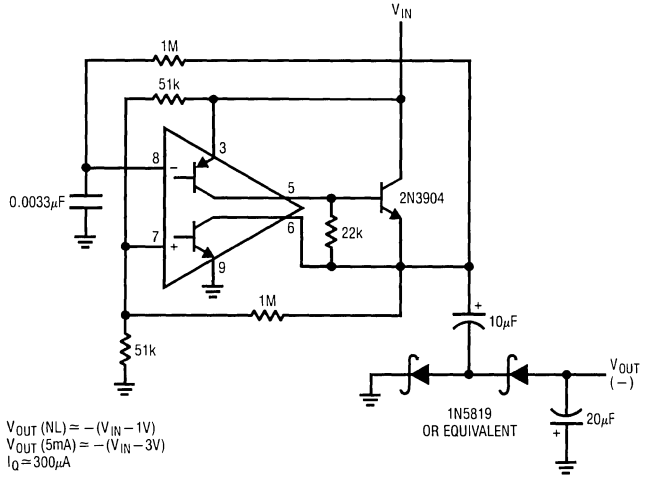


Logic Output on Dropout



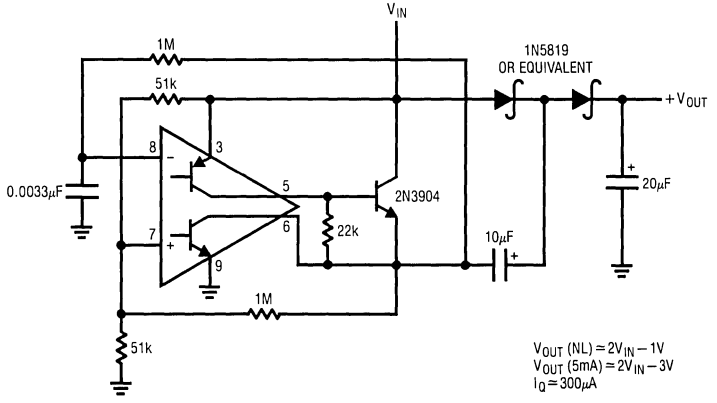
TYPICAL APPLICATIONS

Charge-Pump Negative Voltage Generator



V_{OUT} (NL) ≈ −(V_{IN} − 1V)
V_{OUT} (5mA) ≈ −(V_{IN} − 3V)
I_Q ≈ 300μA

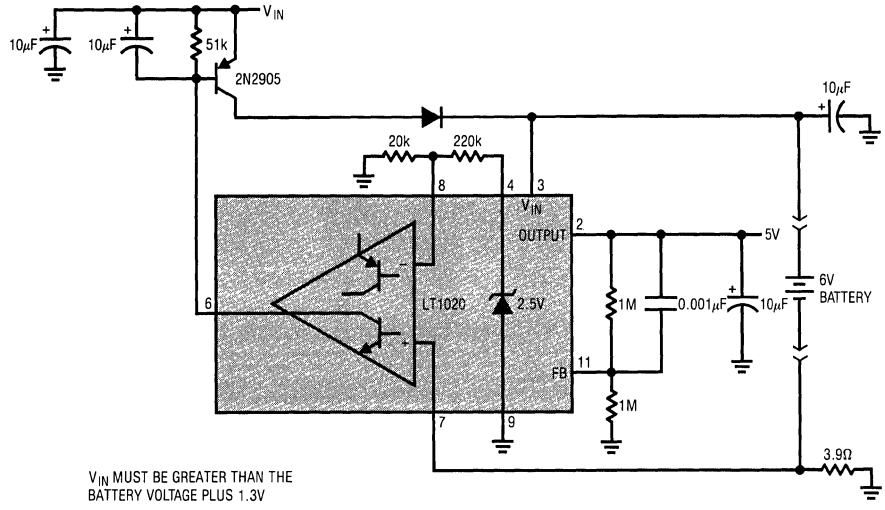
Charge-Pump Voltage Doubler



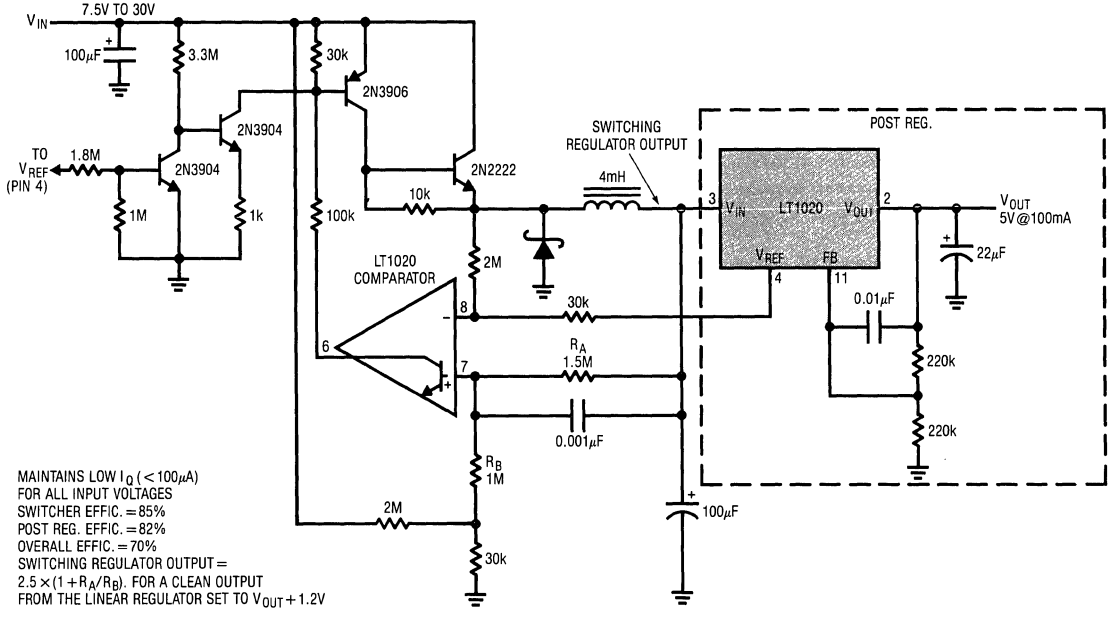
V_{OUT} (NL) ≈ 2V_{IN} − 1V
V_{OUT} (5mA) ≈ 2V_{IN} − 3V
I_Q ≈ 300μA

TYPICAL APPLICATIONS

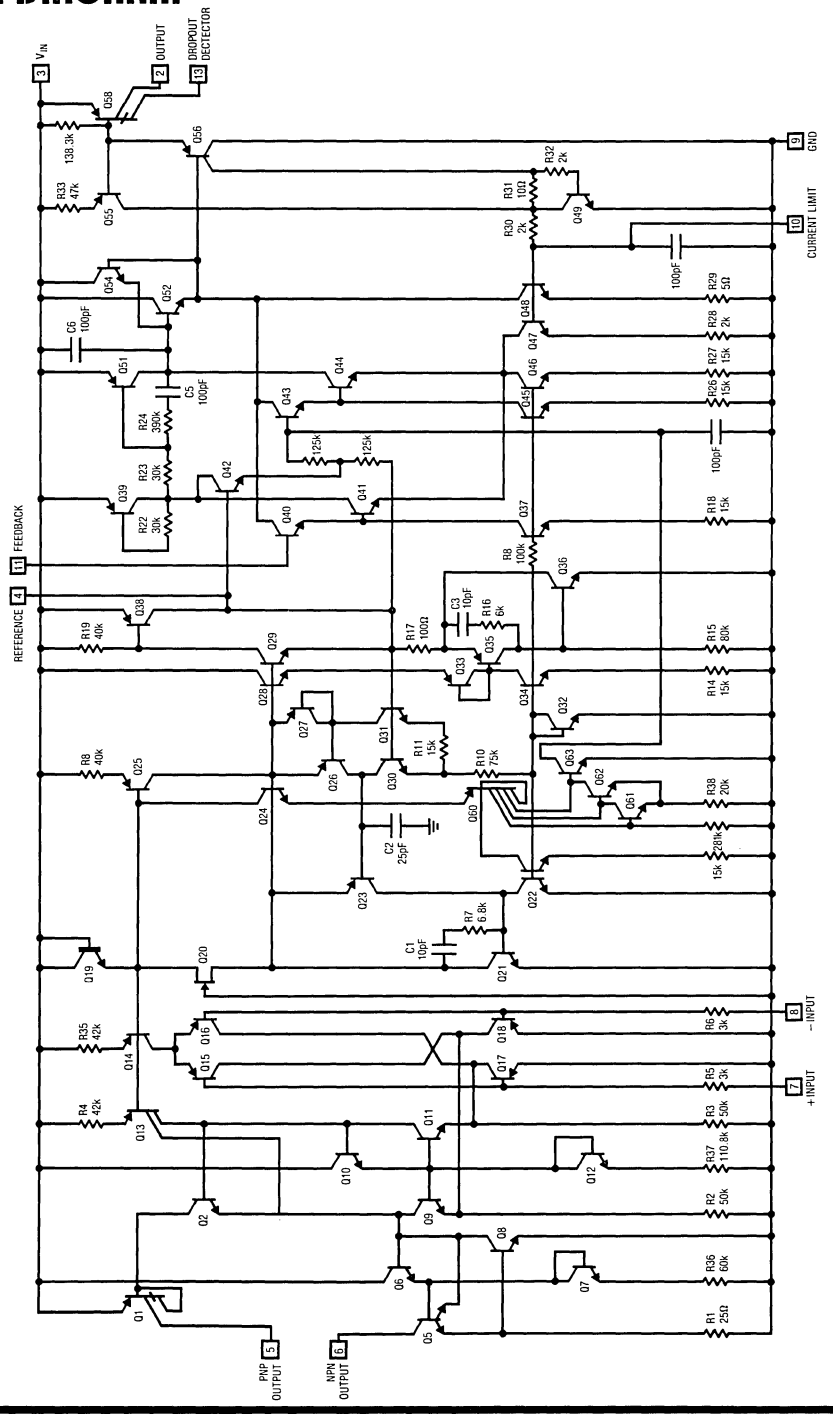
50mA Battery Charger and Regulator



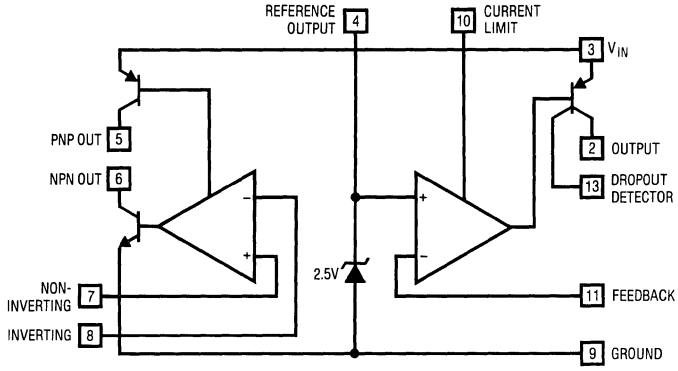
Switching Preregulator for Wide Input Voltage Range



SCHEMATIC DIAGRAM

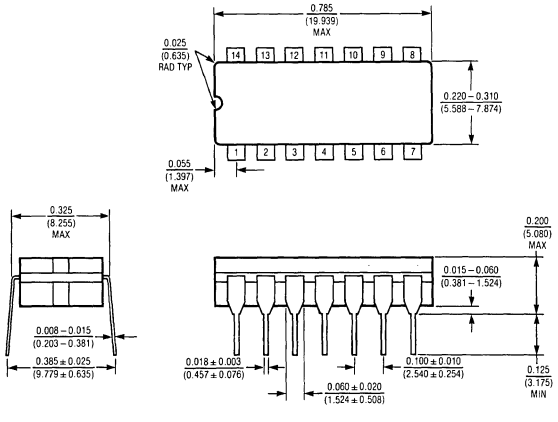


BLOCK DIAGRAM



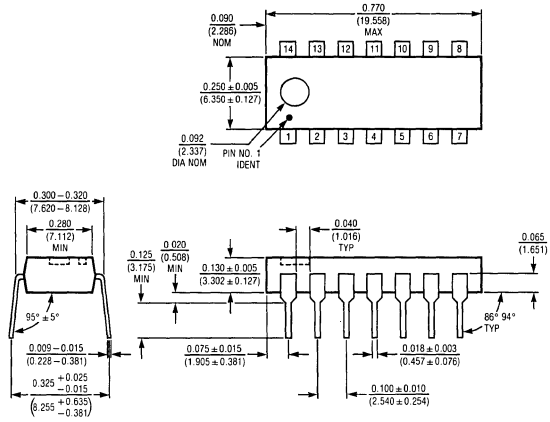
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J14 Package Hermetic DIP



T_{jmax}	Θ_{jA}
150°C	80°C/W

N14 Package Plastic DIP



T_{jmax}	Θ_{jA}
110°C	130°C/W

5A and 2.5A High Efficiency Switching Regulators

FEATURES

- Wide Input Voltage Range 3V-60V
- Low Quiescent Current—6mA
- Internal 5A Switch (2.5A for LT1071)
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages
- Can be Externally Synchronized (Consult Factory)

APPLICATIONS

- Logic Supply 5V @ 10A
- 5V Logic to ±15V Op Amp Supply
- Offline Converter up to 200W
- Battery Upconverter
- Power Inverter (+ to −) or (− to +)
- Fully Floating Multiple Outputs

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1070/LT1071. Application circuits are included to show the capability of the LT1070/LT1071. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1071 by factoring in the lower switch current rating.

DESCRIPTION

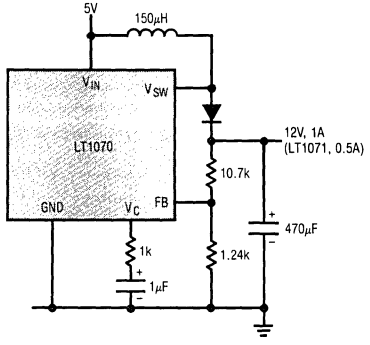
The LT1070 and LT1071 are monolithic high power switching regulators. They can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1070/LT1071 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1070/LT1071 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 100 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

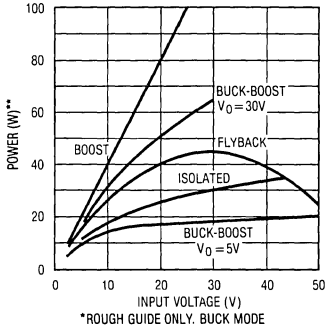
The LT1070/LT1071 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1070/LT1071, without the need for opto-couplers or extra transformer windings.

TYPICAL APPLICATION

Boost Converter (5V to 12V)



Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 5A \times V_{OUT}$. SPECIAL TOPOLOGIES DELIVER MORE POWER.

**DIVIDE VERTICAL POWER SCALE BY 2 FOR LT1071

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1070/71HV (See Note 1) 60V
- LT1070/71 (See Note 1) 40V

Switch Output Voltage
- LT1070/71HV (Note 2) 75V
- LT1070/71 ..... 65V

Feedback Pin Voltage (Transient, 1ms) ..... ± 15V

Operating Junction Temperature Range
- LT1070/71HVM, LT1070/71M ..... – 55°C to + 150°C
- LT1070/71HVC, LT1070/71C (Oper.) ..... 0°C to + 100°C
- LT1070/71HVC, LT1070/71C (Sh. Ckt.) ... 0°C to + 125°C

Storage Temperature Range ..... – 65°C to + 150°C

Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Minimum switch "on" time for the LT1070/LT1071 in current limit is ≈1.0μsec. This limits the maximum input voltage during short circuit conditions, *in the buck and inverting modes only,* to ≈35V. Normal (unshorted) conditions are not affected. Mask changes are being implemented which will reduce minimum "on" time to ≤1μsec, increasing maximum short circuit input voltage above 40V. If the present LT1070/LT1071 (contact factory for package date code) is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

The value of the resistor is given by:

$$R = \frac{t \bullet f \bullet V_{IN} - Vf}{I_{(LIMIT)}} - R_L$$

t = Minimum "on" time of LT1070/LT1071 in current limit, ≈1μs

f = Operating frequency (40kHz)

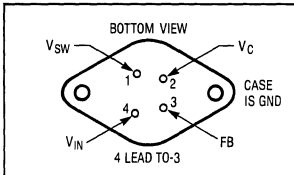
Vf = Forward voltage of external catch diode at $I_{(LIMIT)}$

$I_{(LIMIT)}$ = Current limit of LT1070 (≈8A), LT1071 (≈4A)

R_L = Internal series resistance of inductor

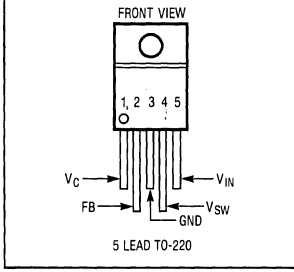
Note 2: Consult factory for availability of LT1070HV and LT1071HV units rated at 90V maximum switch voltage.

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1070/LT1071HVMK
LT1070/LT1071MK
LT1070/LT1071HVCK
LT1070/LT1071CK



LT1070/LT1071HVCT
LT1070/LT1071CT

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin	● ●	1.224 1.214	1.244 1.244	1.264 1.274	V
I_B	Feedback Input Current	V_{FB} = V_{REF}	 ●		350	750 1100	nA
gm	Error Amplifier Transconductance	ΔI_C = ± 25μA	● ●	3000 2400	4400	6000 7000	μmho
	Error Amplifier Source or Sink Current	V_C = 1.5V	● ●	150 120	200	350 400	μA μA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V Lo Clamp, V_{FB} = 1.5V		1.8 0.25	0.38	2.3 0.52	V V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.7V ≤ V_C ≤ 1.4V		500	800	2000	V/V
	Minimum Input Voltage		●		2.6	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			6	9	mA
	Control Pin Threshold	Duty Cycle = 0	 ●	0.8 0.6	0.9	1.08 1.25	V
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Flyback Reference Voltage	I_{FB} = 50μA		15	16.3	17.6	V
			●	14		18	
	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 50μA 3V ≤ V_{IN} ≤ V_{MAX}			0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	ΔI_C = ±10μA		150	300	500	μmho
	Flyback Amplifier Source and Sink Current	V_C = 1.5V Source	●	15	32	50	μA
		I_{FB} = 50μA Sink	●	25	40	70	μA
BV	Output Switch Breakdown Voltage (Note 2)	3V ≤ V_{IN} ≤ V_{MAX} LT1070/LT1071	●	65	90		V
		I_{SW} = 5mA LT1070HV/LT1071HV	●	75	90		V
V_{SAT}	Output Switch (Note 1) "On" Resistance	I_{SW} = 5A LT1070			0.15	0.24	Ω
		I_{SW} = 2.5A LT1071			0.3	0.5	Ω
	Control Voltage to Switch Current Transconductance	LT1070			8		A/V
		LT1071			4		A/V
I_{LIM}	Switch Current Limit	Duty Cycle = 50% LT1070	●	5		13	A
		Duty Cycle = 80%	●	4		10	A
		Duty Cycle = 50% LT1071	●	2.5		7	A
		Duty Cycle = 80%	●	2		6	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				25	35	mA/A
f	Switching Frequency			35	40	45	kHz
			●	33		47	
DC (max)	Maximum Switch Duty Cycle			90	92	97	%
	Flyback Sense Delay Time				1.5		μs
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ V_{MAX} V_C = 0.05V			100	250	μA
	Shutdown Mode Threshold Voltage	3V ≤ V_{IN} ≤ V_{MAX}		100	150	250	mV
			●	50		300	mV

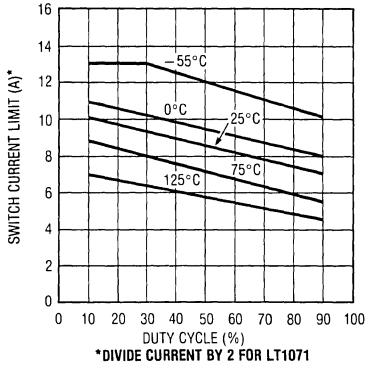
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

Note 2: Consult factory for availability of LT1070HV and LT1071HV units rated at 90V maximum switch voltage.

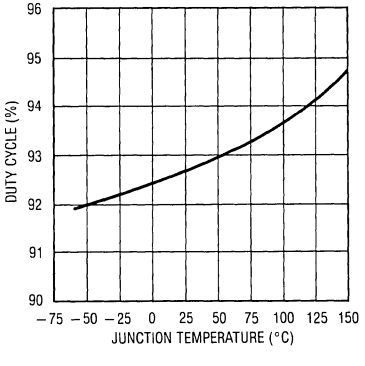
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Current Limit vs Duty Cycle

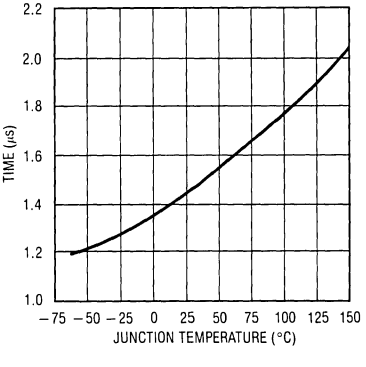


*DIVIDE CURRENT BY 2 FOR LT1071

Maximum Duty Cycle

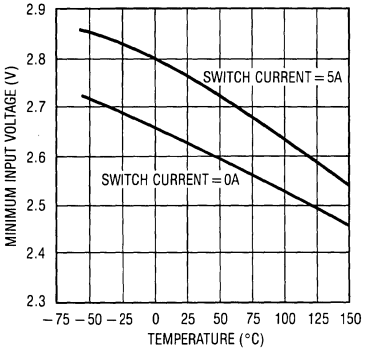


Flyback Blanking Time

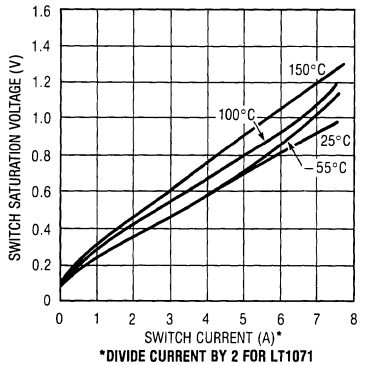


TYPICAL PERFORMANCE CHARACTERISTICS

Minimum Input Voltage

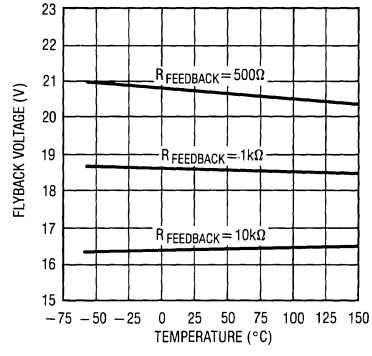


Switch Saturation Voltage

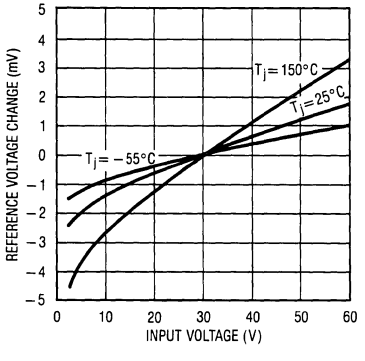


*DIVIDE CURRENT BY 2 FOR LT1071

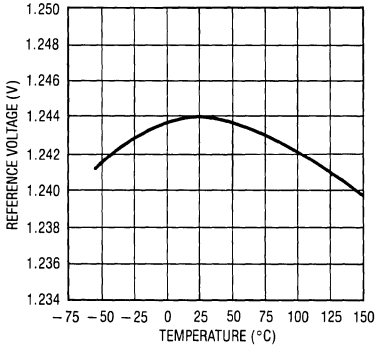
Isolated Mode Flyback Reference Voltage



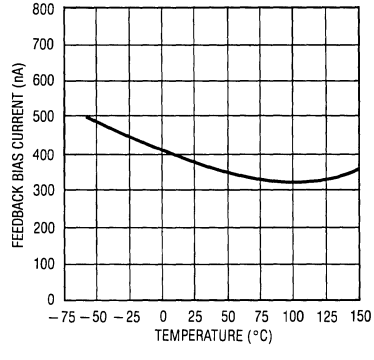
Line Regulation



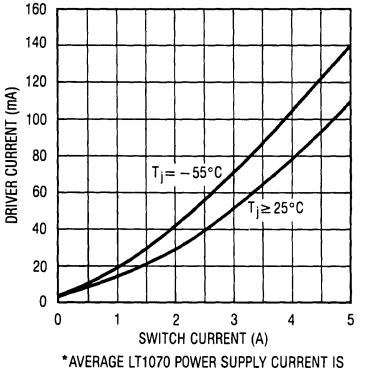
Reference Voltage vs Temperature



Feedback Bias Current vs Temperature

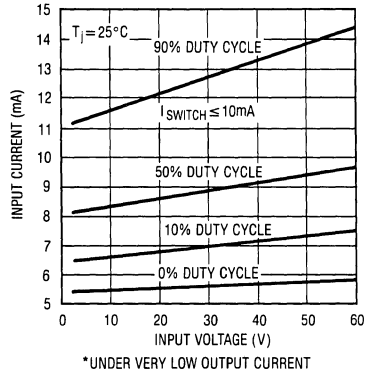


Driver Current* vs Switch Current



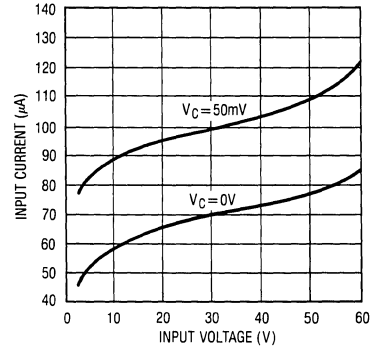
*AVERAGE LT1070 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*



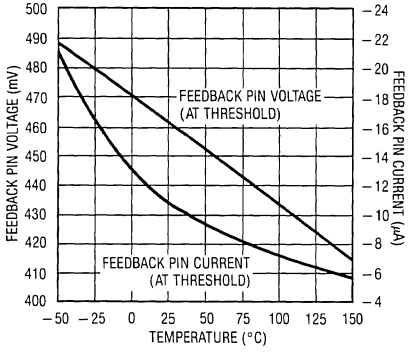
*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

Supply Current vs Input Voltage Shutdown Mode

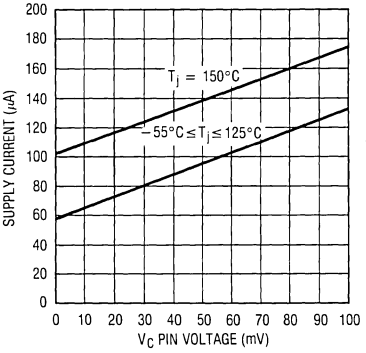


TYPICAL PERFORMANCE CHARACTERISTICS

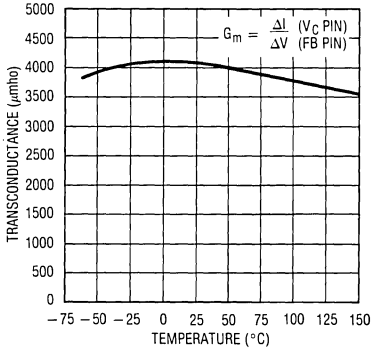
Normal/Flyback Mode Threshold on Feedback Pin



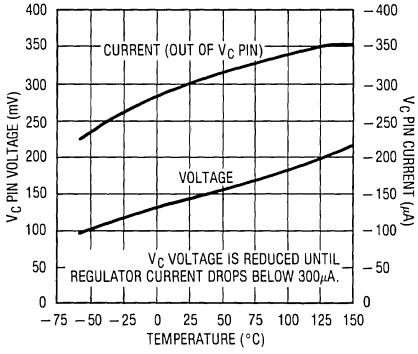
Shutdown Mode Supply Current



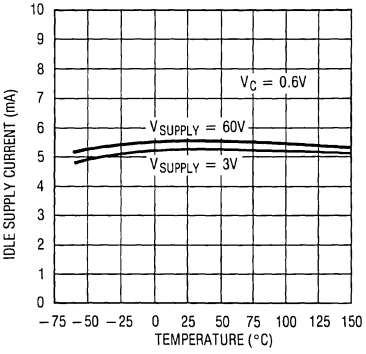
Error Amplifier Transconductance



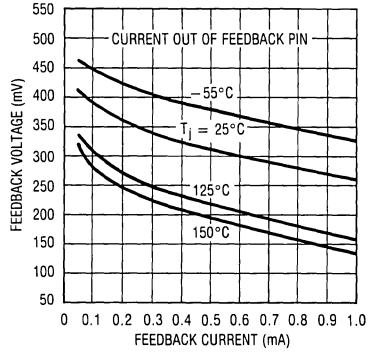
Shutdown Thresholds



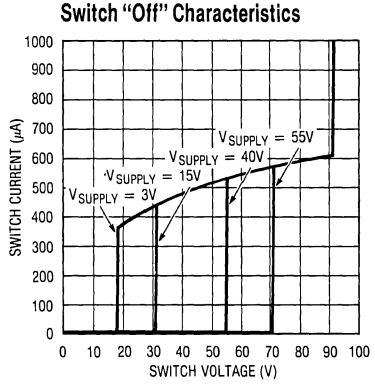
Idle Supply Current vs Temperature



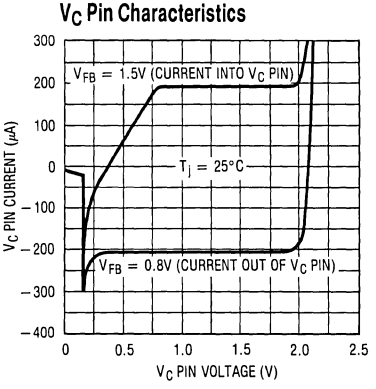
Feedback Pin Clamp Voltage



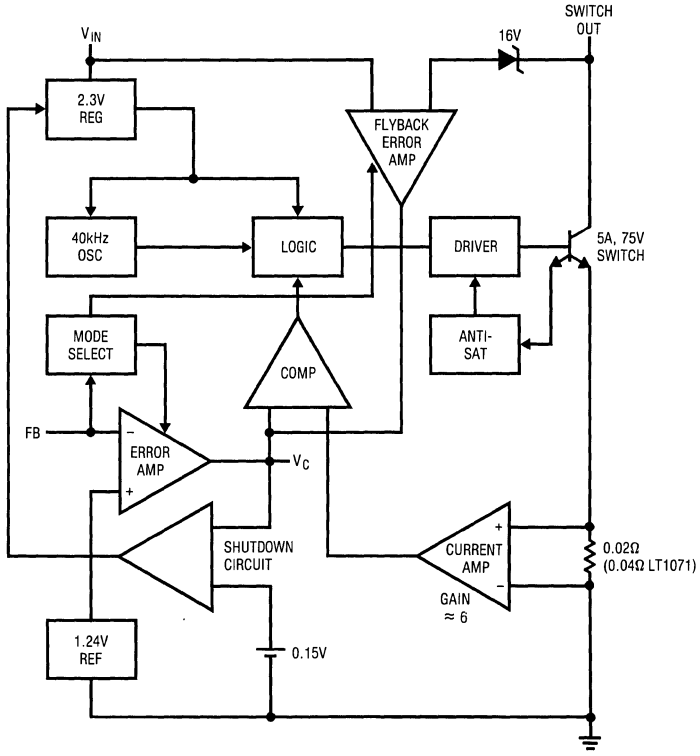
Switch "Off" Characteristics



V_C Pin Characteristics



BLOCK DIAGRAM



LT1070/LT1071 OPERATION

The LT1070/LT1071 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070/LT1071. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070/LT1071 to disconnect the main error amplifier output

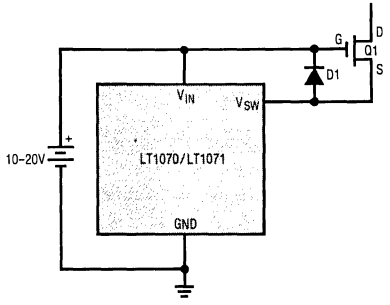
LT1070/LT1071 OPERATION

and connects the output of the flyback amplifier to the comparator input. The LT1070/LT1071 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070/LT1071 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

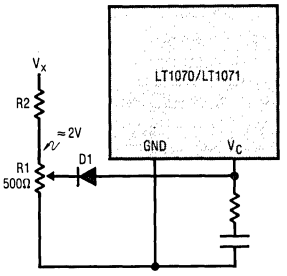
The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070/LT1071 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing. See AN-19 for full application details.

TYPICAL APPLICATIONS (Note that maximum output currents are divided by 2 for LT1071.)

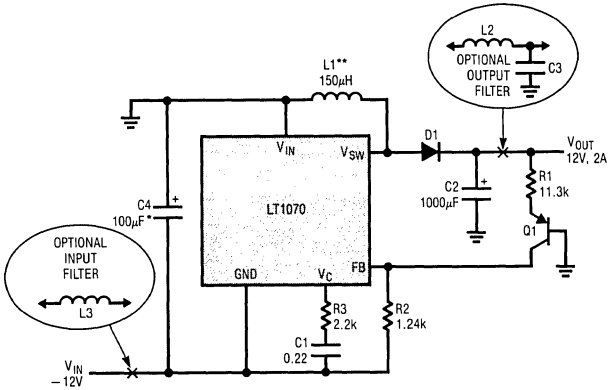
Driving High Voltage FET



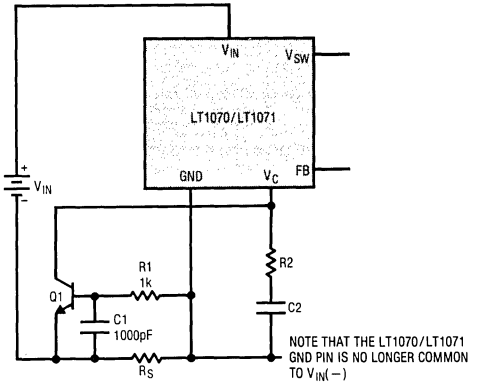
External Current Limit



Negative to Positive Buck-Boost Converter

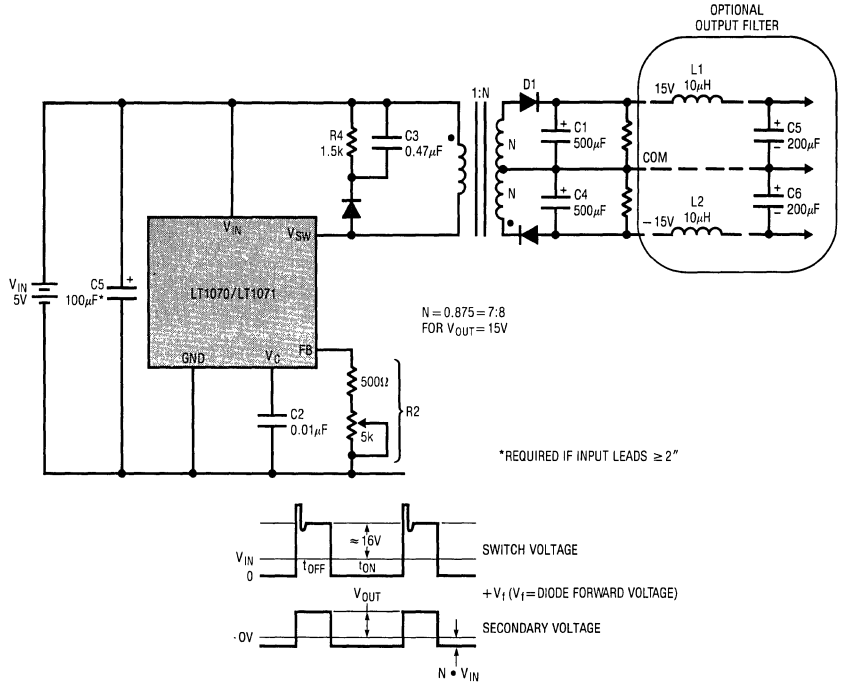


External Current Limit

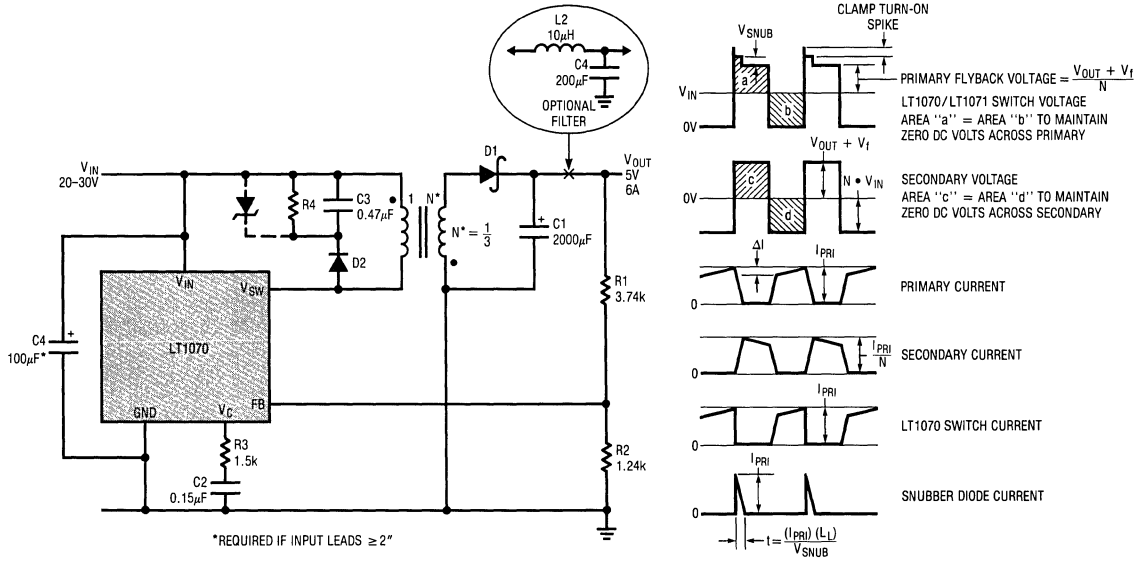


TYPICAL APPLICATIONS

Totally Isolated Converter

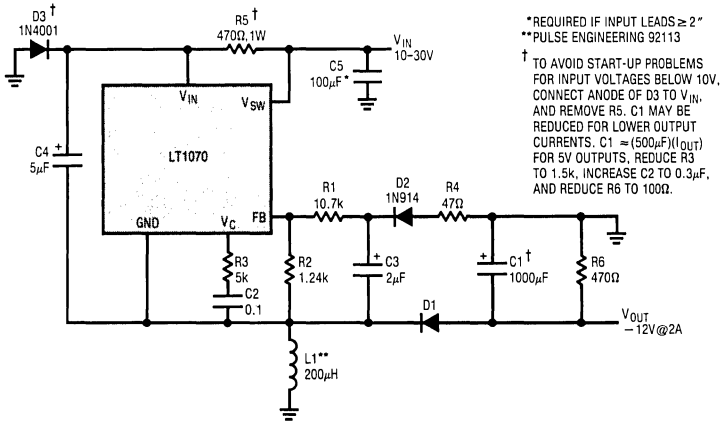


Flyback Converter

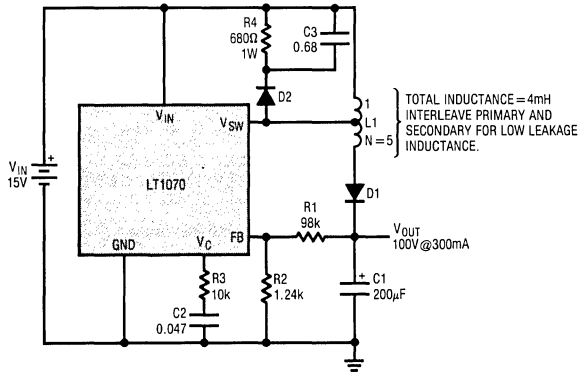


TYPICAL APPLICATIONS

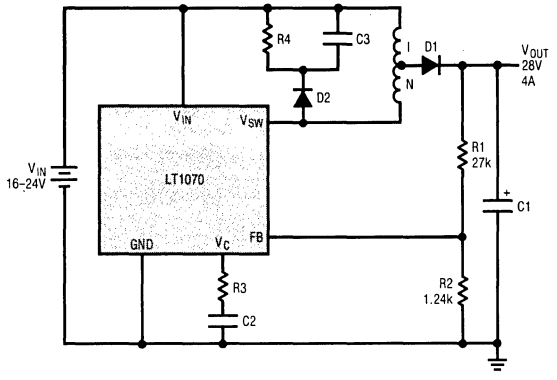
Positive to Negative Buck-Boost Converter



Voltage Boosted Boost Converter

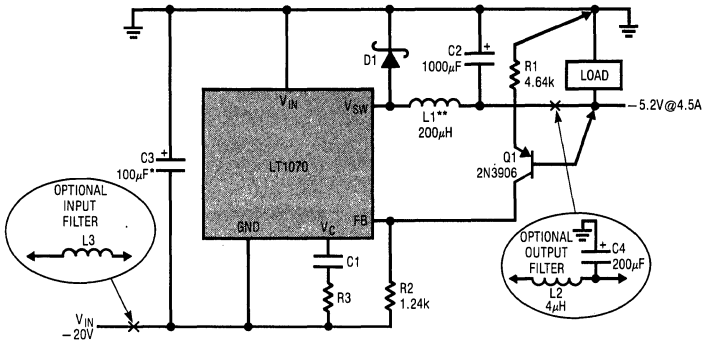


Current Boosted Boost Converter



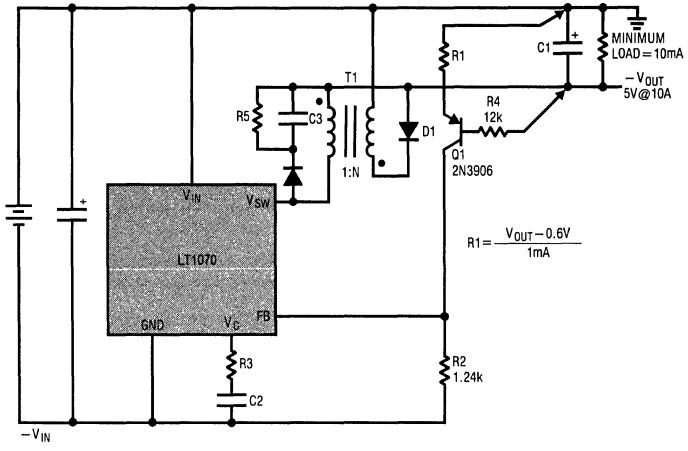
TYPICAL APPLICATIONS

Negative Buck Converter

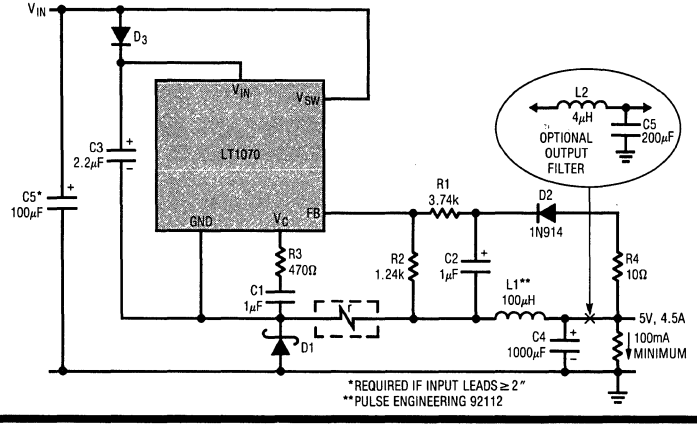


*REQUIRED IF INPUT LEADS ≥ 2″
**PULSE ENGINEERING 92113

Negative Current Boosted Buck Converter



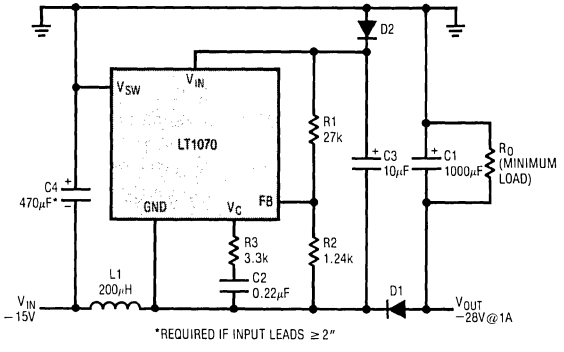
Positive Buck Converter



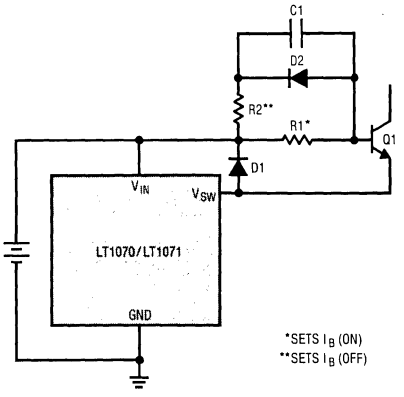
*REQUIRED IF INPUT LEADS ≥ 2″
**PULSE ENGINEERING 92112

TYPICAL APPLICATIONS

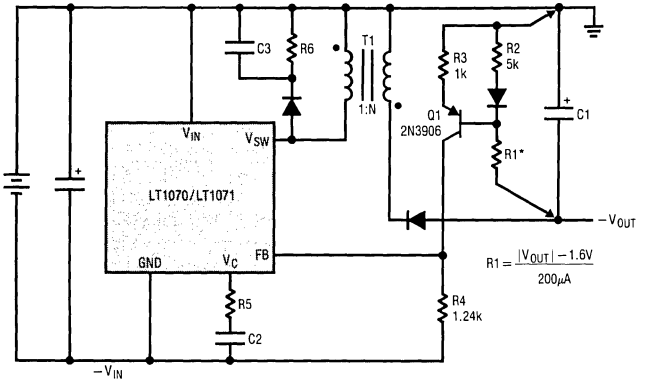
Negative Boost Regulator



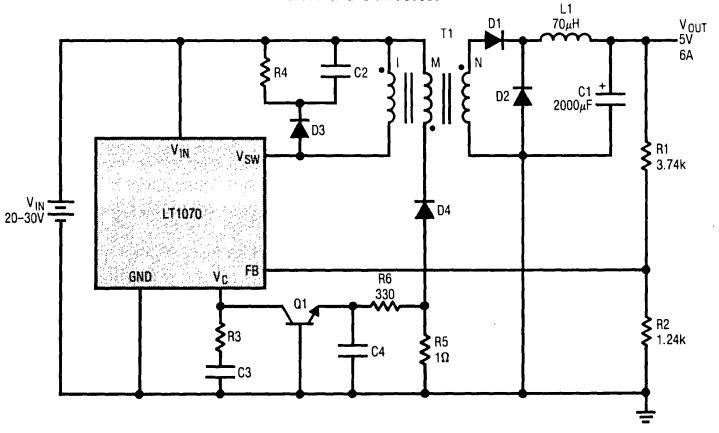
Driving High Voltage NPN



Negative Input-Negative Output Flyback Converter

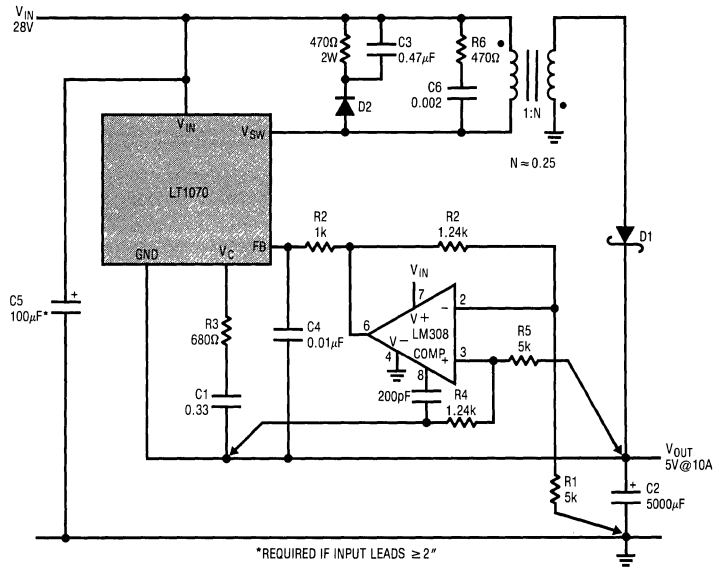


Forward Converter



TYPICAL APPLICATIONS

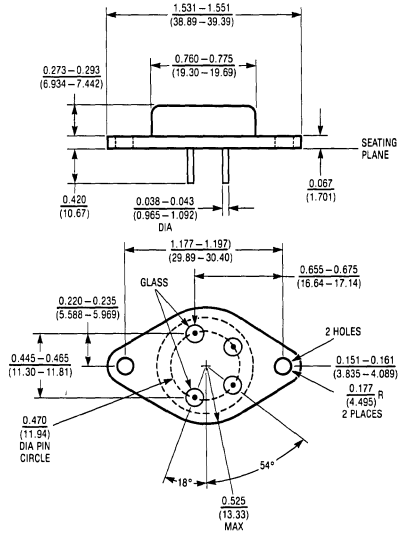
Positive Current Boosted Buck Converter



PACKAGE DESCRIPTION

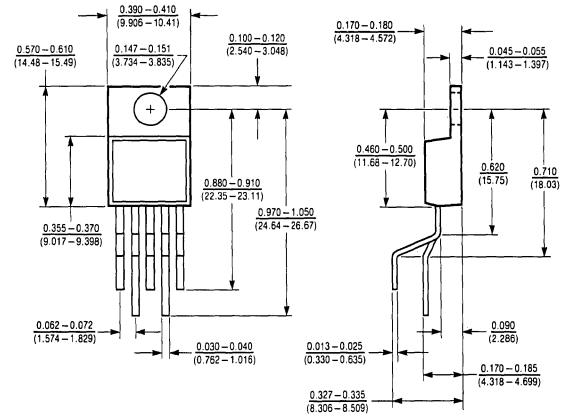
Dimensions in inches (millimeters) unless otherwise noted.

TO-3 Type Metal Can (Steel) K Package



	T_{JMAX}	θ_{JC}	θ_{JA}
LT1070MK, LT1070HVMK	150°C	2°C/W	35°C/W
LT1070CK, LT1070HVCK	100°C	2°C/W	35°C/W
LT1071MK, LT1071HVMK	150°C	4°C/W	35°C/W
LT1071CK, LT1071HVCK	100°C	4°C/W	35°C/W

TO-220 Type Plastic T Package



	T_{JMAX}	θ_{JC}	θ_{JA}
LT1070CT, LT1070HVCT	100°C	2°C/W	75°C/W
LT1071CT, LT1071HVCT	100°C	4°C/W	75°C/W

7.5A, 5A, 3A Low Dropout Positive Adjustable Regulators

FEATURES

- Three Terminal Adjustable
- Output Current of 3A, 5A or 7.5A
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.015% Line Regulation
- 0.01% Load Regulation
- 100% Thermal Limit Burn-In

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

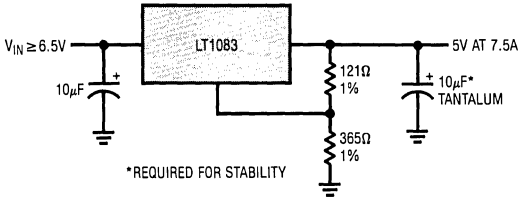
DESCRIPTION

The LT1083 series of positive adjustable regulators are designed to provide 7.5A, 5A and 3A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

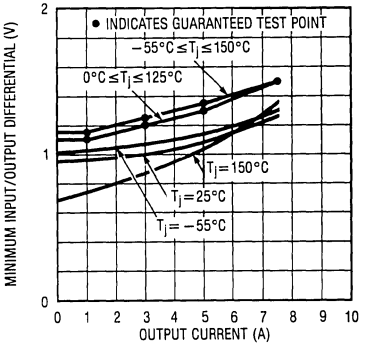
The LT1083/84/85 series devices are pin compatible with older 3 terminal regulators. A 10μF output capacitor is required on these new devices; however, this is usually included in most regulator designs.

Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1083 quiescent current flows into the load, increasing efficiency.

5V, 7.5A Regulator



LT1083 Dropout Voltage vs Output Current



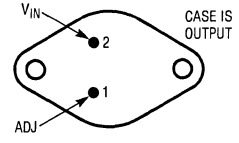
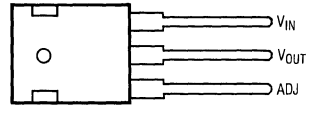
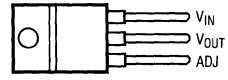
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential
"M" Grades 35V
"C" Grades 30V
Operating Junction Temperature Range
"M" Grades
Control Section ..... –55°C to 150°C
Power Transistor ..... –55°C to 200°C
"C" Grades
Control Section ..... 0°C to 125°C
Power Transistor ..... 0°C to 150°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PRECONDITIONING

100% Thermal Limit Burn-In

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  K PACKAGE TO-3 METAL CAN	LT1083MK LT1084CK LT1083CK LT1085MK LT1084MK LT1085CK
FRONT VIEW  P PACKAGE TO-247 PLASTIC	LT1083CP LT1084CP
FRONT VIEW  T PACKAGE TO-220 PLASTIC	LT1085CT

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	I_{OUT} = 10mA, T_j = 25°C, (V_{IN} – V_{OUT}) = 3V (K Package Only)		1.238	1.250	1.262	V
	10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$ 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 25V (Note 3)	●	1.225	1.250	1.270	V
Line Regulation	I_{LOAD} = 10mA, 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 15V, T_j = 25°C			0.015	0.2	%
		●		0.035	0.2	%
	M Grade 15V ≤ (V_{IN} – V_{OUT}) ≤ 35V	●		0.05	0.5	%
	C Grade 15V ≤ (V_{IN} – V_{OUT}) ≤ 30V (Notes 1, 2)	●		0.05	0.5	%
Load Regulation	(V_{IN} – V_{OUT}) = 3V 10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$ T_j = 25°C (Notes 1, 2, 3)			0.1	0.3	%
		●		0.2	0.4	%
Dropout Voltage	ΔV_{REF} = 1%, I_{OUT} = $I_{FULL\ LOAD}$, (Note 4)	●		1.3	1.5	V
Current Limit						
LT1083	(V_{IN} – V_{OUT}) = 5V	●	8.0	9.5		A
	(V_{IN} – V_{OUT}) = 25V	●	0.4	1.0		A
LT1084	(V_{IN} – V_{OUT}) = 5V	●	5.5	6.5		A
	(V_{IN} – V_{OUT}) = 25V	●	0.3	0.6		A
LT1085	(V_{IN} – V_{OUT}) = 5V	●	3.2	4		A
	(V_{IN} – V_{OUT}) = 25V	●	0.2	0.5		A

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Load Current	$(V_{IN} - V_{OUT}) = 25V$	●		5	10	mA
Thermal Regulation	$T_A = 25°C$, 30ms pulse					
LT1083				0.002	0.01	%/W
LT1084				0.003	0.15	%/W
LT1085				0.004	0.02	%/W
Ripple Rejection	f = 120Hz $C_{ADJ} = 25\mu F$, $C_{OUT} = 25\mu F$ Tantalum $I_{OUT} = I_{FULL\ LOAD}$, $(V_{IN} - V_{OUT}) = 3V$	●	60	75		dB
Adjust Pin Current	$T_j = 25°C$			55		μA
		●			120	μA
Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{FULL\ LOAD}$ $1.5V \le (V_{IN} - V_{OUT}) \le 25V$	●		0.2	5	μA
Temperature Stability		●		0.5		%
Long Term Stability	$T_A = 125°C$, 1000 Hrs.			0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$ $10Hz = \le f \le 10kHz$			0.003		%
Thermal Resistance Junction to Case						
LT1083	K Package: Control Circuitry/Power Transistor				0.6/1.6	°C/W
	P Package: Control Circuitry/Power Transistor				0.5/1.6	°C/W
LT1084	K Package: Control Circuitry/Power Transistor				0.75/2.3	°C/W
	P Package: Control Circuitry/Power Transistor				0.65/2.3	°C/W
LT1085	K Package: Control Circuitry/Power Transistor				0.9/3.0	°C/W
	T Package: Control Circuitry/Power Transistor				0.7/3.0	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

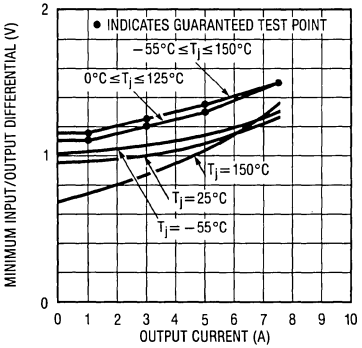
Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (60W for the LT1083, 45W for the LT1084, 30W for the LT1085). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range.

Note 3: $I_{FULL\ LOAD}$ is defined in the current limit curves. $I_{FULL\ LOAD}$ curve is defined as the minimum value of current limit as a function of input to output voltage. Note that the 60W power dissipation for the LT1083 (45W for the LT1084 or 30W for the LT1085) is only achievable over a limited range of input to output voltage.

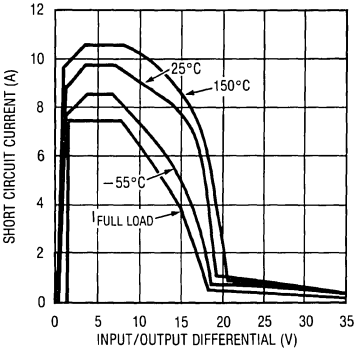
Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

TYPICAL PERFORMANCE CHARACTERISTICS

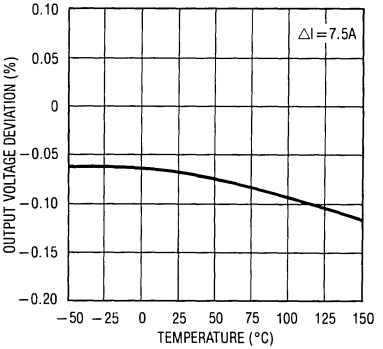
LT1083 Dropout Voltage



LT1083 Short Circuit Current

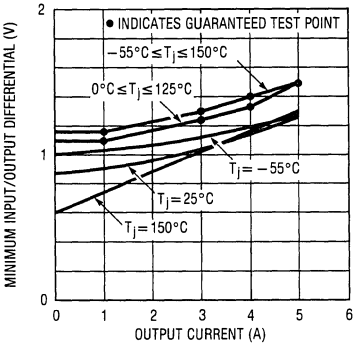


LT1083 Load Regulation

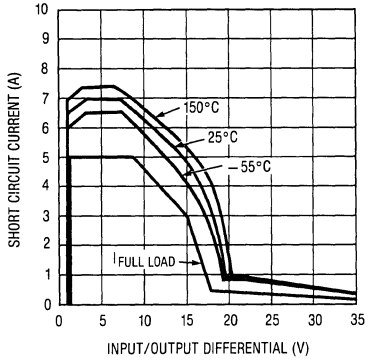


TYPICAL PERFORMANCE CHARACTERISTICS

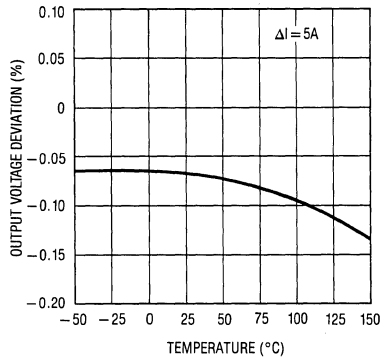
LT1084 Dropout Voltage



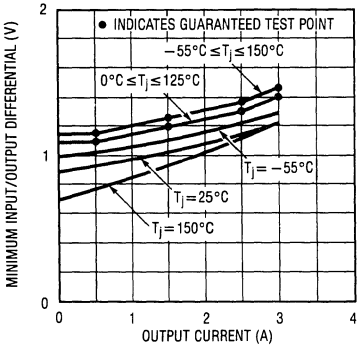
LT1084 Short Circuit Current



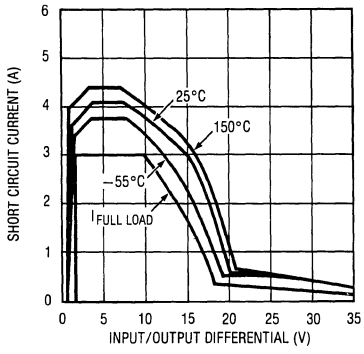
LT1084 Load Regulation



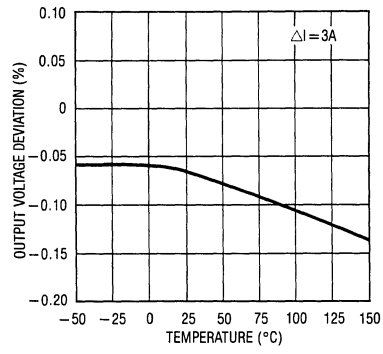
LT1085 Dropout Voltage



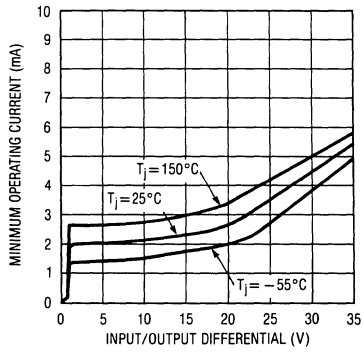
LT1085 Short Circuit Current



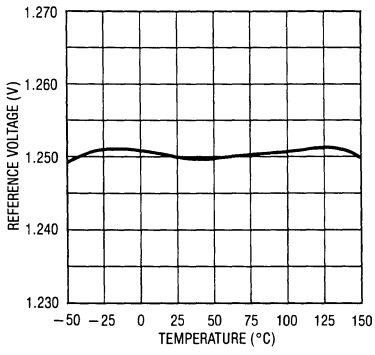
LT1085 Load Regulation



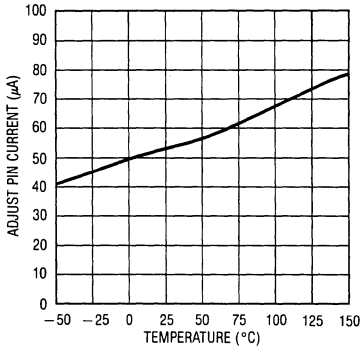
Minimum Operating Current



Temperature Stability

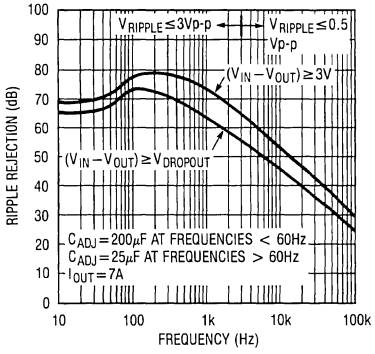


Adjust Pin Current

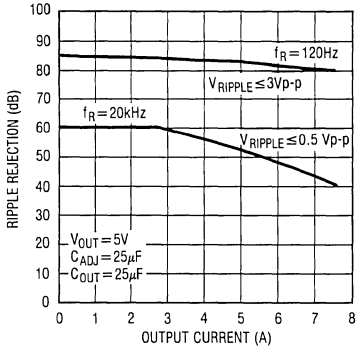


TYPICAL PERFORMANCE CHARACTERISTICS

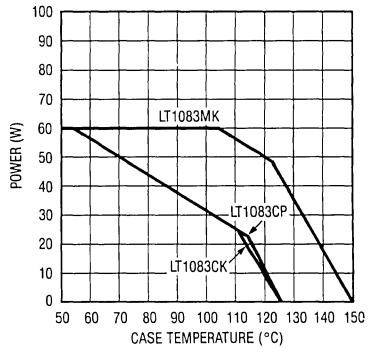
LT1083 Ripple Rejection



LT1083 Ripple Rejection vs Current

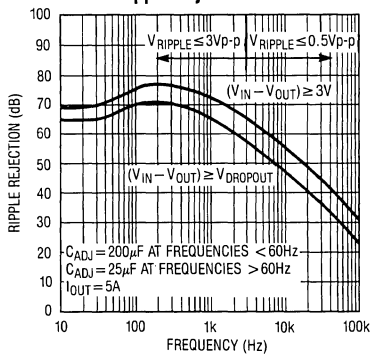


LT1083 Maximum Power Dissipation*

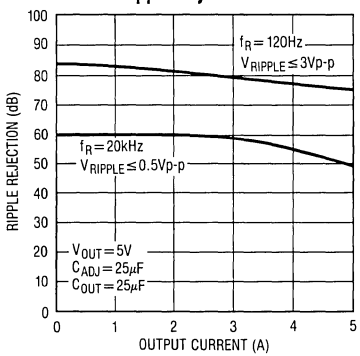


* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

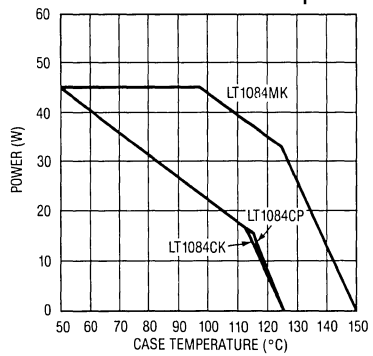
LT1084 Ripple Rejection



LT1084 Ripple Rejection vs Current

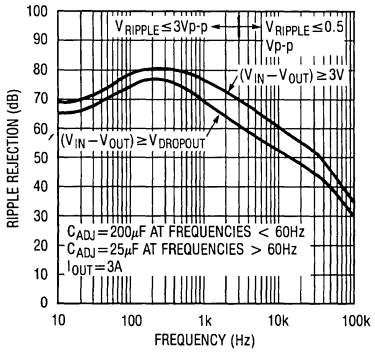


LT1084 Maximum Power Dissipation *

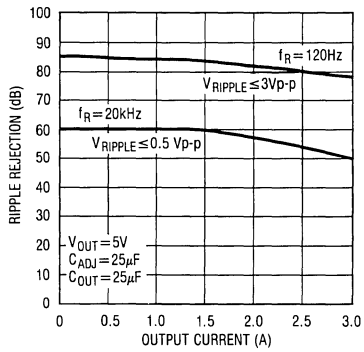


*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

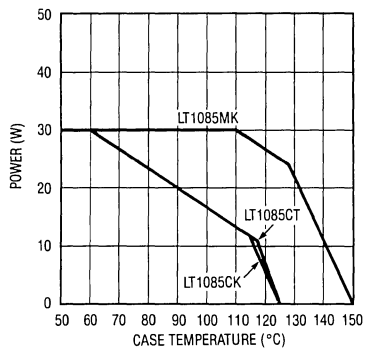
LT1085 Ripple Rejection



LT1085 Ripple Rejection vs Current



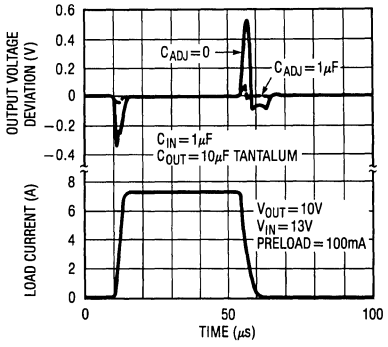
LT1085 Maximum Power Dissipation*



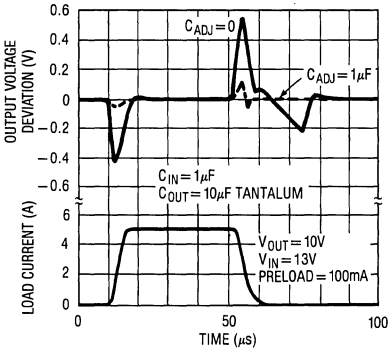
*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS

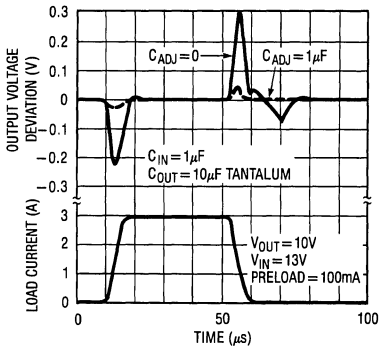
LT1083 Load Transient Response



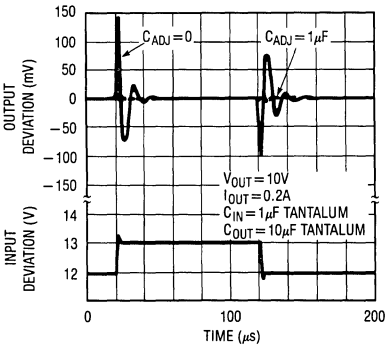
LT1084 Load Transient Response



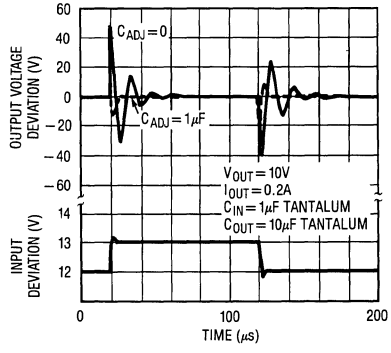
LT1085 Load Transient Response



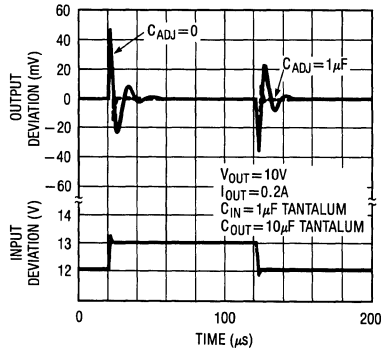
LT1083 Line Transient Response



LT1084 Line Transient Response



LT1085 Line Transient Response



APPLICATION HINTS

The LT1083 family of three terminal adjustable regulators is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short circuit protected, have safe area protection as well as thermal shutdown to turn off the regulator should the temperature exceed about 165°C.

These regulators are pin compatible with older three terminal adjustable devices, offer lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1083 family and older regulators is that they require an output capacitor for stability.

Stability

The circuit design used in the LT1083 family requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150μF aluminum electrolytic or a 22μF solid tantalum on the output will ensure stability. Normally, capacitors much smaller than this can be used with the LT1083. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, and capacitance temperature coefficient. The 150μF or 22μF values given will ensure stability.

APPLICATION HINTS

When the adjustment terminal is bypassed to improve the ripple rejection, the requirement for an output capacitor increases. The values of 22μF tantalum or 150μF aluminum cover all cases of bypassing the adjustment terminal. Without bypassing the adjustment terminal, smaller capacitors can be used with equally good results and the table below shows approximately what size capacitors are needed to ensure stability.

Recommended Capacitor Values

Input	Output	Adjustment
10μF	10μF Tantalum, 50μF Aluminum	None
10μF	22μF Tantalum, 150μF Aluminum	20μF

Normally, capacitor values on the order of 100μF are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitor further improve stability and transient response of the LT1083 regulators.

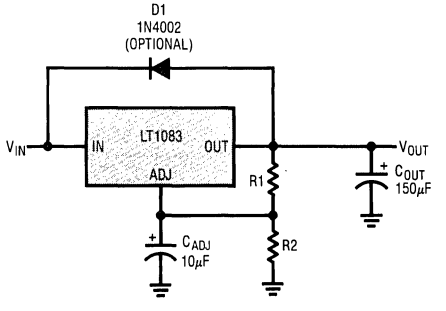
Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because, in current limit, the safe area protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negative resistance since increasing voltage causes current to decrease. Negative resistance during current limit is not unique to the LT1083 series and has been present on all power IC regulators. The value of the negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however it does not cause any problems with the IC regulator and can usually be ignored.

Protection Diodes

In normal operation, the LT1083 family does not need any protection diodes. Older adjustable regulators required protection diodes between the adjustment pin and the output and from the output to the input to prevent overstressing the die. The internal current paths on the LT1083 adjustment pin are limited by internal resistors. Therefore, even with capacitors on the adjustment pin, no protection diode is needed to ensure device safety under short circuit conditions.

Diodes between input and output are usually not needed. The internal diode between the input and the output pins of the LT1083 family can handle microsecond surge currents of 50A to 100A. Even with large output capacitances, it is very difficult to get those values of surge currents in normal operations. Only with high value of output capacitors, such as 1000μF to 5000μF and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1083 can generate those kinds of currents, and a diode from output to input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate current large enough to do any damage.

The adjustment pin can be driven on a transient basis ±25V, with respect to the output without any device degradation. Of course, as with any IC regulator, exceeding the maximum input to output voltage differential causes the internal transistors to break down and none of the protection circuitry is functional.



Overload Recovery

Like any of the IC power regulators, the LT1083 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and

APPLICATION HINTS

keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1083 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small, allowing the regulator to supply large output currents. With high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators, such as the 7800 series, also exhibited this phenomenon, so it is not unique to the LT1083.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after a removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the power supply may need to be cycled down to zero and brought up again to make the output recover.

Ripple Rejection

The typical curves for ripple rejection reflect values for a bypassed adjustment pin. This curve will be true for all values of output voltage. For proper bypassing, and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor, at the ripple frequency should equal the value of R1, (normally 100Ω-120Ω). The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz the adjust pin capacitor should be 13μF if R1 = 100Ω. At 10kHz only 0.16μF is needed.

For circuits without an adjust pin bypass capacitor, the ripple rejection will be a function of output voltage. The output ripple will increase directly as a ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V, and no adjust pin capacitor, the output ripple will be higher by the ratio of 5V/1.25V or 4 times larger. Ripple rejection will be degraded by 12dB from the value shown on the typical curve.

Output Voltage

The LT1083 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

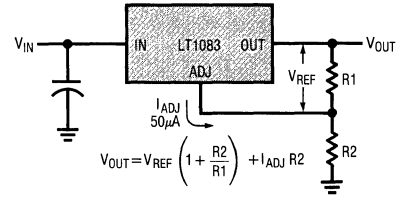


Figure 1. Basic Adjustable Regulator

Load Regulation

Because the LT1083 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negatived side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected *directly* to the case *not to the load.* This is illustrated in Figure 2. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R2 + R1}{R1}\right), \; R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.

APPLICATION HINTS

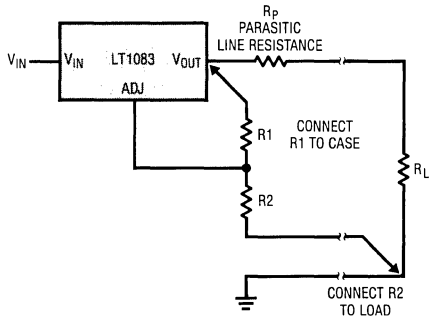


Figure 2. Connections for Best Load Regulation

Thermal Considerations

The LT1083 series of regulators have internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction to case, case to heat sink interface, and heat sink resistance itself. New thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Transistor*. Previous regulators, with a single junction to case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case-to-heat-sink interface is strongly recommended. If the case of the device must be electrically isolated, a thermally conductive spacer can be used, as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

For example, using a LT1083CK (TO-3, Commercial) and assuming:

V_{IN} (max continuous) = 9V, V_{OUT} = 5V, I_{OUT} = 6A,
$T_{AMBIENT}$ = 75°C, $\theta_{HEAT\ SINK}$ = 1°C/W,
$\theta_{CASE\text{-}TO\text{-}HEAT\text{-}SINK}$ = 0.2°C/W for K package with thermal compound.

Power dissipation under these conditions is equal to:

$$P_D = (V_{IN} - V_{OUT})(I_{OUT}) = 24W$$

Junction temperature will be equal to:

$$T_j = T_{AMBIENT} + P_D(\theta_{HEAT\text{-}SINK} + \theta_{CASE\text{-}TO\text{-}HEAT\text{-}SINK} + \theta_{jc})$$

For the Control Section:

$T_j = 75°C + 24W(1°C/W + 0.2°C/W + 0.6°C/W) = 118°C$
$118°C < 125°C = T_{jmax}$ (Control Section Commercial Range)

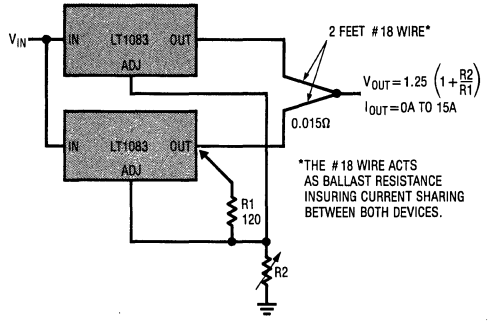
For the Power Transistor:

$T_j = 75°C + 24W(1°C/W + 0.2°C/W + 1.6°C/W) = 142°C$
$142°C < 150°C = T_{jmax}$ (Power Transistor Commercial Range)

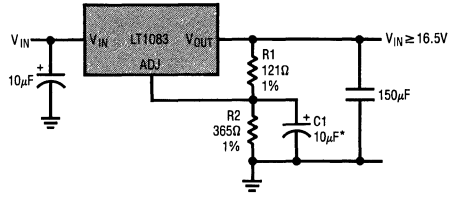
In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

TYPICAL APPLICATIONS

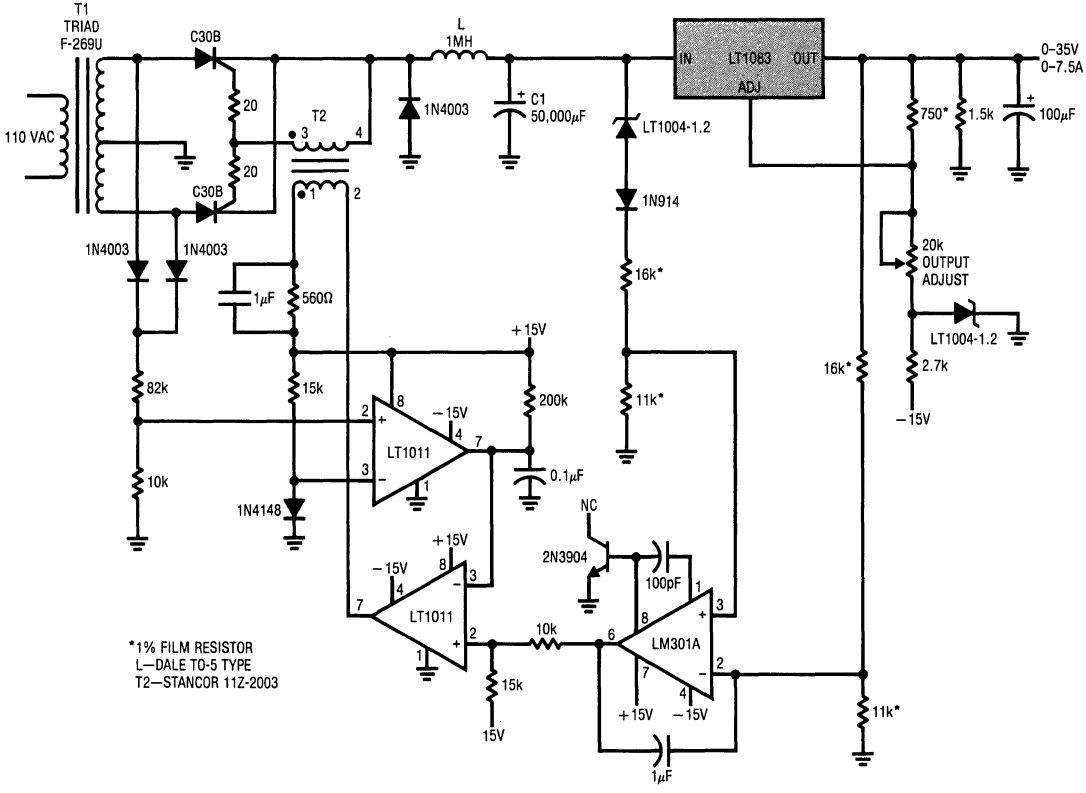
Paralleling Regulators



Improving Ripple Rejection



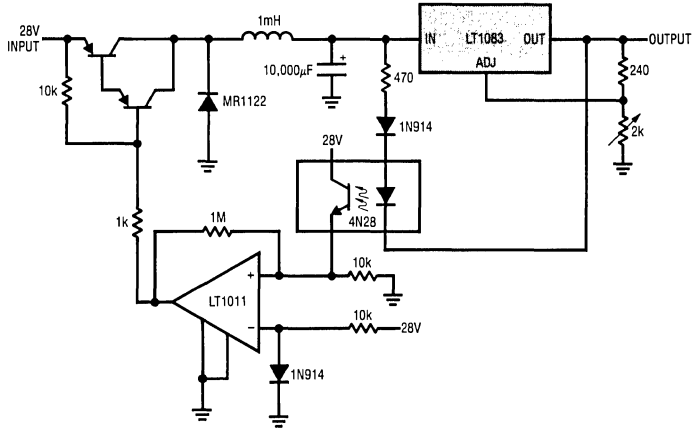
7.5A Variable Regulator



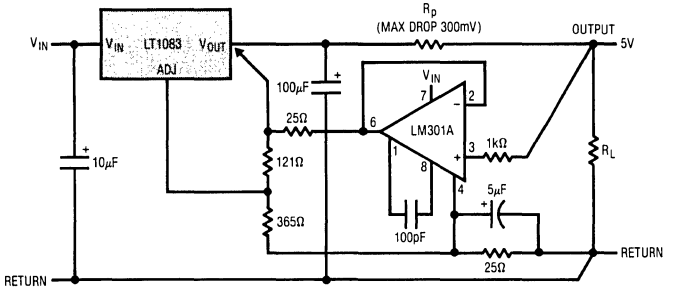
GENERAL PURPOSE REGULATOR WITH SCR PREREGULATOR TO LOWER POWER DISSIPATION. ABOUT 1.7V DIFFERENTIAL IS MAINTAINED ACROSS THE LT1083 INDEPENDENT OF OUTPUT VOLTAGE AND LOAD CURRENT.

TYPICAL APPLICATIONS

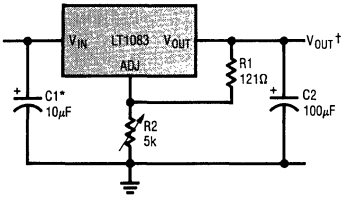
High Efficiency Regulator



Remote Sensing



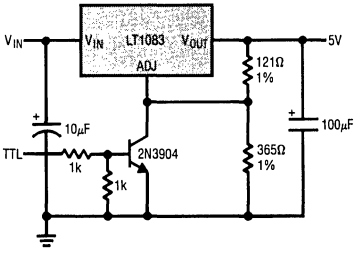
1.2V–15V Adjustable Regulator



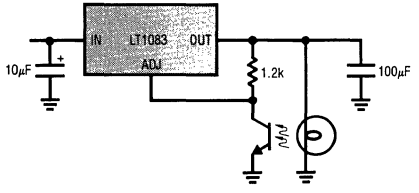
*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

†$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$

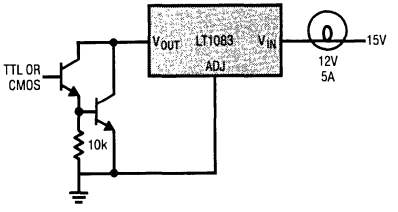
5V Regulator with Shutdown



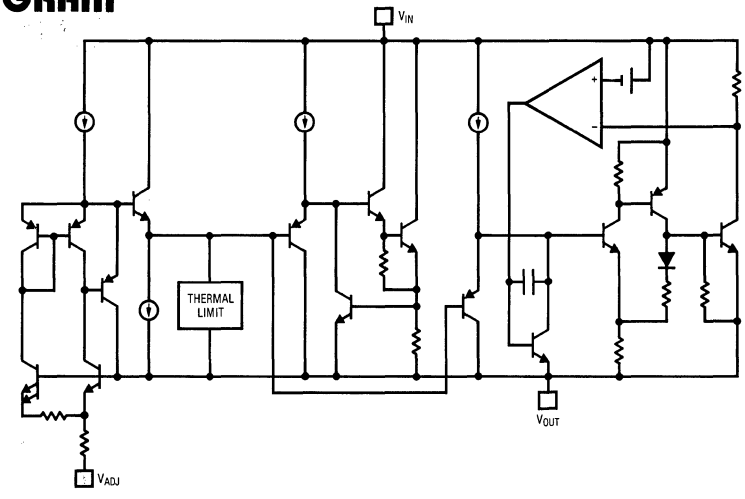
Automatic Light Control



Protected High Current Lamp Driver

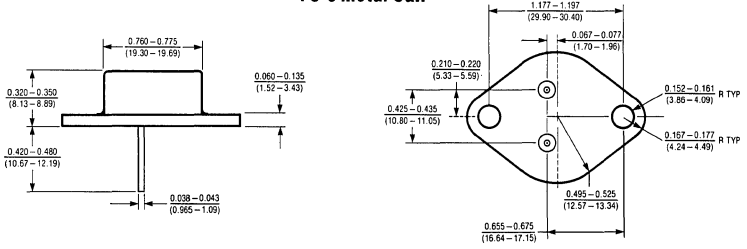


BLOCK DIAGRAM

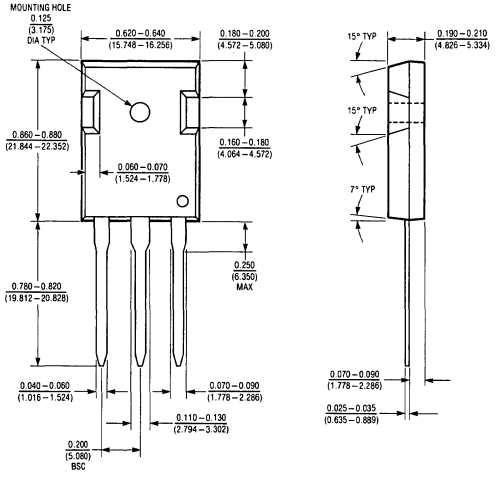


PACKAGE DESCRIPTIONS Dimensions in inches (millimeters) unless otherwise noted.

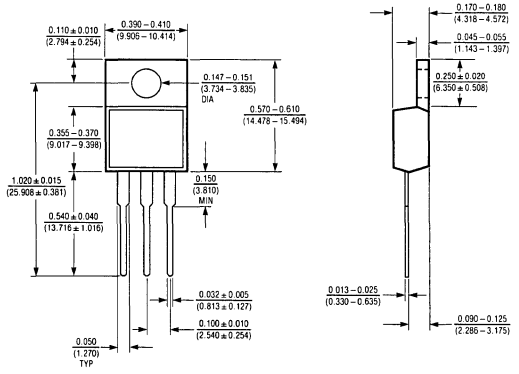
K Package
TO-3 Metal Can



P Package
TO-247 Plastic



T Package
TO-220 Plastic



SECTION 4—VOLTAGE REFERENCES

SECTION 4—VOLTAGE REFERENCES

MILITARY TEMPERATURE RANGE

–55°C to +125°C

VOLTAGE V_Z (VOLTS)	VOLTAGE TOLERANCE MAXIMUM T_A = 25°C	DEVICE	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	MAXIMUM DYNAMIC IMPEDANCE (Ω)	MAJOR FEATURE
1.235	±0.32%	LT1004M-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±1%	LM185-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±1%	LT1034BM-1.2	20ppm (max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±1%	LT1034M-1.2	40ppm (max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
2.5	±0.5%	LT1004M-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±0.2%	LT1009M	18mV (max)	400μA to 10mA	1.0	Precision
	±0.2%	LT1019M-2.5	25ppm (max)	1.2mA	N/A	Precision Bandgap
	±2%	LM136-2.5	18mV (max)	400μA to 10mA	1.0	General Purpose
	±1%	LM136A-2.5	18mV (max)	400μA to 10mA	1.0	General Purpose
	±1.5%	LM185-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±1%	AD580S	55ppm (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580T	25ppm (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580U	10ppm (max)	1.5mA	N/A	3 Terminal Low Drift
5.0	±0.2%	LT1019M-5	25ppm (max)	1.2mA	N/A	Precision Bandgap
	±1%	LT1021BM-5	5ppm (max)	1.2mA	0.1	Very Low Drift
	±0.05%	LT1021CM-5	20ppm (max)	1.2mA	0.1	Very Tight Inital Tolerance
	±1	LT1021DM-5	20ppm (max)	1.2mA	0.1	Low Cost, High Performance
	±0.2%	LT1029AM	20ppm (max)	600μA to 10mA	0.6	Precision Bandgap
	±1%	LT1029M	40ppm (max)	600μA to 10mA	0.6	Precision Bandgap
	±0.3%	REF02A	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
	±0.5%	REF02	25ppm (max)	1.4mA	N/A	Precision Bandgap
6.9	±3%	LM129A	10ppm (max)	600μA to 15mA	0.8 (typ)	Low Drift
	±3%	LM129B	20ppm (max)	600μA to 15mA	0.8 (typ)	Low Drift
	±3%	LM129C	50ppm (max)	600μA to 15mA	0.8 (typ)	Low Cost
6.95	±2%	LM199A	0.5ppm (max) – 55°C to +85°C 10ppm (max) + 85°C to +125°C	500μA to 10mA	1.0	Ultra Low Drift
	±2%	LM199	1ppm (max) – 55°C to +85°C 15ppm (max) + 85°C to +125°C	500μA to 10mA	1.0	Ultra Low Drift
7.0	±0.7%	LT1021BM-7	5ppm (max)	1.0mA	0.2	Low Drift/Noise, Exc. Stability
	±0.7%	LT1021DM-7	20ppm (max)	1.0mA	0.2	Low Cost, High Performance
10.0	±0.2%	LT1019M-10	25ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.5%	LT1021BM-10	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.05%	LT1021CM-10	20ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.5%	LT021DM-10	20ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.05%	LT1031BM	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.1%	LT1031CM	15ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.2%	LT1031DM	25ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.3%	AD581J	30ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.1%	AD581T	15ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.05%	LH0070-2	6.7ppm (max)	5.0mA	0.6	Low Drift
	±0.1%	LH0070-1	17ppm (max)	5.0mA	0.6	Good Initial Tolerance
	±0.1%	LH0070-0	33ppm (max)	5.0mA	0.6	Low Cost, High Performance
	±0.3%	REF01A	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
	±0.5%	REF01	25ppm (max)	1.4mA	N/A	Precision Bandgap

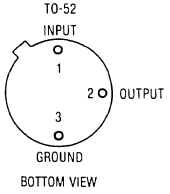
COMMERCIAL TEMPERATURE RANGE

0°C to +70°C

VOLTAGE V_Z (VOLTS)	VOLTAGE TOLERANCE MAXIMUM T_A = 25°C	DEVICE	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	MAXIMUM DYNAMIC IMPEDANCE (Ω)	MAJOR FEATURE
1.235	±0.32%	LT1004C-1.2	20ppm (typ)	10μA to 20mA	1.5	Micropower
	±1%	LT1034BC-1.2	20ppm (max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±1%	LT1034C-1.2	40ppm (max)	20μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	±2%	LM385-1.2	20ppm (typ)	15μA to 20mA	1.5	Micropower
	±1%	LM385B-1.2	20ppm (typ)	15μA to 20mA	1.5	Micropower
2.5	±0.5%	LT1004C-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±0.2%	LT1009C	6mV (max)	400μA to 10mA	1.4	Precision
	±0.2%	LT1019C-2.5	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±4%	LM336-2.5	6mV (max)	400μA to 10mA	1.4	General Purpose
	±2%	LM336B-2.5	6mV (max)	400μA to 10mA	1.4	General Purpose
	±3%	LM385-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±1.5%	LM385B-2.5	20ppm (typ)	20μA to 20mA	1.5	Micropower
	±3%	AD580J	85 (max)	1.5mA	N/A	3 Terminal Low Drift
	±1%	AD580K	40 (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580L	25 (max)	1.5mA	N/A	3 Terminal Low Drift
	±0.4%	AD580M	10 (max)	1.5mA	N/A	3 Terminal Low Drift
5.0	±0.2%	LT1019C-5	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±1%	LT1021BC-5	5ppm (max)	1.2mA	0.1	Very Low Drift
	±0.05%	LT1021CC-5	20ppm (max)	1.2mA	0.1	Very Tight Inital Tolerance
	±1	LT1021DC-5	20ppm (max)	1.2mA	0.1	Low Cost, High Performance
	±0.2%	LT1029AC	20ppm (max)	600μA to 10mA	0.6	Precision Bandgap
	±1%	LT1029C	34ppm (max)	600μA to 10mA	0.6	Precision Bandgap
	±0.3%	REF02E	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
	±0.5%	REF02H	25ppm (max)	1.4mA	N/A	Precision Bandgap
	±1%	REF02C	65ppm (max)	1.6mA	N/A	Precision Bandgap
	±2%	REF02D	250ppm (max)	2.0mA	N/A	Bandgap
6.9	±3%	LM329A	10ppm (max)	600μA to 15mA	1.0 (typ)	Low Drift
	±5%	LM329B	20ppm (max)	600μA to 15mA	1.0 (typ)	Low Drift
	±5%	LM329C	50ppm (max)	600μA to 15mA	1.0 (typ)	General Purpose
	±5%	LM329D	100ppm (max)	600μA to 15mA	1.0 (typ)	General Purpose
	±4%	LTZ1000	0.1ppm/°C	4mA	20.0	Ultra Low Drift, 2ppm Long Term Stability*
6.95	±5%	LM399	2ppm (max)	500μA to 10mA	1.5	Ultra Low Drift
	±5%	LM399A	1ppm (max)	500μA to 10mA	1.5	Ultra Low Drift
7.0	±0.7%	LT1021BC-7	5ppm (max)	1.0mA	0.2	Low Drift/Noise, Exc. Stability
	±0.7%	LT1021DC-7	20ppm (max)	1.0mA	0.2	Low Cost, High Performance
10.0	±0.2%	LT1019C-10	20ppm (max)	1.2mA	N/A	Precision Bandgap
	±0.5%	LT1021BC-10	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.05%	LT1021CC-10	20ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.5%	LT021DC-10	20ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.5%	LT1031BC	5ppm (max)	1.7mA	0.25	Very Low Drift
	±0.1%	LT1031CC	15ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	±0.2%	LT1031DC	25ppm (max)	1.7mA	0.25	Low Cost, High Performance
	±0.3%	AD581J	30ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.1%	AD581K	15ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	±0.3%	REF01E	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
	±0.5%	REF01H	25ppm (max)	1.4mA	N/A	Precision Bandgap
	±1%	REF01C	65ppm (max)	1.6mA	N/A	Precision Bandgap

*LTZ1000 requires external control and biasing circuits.

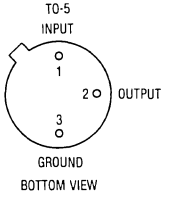
AD580



– FEATURES –
- 2.5V Output
- Direct Replacement for Analog Devices
- Selected Parts with 10ppm/°C TC
- Low Quiescent Current

– MINI DESCRIPTION –
Alternate source for industry standard 2.5V 3 terminal reference.

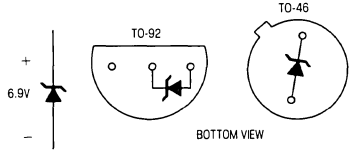
AD581



– FEATURES –
- 10V Output
- Direct Replacement for Analog Devices
- Low Quiescent Current

– MINI DESCRIPTION –
Alternate source for industry standard 10V 3-terminal reference.

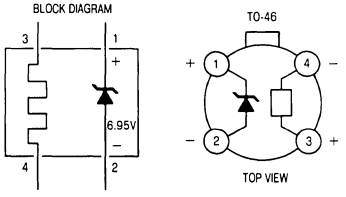
LM129/329



– FEATURES –
- Low Noise
- Low Cost
- Max Temperature Drift Selections 10, 20, 50 and 100ppm/°C
- Wide Operating Current Range

– MINI DESCRIPTION –
Subsurface zener reference with wide operating current range from 600μA to 15mA. Similar to LM199/399 without stabilizing heater on the die.

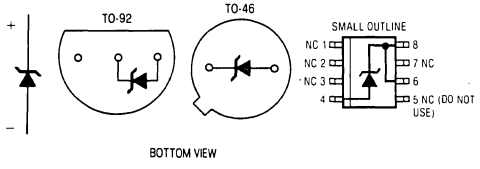
LM199A/199
LM399A/399



– FEATURES –
- Ultra Low Drift
- Very Low Noise
- Wide Operating Current Range
- Provided with Thermal Shield
- Excellent Long Term Stability
- Low Hysteresis
- Guaranteed Long Term Stability Available

– MINI DESCRIPTION –
An on board stabilizing heater keeps the die at constant temperature. Reference is a low noise subsurface zener. Excellent long term stability.

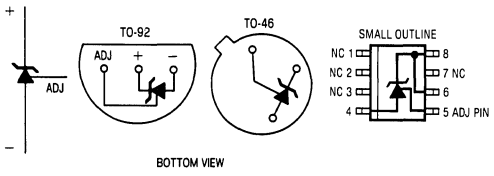
LT1004
LM185/385



– FEATURES –
- Micropower
- 1.235V and 2.5V Available
- Low Dynamic Impedance
- Wide Operating Current Range
- Very Tight Tolerance

– MINI DESCRIPTION –
Bandgap reference with operating current range as low as 10μA. Low noise and good long term stability.

LT1009
LM136/336



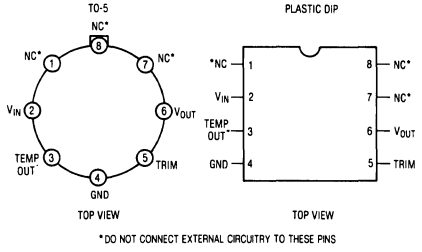
– FEATURES –

- No Adjustment Needed on LT1009
- Temperature Coefficient or Voltage Easily Adjusted on LM136
- Wide Operating Current Range
- Low Cost
- 2.5V
- Very Tight Tolerance

– MINI DESCRIPTION –

General purpose reference using bandgap circuit. Low cost, medium performance.

LT1019



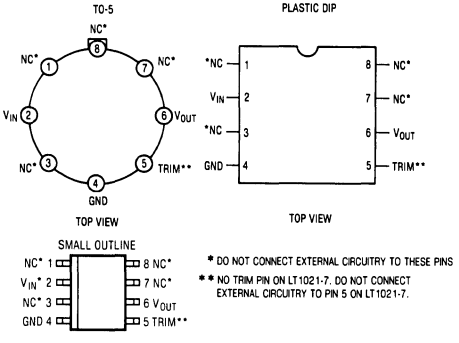
– FEATURES –

- 2.5V, 5V and 10V Versions
- Plug-In Replacement for Many Devices
- Series or Shunt Operation
- Low Drift—3ppm/°C Typ.
- 100% Noise Tested
- Optional Chip Heater Can Be Used for Lower Drift
- Temperature Output

– MINI DESCRIPTION –

Curvature corrected bandgap design for very low drift and tight initial tolerance. Replaces and upgrades REF01, REF02, MC14XX and other popular series type references.

LT1021



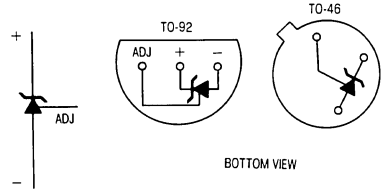
– FEATURES –

- Ultra Low Drift
- Trimmed Output Voltage
- Very Low Noise
- Operates in Series or Shunt Mode
- Replaces REF01, REF02, LM368, MC1400 and MC1404 with Improved Stability, Noise and Drift

– MINI DESCRIPTION –

Trimmed voltage reference with ultra low drift. Reference is a low noise subsurface zener. Available in 5V, 7V and 10V versions. The 7V and 10V versions can be used as 2-terminal shunt regulators as well as series references.

LT1029



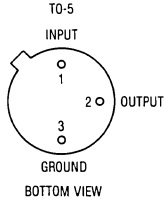
– FEATURES –

- 0.2% Output Tolerance
- 0.05Ω Shunt Impedance
- 600μA to 10mA Operating Current
- Pin Compatible with LM136-5
- 20ppm/°C Max. Drift Output Voltage Trim does not Affect Drift
- Can be Used as Positive or Negative Reference

– MINI DESCRIPTION –

Precision 3 terminal shunt 5V bandgap reference. Very low drift and tight initial output tolerance.

LT1031/LH0070



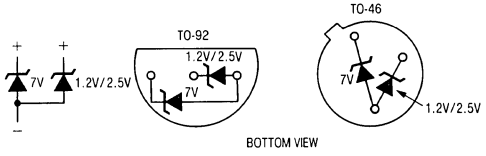
– FEATURES –

- 10V Output
- Ultra Low Drift
- Very Low Noise
- Trimmed Output Voltage
- Operates in Series or Shunt Mode
- Pin Compatible with AD581
- LH0070 is a Direct Replacement for NSC LH0070

– MINI DESCRIPTION –

Very low tempco is achieved without chip heater. The LT1031 can replace the AD581 with better specifications.

LT1034



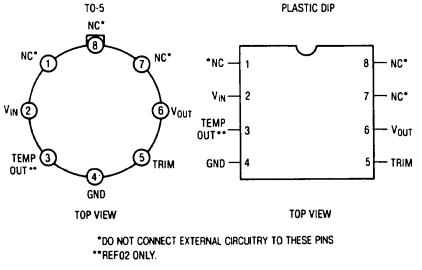
– FEATURES –

- 1.2V and 2.5 Versions
- *Guaranteed* Drift of 20ppm/°C and 40ppm/°C
- 1.2V and 7V Reference
- 1.2V Reference Operates 20μA to 20mA
- 1% Tolerance on 1.2V Reference
- 7V Reference Operates 100μA to 20mA
- Compatible with the LM385 and LT1004

– MINI DESCRIPTION –

The LT1034 is a bandgap 1.2V or 2.5V reference with low operating current and low temperature coefficient, combined with a 7V subsurface zener reference on the same chip.

REF01/REF02



– FEATURES –

- Direct Replacement for PMI Devices
- Low Drift
- High Line Rejection
- Low Supply Current
- Temperature Output on REF02

– MINI DESCRIPTION –

Industry standard 5V and 10V bandgap voltage references.

FEATURES

- 1.2μVp-p Noise
- 2μV Long Term Stability
- Very Low Hysteresis
- 0.05ppm/°C Drift
- Temperature Stabilized

APPLICATIONS

- Voltmeters
- Calibrators
- Standard Cells
- Scales
- Low Noise RF Oscillators

DESCRIPTION

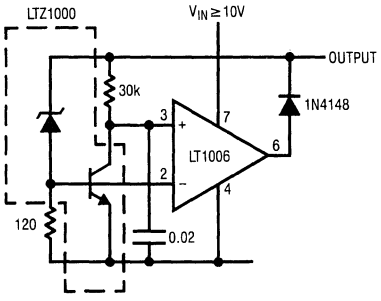
The LTZ1000 and LTZ1000A are ultra stable temperature controllable references. They are designed to provide 7V outputs with temperature drifts of 0.05ppm/°C, about 1.2μVp-p of noise and long term stabilities of 2μV per month.

Included on the chip is a subsurface zener reference, heater resistor for temperature stabilization, and a temperature sensing transistor. External circuitry is used to set operating currents and to temperature stabilize the reference. This allows maximum flexibility and best long term stability and noise.

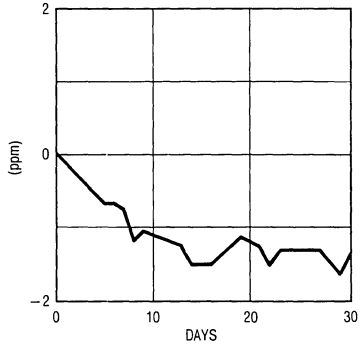
The LTZ1000 and LTZ1000A references can provide superior performance to older references such as the LM199 at the expense of increased circuit complexity and thermal layout considerations. The LTZ1000 is packaged in a standard TO-99 package while the LTZ1000A utilizes a proprietary high thermal resistance die attach which eases thermally insulating the reference.

TYPICAL APPLICATION

Low Noise Reference



Long Term Stability



LONG TERM STABILITY OF A TYPICAL DEVICE FROM TIME = 0 WITH NO PRECONDITIONING OR AGING

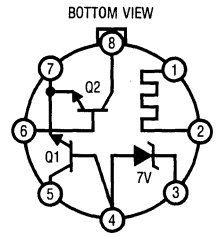
ABSOLUTE MAXIMUM RATINGS

Heater to Substrate 35V
Collector Emitter Breakdown Q1 ..... 15V
Collector Emitter Breakdown Q2 ..... 35V
Emitter Base Reverse Bias 2V
Operating Temperature Range ..... $-55°C \leq T_A \leq 125°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq 150°C$
Substrate Forward Bias 0.1V

PRECONDITIONING

150°C Burn-In

PACKAGE/ORDER INFORMATION



H8 PACKAGE
METAL CAN

ORDER PART NUMBER
LTZ1000 LTZ1000A

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zener Voltage	$I_Z = 5mA$, $(V_Z + VBE_{Q1})$ $I_{Q1} = 100\mu A$ $I_Z = 1\ mA$, $(V_Z + VBE_{Q1})$ $I_{Q1} = 100\mu A$	7.0 6.9	7.2 7.15	7.5 7.45	V V
Zener Change with Current	$1mA \leq I_Z < 5mA$		80	240	mV
Zener Leakage Current	$V_Z = 5V$		20	200	μA
Zener Noise	$I_Z = 5mA$, $0.1Hz < f < 10Hz$ $I_{Q1} = 100\mu A$		1.2	2	$\mu Vp\text{-}p$
Heater Resistance	$I_L \leq 100\mu A$	200	300	420	Ω
Heater Breakdown Voltage		35			V
Transistor Q1 Breakdown	$I_C = 10\mu A$, LVCEO	15	20		V
Transistor Q2 Breakdown	$I_C = 10\mu A$, LVCEO	35	50		V
Q1, Q2 Current Gain	$I_C = 100\mu A$	80	200	450	
Thermal Resistance	LTZ1000 Time = 5 Minutes LTZ1000A Time = 5 Minutes		80 400		°C/W °C/W
Long Term Stability	T = 65°C		2		$\mu V/\sqrt{khr}$

Note 1: All testing is done at 25°C. Pulse testing is used for LTZ1000A to minimize temperature rise during testing. LTZ1000 and LTZ1000A devices are QA tested at −55°C and 125°C.

PIN FUNCTIONS

Pin 1: Heater positive. Must be more positive than Pin 4 and less than 40V.

Pin 2: Heater negative. Must be more positive than Pin 4 and less than 40V.

Pin 3: Zener positive. Must be more positive than Pin 4.

Pin 4: Substrate and Zener negative. Must be more positive than pin 7. If Q1 is Zenered (about 7V) a permanent degradation in beta will result.

Pin 5: Temperature compensating transistor collector.

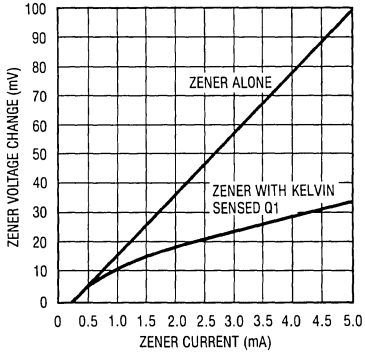
Pin 6: Temperature sensing transistor base. If the base emitter junction is Zenered (about 7V) the transistor will suffer permanent beta degradation.

Pin 7: Emitter of sensing and compensating transistors.

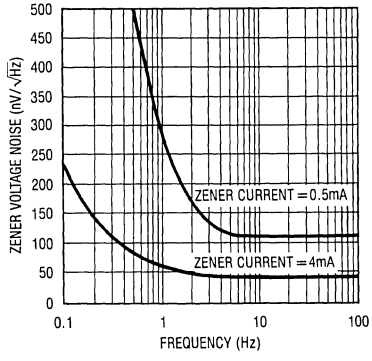
Pin 8: Collector of sensing transistor.

TYPICAL PERFORMANCE CHARACTERISTICS

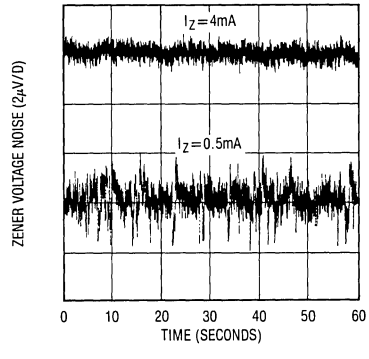
Zener Voltage vs Current



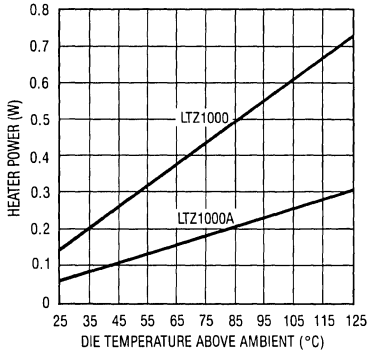
Zener Voltage Noise Spectrum



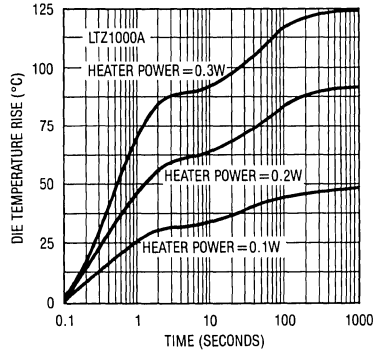
Zener Noise



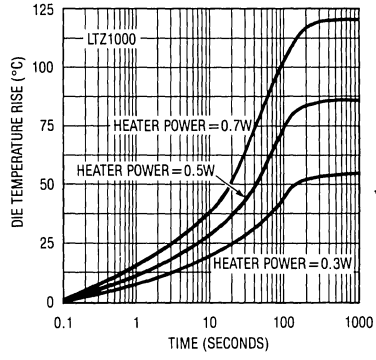
Die Temperature Rise vs Heater Power



Die Temperature Rise vs Time



Die Temperature Rise vs Time



APPLICATION HINTS

LTZ1000 and LTZ1000A are capable of providing ultimate voltage reference performance. Temperature drifts of better than 0.03ppm/°C and long term stability on the order of 1μV per month can be achieved. Noise of about 0.15ppm can also be obtained. This performance is at the expense of circuit complexity, since external influences can easily cause output voltage shifts of more than 1ppm.

Thermocouple effects are one of the worst problems and can give apparent drifts of many ppm/°C as well as cause low frequency noise. The kovar input leads of the TO-5 package form thermocouples when connected to copper PC boards. These thermocouples generate outputs of 35μV/°C. It is mandatory to keep the zener and transistor leads at the same temperature, otherwise 1 to 5ppm shifts in the output voltage can easily be expected from these thermocouples.

Air currents blowing across the leads can also cause small temperature variations, especially since the package is heated. This will look like 1 to 5ppm of low frequency noise occurring over a several minute period. For best results, the device should be located in an enclosed area and well shielded from air currents.

Certainly, any temperature gradient externally generated, say from a power supply, should not appear across the critical circuitry. The leads to the transistor and zener should be connected to equal size PC traces to equalize the heat loss and maintain them at similar temperatures. The bottom portion of the PC board should be shielded against air currents as well.

Resistors, as well as having resistance temperature coefficients, can generate thermocouple effects. Some types of resistors can generate hundreds of microvolts of thermocouple voltage. These thermocouple effects in the resistor can also interfere with the output voltage. Wire wound resistors usually have the lowest thermocouple voltage, while tin oxide type resistors have very high thermocouple voltage. Film resistors, especially Vishay precision film resistors, can have low thermocouple voltage.

Ordinary breadboarding techniques are not good enough to give stable output voltage with the LTZ1000 family devices. For breadboarding, it is suggested that a small printed circuit board be made up using the reference, the amplifier, and wire wound resistors. Care must be taken to ensure that heater current does not flow through the same ground lead as the negative side of the reference (emitter of Q1). Current changes in the heater could add to or subtract from the reference voltage causing errors with temperature. Single point grounding using low resistance wiring is suggested.

Setting Control Temperature

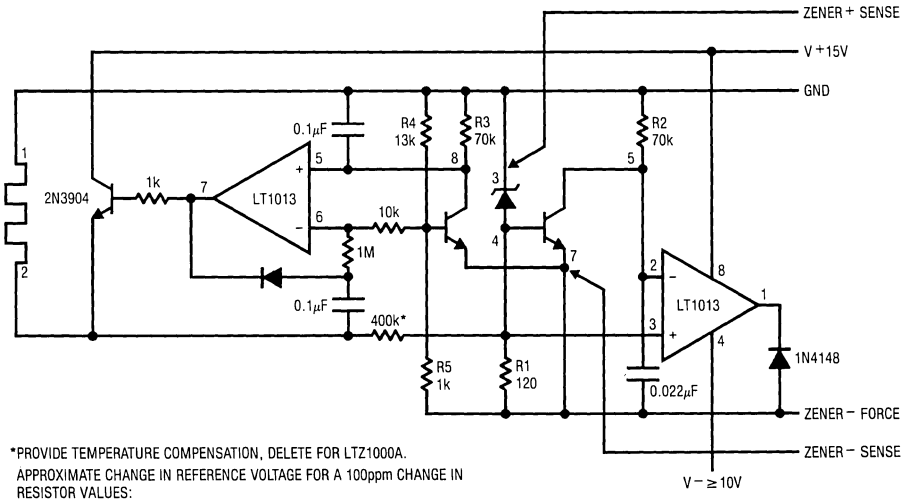
The emitter-base voltage of the control transistor sets the stabilization temperature for the LTZ1000. With the values given in the applications, temperature is normally 60°C. Production variations in emitter-base voltage will typically cause about ± 10°C variation. Since the emitter-base voltage changes about 2mV/°C and is very predictable, other temperatures are easily set.

The lowest temperature consistent with the operating environment should be used. Higher temperatures accelerate aging and decrease long term stability. The LTZ1000A should be set about 10°C higher than the LTZ1000. This is because normal operating power dissipation in the LTZ1000A causes a temperature rise of about 10°C. Of course both types of devices should be insulated from ambient. Several minutes of warm-up is usual.

For applications not requiring the extreme precision or the low noise of the LTZ1000, Linear Technology makes a broad line of voltage references. Devices like the LT1021 can provide drifts as low as 2ppm/°C and devices such as the LM399A can provide drifts of 1ppm/°C. Only applications requiring the very low noise or low drift with time of the LTZ1000 should use this device. Application help is available from Linear Technology.

TYPICAL APPLICATIONS

Negative Voltage Reference



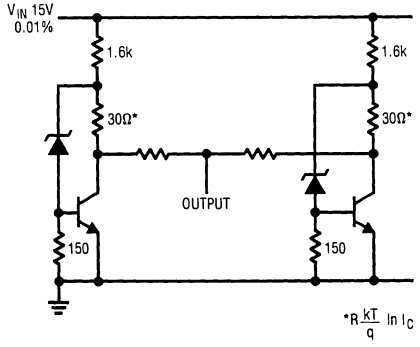
*PROVIDE TEMPERATURE COMPENSATION, DELETE FOR LTZ1000A.

APPROXIMATE CHANGE IN REFERENCE VOLTAGE FOR A 100ppm CHANGE IN RESISTOR VALUES:

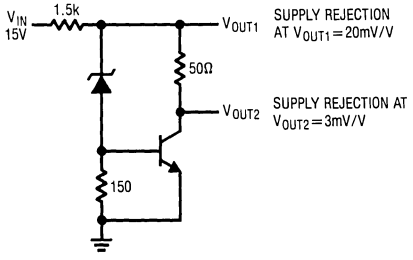
	100ppm = △R(Ω)	△V_Z
R1	0.012Ω	1ppm
R2	7Ω	0.3ppm
R3	7Ω	0.2ppm
R4/R5 RATIO	△R = 0.01%	1ppm

BOTH A1 AND A2 CONTRIBUTE LESS THAN 2μV OF OUTPUT DRIFT OVER A 50°C RANGE.

Averaging Reference Voltages for Lower Noise and Better Stability

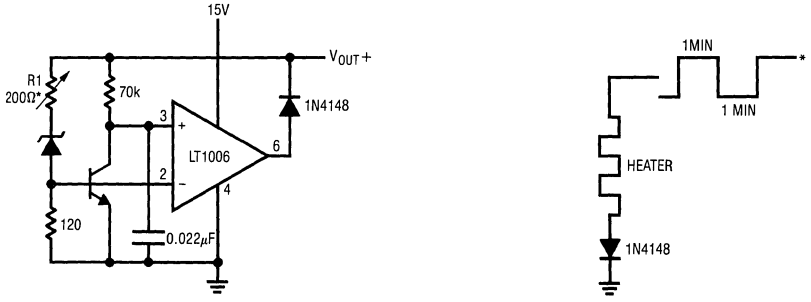


Improving Supply Rejection



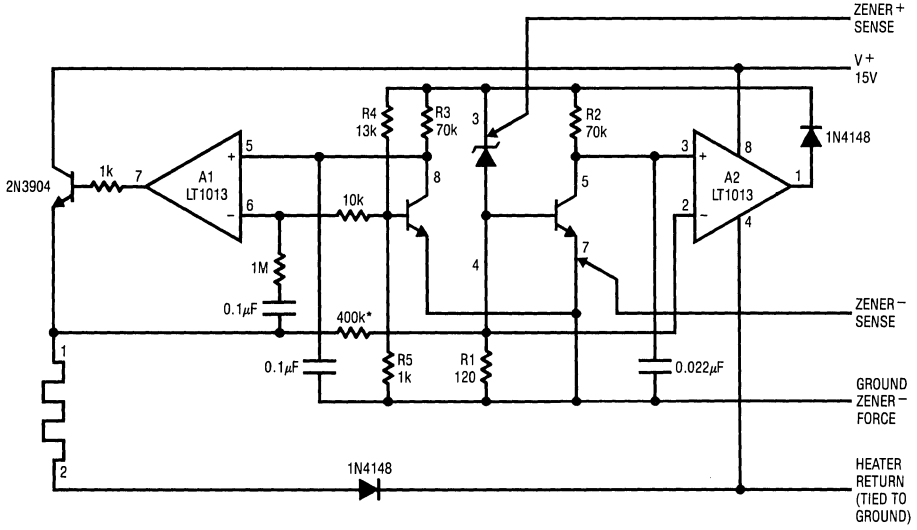
TYPICAL APPLICATIONS

Adjusting Temperature Coefficient in Unstabilized Applications



*PULSE HEATER ON AND OFF TO HEAT AND COOL THE REFERENCE. ADJUST R1 FOR MINIMUM VOLTAGE CHANGE THROUGH A TEMPERATURE CYCLE.

7V Positive Reference Circuit



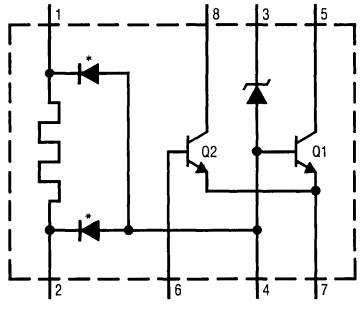
*PROVIDES TC COMPENSATION, DELETE FOR LTZ1000A.

APPROXIMATE CHANGE IN REFERENCE VOLTAGE FOR A 100ppm (0.01%) CHANGE IN RESISTOR VALUES:

	△R(Ω)	$\triangle V_Z$
R1	0.012Ω	1ppm
R2	7Ω	0.3ppm
R3	7Ω	0.2ppm
R4/R5 RATIO	△R=0.01%	1ppm

BOTH A1 AND A2 CONTRIBUTE LESS THAN 2μV OF OUTPUT DRIFT OVER A 50°C RANGE.

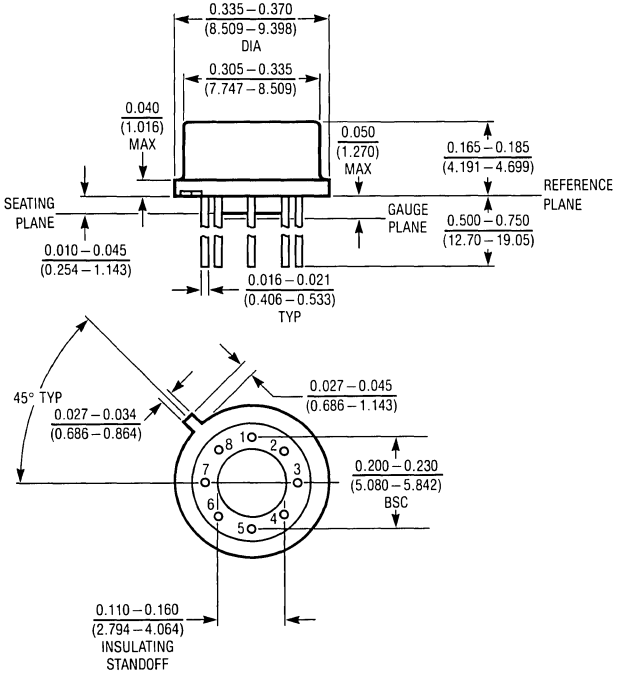
BLOCK DIAGRAM



*SUBSTRATE DIODES-DO NOT FORWARD BIAS

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H8 Package
Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN
THE REFERENCE PLANE AND SEATING PLANE.

	θ_{JA}
LTZ1000	80°C/W
LTZ1000A	400°C/W

SECTION 5—COMPARATORS

SECTION 5—COMPARATORS

MILITARY

PART NUMBER	RESPONSE TIME MAX (ns)	V_{OS} MAX (mV)	I_B MAX (nA)	DRIVE CAPABILITY (mA)	GAIN MIN (V/mV)	I_{SUPPLY} POSITIVE (mA)	I_{SUPPLY} NEGATIVE (mA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
LT1011AM	250	0.5	25	50	200	4.0	2.5	H, J8	Low V_{OS}, Low I_B, High Output Drive, 12 Bit Acc.
LT1011M	250	1.5	50	50	200	4.0	2.5	H, J8	
LT1016M	12	±2.5	10000	10	2	35	5	H, J8	Ultra High Speed, TTL Outputs, True Output Latch, Stable in Active Region, Pin/Pin Replacement for AM686.
LT1017M	—	1	15	30	1000	0.060	—	H, J8	LT1017 Has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pin-Out as 193 Types.
LT1018M	—	1	75	35	1000	0.250	—	H, J8	
LT111A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V_{OS}, High Gain
LM111	—	3.0	100	50	40	6.0	5.0	H, J8	General Purpose
LT119A	80 (typ)	1.0	500	25	20	11.5	4.5	H, J	Dual, Low V_{OS}, Hi CMRR
LM119	80 (typ)	4.0	500	25	10	11.5	4.5	H, J	Dual, General Purpose
LTC1040M	100µs	0.5	3	*	†	300nA**	1nA	J	CMOS Sampling Comparator
LTC1042M	100µs	1.0	3	*	†	300nA**	1nA	J	CMOS Window Comparator

COMMERCIAL

PART NUMBER	RESPONSE TIME MAX (ns)	V_{OS} MAX (mV)	I_B MAX (nA)	DRIVE CAPABILITY (mA)	GAIN MIN (V/mV)	I_{SUPPLY} POSITIVE (mA)	I_{SUPPLY} NEGATIVE (mA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
LT1011AC	250	0.5	25	50	200	4.0	2.5	H, J8, N8	Low V_{OS}, Low I_B, High Output Drive, 12 Bit Acc.
LT1011C	250	0.5	50	50	200	4.0	2.5	H, J8, N8	
LT1016C	12	±2.5	10000	10	2	35	5	H, J8	Ultra High Speed, TTL Outputs, True Output Latch, Stable in Active Region, Pin/Pin Replacement for AM686.
LT1017C	—	1	15	30	1000	0.060	—	H	LT1017 Has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pin-Out as 193 Types.
LT1018C	—	1	75	35	1000	0.250	—	H	
LT311A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V_{OS}, High Gain
LM311	—	7.5	250	50	40	7.5	5.0	H, J8	General Purpose
LT319A	80 (typ)	1.0	500	25	20	12.5	5.0	H, J, N	Dual, Low V_{OS}, Hi CMRR
LM319	80 (typ)	8.0	1000	25	8	12.5	5.0	H, J, N	Dual, General Purpose
LTC1040C	100µs	0.5	3	*	†	300nA**	1nA	J, N	CMOS Sampling Comparator
LTC1042C	100µs	1.0	3	*	†	300nA**	1nA	J, N	CMOS Window Comparator

*1 Std. TTL Load **Supply Current Depends on Clock Rate †Gain errors are included in V_{OS} spec.

Window Comparator

FEATURES

- Micropower 1.5μW (1 Sample/Second)
- Wide Supply Range— + 2.8V to + 16V
- High Accuracy
  - Center Error ± 1mV Max
  - Width Error ± 0.15% Max
- Wide Input Voltage Range
  - V^+ to Ground
- TTL Outputs with 5V Supply
- Two Independent Ground-Referred Control Inputs
- Small Size 8-Pin MiniDIP

APPLICATIONS

- Fault Detectors
- Go/No-Go Testing
- Microprocessor Power Supply Monitor

DESCRIPTION

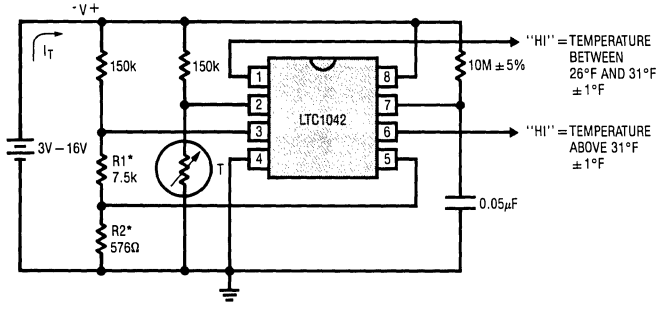
The LTC1042 is a monolithic CMOS window comparator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Two high impedance voltage inputs, CENTER and WIDTH/2, define the middle and width of the comparison window. Whenever the input voltage, V_{IN}, is inside the window the WITHIN WINDOW output is high. The ABOVE WINDOW output is high whenever V_{IN} is above the window. By interchanging V_{IN} and CENTER the ABOVE WINDOW output becomes BELOW WINDOW and is high if V_{IN} is below the window.

Sampling techniques provide high impedance voltage inputs that can common-mode to both supply rails (V^+ and GND). An important feature of the inputs is their non-interaction. Also the device is effectively "chopper stabilized", giving it extremely high accuracy over all conditions of temperature, power supply and input voltage range.

Another benefit of the sampling techniques used to design the LTC1042 is the extremely low power consumption. When the device is strobed, it internally turns on the power to the comparators, samples the inputs, stores the outputs in CMOS latches and then turns off power to the comparators. This all happens in about 80μs. Average power can be made small, almost arbitrarily, by lowering the strobe rate. The device can be self-strobed using an external RC network or strobed externally by driving the OSC pin with a CMOS gate.

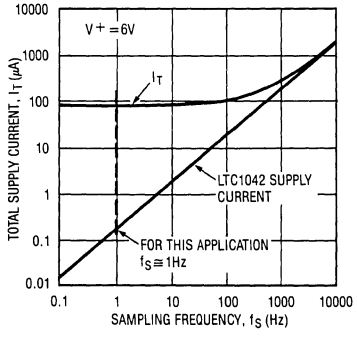
LTCMOS™ is a trademark of Linear Technology Corp.

Battery Powered Remote Freezer Alarm



T = YELLOW SPRINGS INSTRUMENT CO., INC. P/N 44007.
ALL RESISTORS ±1% UNLESS OTHERWISE SPECIFIED.
*OTHER TEMPERATURE BANDS MAY BE SELECTED BY CHOOSING APPROPRIATE VALUES FOR R1 AND R2.

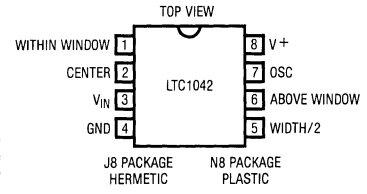
Total Supply Current vs Sampling Frequency



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to GND) 18V
Input Voltage ..... $V^+ + 0.3V$ to $-0.3V$
Operating Temperature Range
LTC1042C ..... $-40°C$ to $85°C$
LTC1042M ..... $-55°C$ to $125°C$
Storage Temperature Range ..... $-55°C$ to $150°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C
Output Short Circuit Duration ..... Continuous

PACKAGE/ORDER INFORMATION



J8 PACKAGE HERMETIC
N8 PACKAGE PLASTIC

ORDER PART NUMBER
LTC1042MJ8 LTC1042CN8

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
	Center Error (Note 2)	$V^+ = 2.8V$ to 6V (Note 1)	●		±0.3 + ±0.05	±1 + ±0.15	mV % WIDTH/2
		$V^+ = 6V$ to 15V (Note 1)	●		±1 + ±0.05	±3 + ±0.15	mV % WIDTH/2
	Width Error (Note 3)	$V^+ = 2.8V$ to 6V (Note 1)	●		±0.6 + ±0.1	±2 + ±0.3	mV % WIDTH/2
		$V^+ = 6V$ to 15V (Note 1)	●		±2 + ±0.1	±6 + ±0.3	mV % WIDTH/2
I_{BIAS}	Input Bias Current	$V^+ = 5V$, $T_A = 25°C$, OSC = GND V_{IN}, CENTER and WIDTH/2 Inputs			±0.3		nA
R_{IN}	Average Input Resistance	$f_S = 1kHz$ (Note 4)	●	10	15		MΩ
	Input Voltage Range		●	GND		V^+	V
PSR	Power Supply Range		●	2.8		16	V
$I_{S(ON)}$	Power Supply ON Current (Note 5)	$V^+ = 5V$	●		1.2	3	mA
$I_{S(OFF)}$	Power Supply OFF Current (Note 5)	$V^+ = 5V$ LTC1042C LTC1042M	● ●		0.001 0.001	0.5 5.0	μA μA
T_D	Response Time (Note 6)	$V^+ = 5V$			80	100	μs
	Output Levels						
V_{OH}	Logic 1 Output	$V^+ = 4.75V$, $I_{OUT} = -360\mu A$	●	2.4	4.4		V
V_{OL}	Logical 0 Output	$V^+ = 4.75V$, $I_{OUT} = 1.6mA$	●		0.25	0.45	V
R_{EXT}	External Timing Resistor	Resistor Connected between V^+ and OSC Pin	●	100		10,000	kΩ
f_S	Sampling Frequency	$V^+ = 5V$, $T_A = 25°C$ $R_{EXT} = 1M\Omega$, $C_{EXT} = 0.1\mu F$			5		Hz

The ● denotes the specfications which apply over the full operating temperature range.

Note 1: Applies over input voltage range limit and includes gain uncertainty.

Note 2: Center error = $[(V_U + V_L)/2 - \text{CENTER}]$ (where V_U = upper band limit and V_L = lower band limit).

Note 3: Width error = $(V_U - V_L - 2 \times \text{WIDTH}/2)$ (where V_U = upper band limit and V_L = lower band limit).

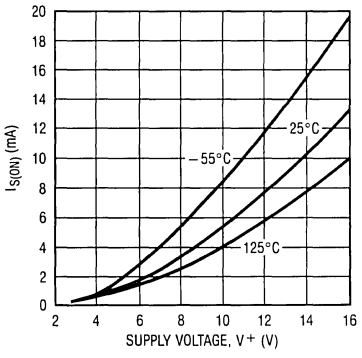
Note 4: R_{IN} is guaranteed by design and is not tested. $R_{IN} = 1/(f_S \times 66pF)$.

Note 5: Average supply current = $T_D \times I_{S(ON)} \times f_S + (1 - T_D f_S) I_{S(OFF)}$.

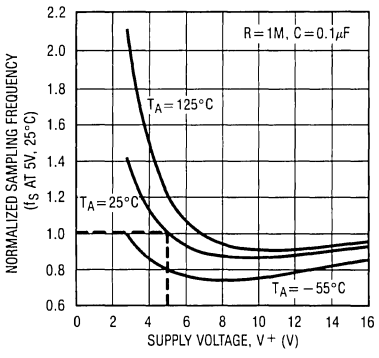
Note 6: Response time is set by an internal oscillator and is independent of overdrive voltage. T_D is guaranteed by correlation test and is not directly measured.

TYPICAL PERFORMANCE CHARACTERISTICS

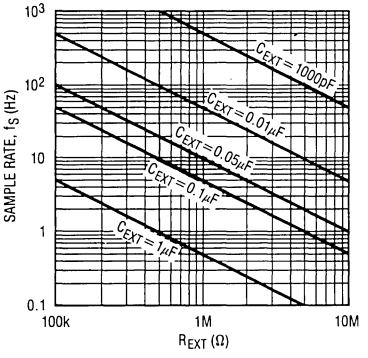
$I_{S(ON)}$ vs V^+



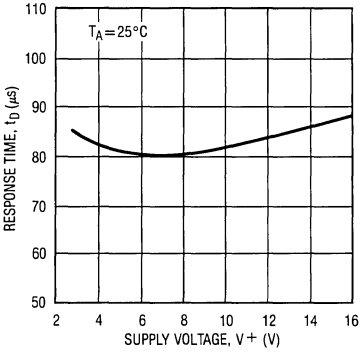
Normalized Sampling Frequency vs V^+, Temperature



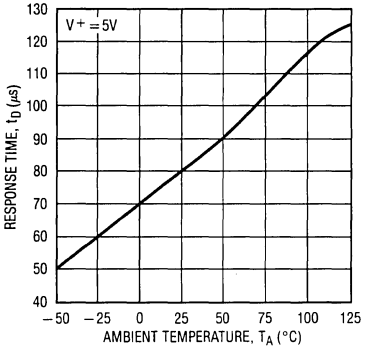
Sampling Rate vs R_{EXT}, C_{EXT}



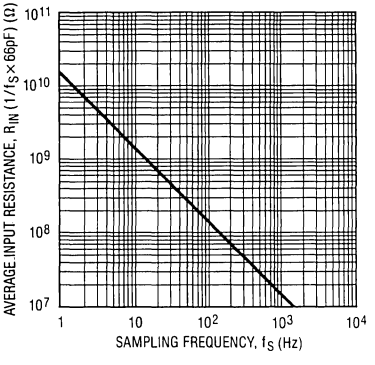
Response Time vs Supply Voltage



Response Time vs Temperature



R_{IN} vs Sampling Frequency



APPLICATIONS INFORMATION

The LTC1042 uses sampled data techniques to achieve its unique characteristics. It consists of two comparators, each of which has two differential inputs (Figure 1). When the sum of the voltages on a comparator's inputs is positive, the output is high; when the sum is negative, the output is low. The inputs are interconnected such that when (CENTER – WIDTH/2) ≤ V_{IN} ≤ (CENTER + WIDTH/2) both comparator outputs are low. In this condition V_{IN} is within the window and the WITHIN WINDOW output is high. When V_{IN} > CENTER + WIDTH/2, V_{IN} is above the window and the ABOVE WINDOW output is high.

APPLICATIONS INFORMATION

An important feature of the LTC1042 is the non-interaction of the inputs. This means the center and width of the window can be changed without one affecting the other. Also note that the width of the window is set by a ground referred signal (WIDTH/2).

Strobing

An external oscillator allows the LTC1042 to strobe itself. The frequency of oscillation sets the sampling rate and is set with an external RC network (see typical curve, OSC frequency vs R_{EXT}, C_{EXT}). To assure oscillation, under all conditions, R_{EXT} must be between 100kΩ and 10MΩ. There is no limit to the size of C_{EXT}.

A sampling cycle is initiated on the positive going transition of the voltage on the OSC pin. When this voltage is near the positive supply, a Schmitt trigger trips and initiates the sampling cycle. A sampling cycle consists of applying power to both comparators, sampling the inputs, storing the results in CMOS output latches and turning power off. This whole process takes approximately 80μs. During the 80μs "active" time, the LTC1042 draws typically 1.2mA ($I_{S(ON)}$) at $V^+ = 5V$. Because power is consumed only during the "active" time, extremely low average power consumption can be achieved at low sample rates. For example at a sample rate of 1 sample/second the average power consumption is:

$$\text{Power} = (V^+)(I_{S(AVG)}) = 5V \times 1.2mA \times 80\mu s/1sec$$
$$= 0.48\mu W$$

At low sampling rates, R_{EXT} dominates the power consumption. R_{EXT} consumes power continuously. The average voltage at the OSC pin is approximately $V^+/2$. The power consumed by R_{EXT} is:

$$P(R_{EXT}) = (V^+/2)^2/R_{EXT}$$

EXAMPLE: Assume $R_{EXT} = 1M\Omega$ and $V^+ = 5V$. Then:
$P(R_{EXT}) = (2.5)^2/1M\Omega = 6.25\mu W$

This is more than ten times the typical power consumed by the LTC1042 at $V^+ = 5V$ and 1 sample/second. Where power is a premium, R_{EXT} should be made as large as possible. Note that the power dissipated by R_{EXT} is *not* a function of the sampling frequency or C_{EXT}.

If high sampling rates are needed and power consumption is of secondary importance, a convenient way to get the maximum possible sampling rate is to make $R_{EXT} = 100k\Omega$ and $C_{EXT} = 0$. The sampling rate, set by the LTC1042's active time, will nominally be ≈10kHz.

To synchronize the sampling of the LTC1042 to an external frequency source, the OSC pin can be driven by a CMOS gate. A CMOS gate is necessary because the input trip points of the oscillator are close to the supply rails and TTL does not have enough output swing. Externally driven, there will be a delay from the rising edge of the OSC input and the start of the sampling cycle of approximately 5μs.

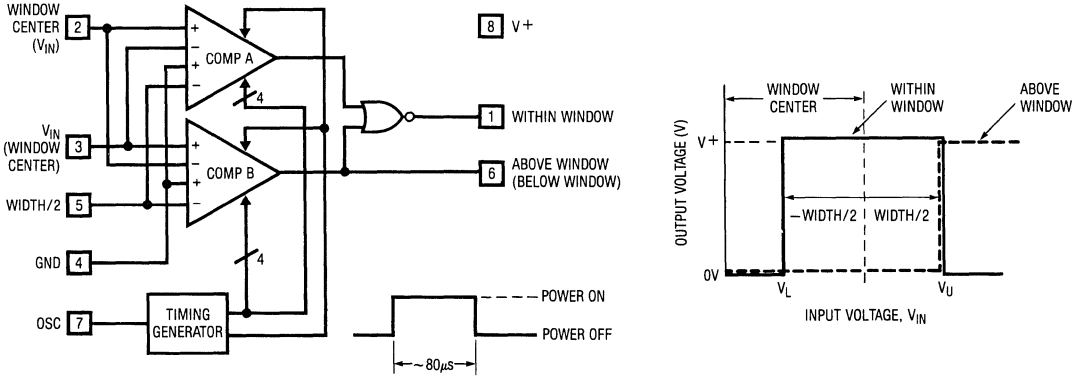


Figure 1. LTC1042 Block Diagram

APPLICATIONS INFORMATION

Input Impedance

The input impedance of the LTC1042 does not look like a classic linear comparator. CMOS switches and a precision capacitor array form the dual differential input structure. Input impedance characteristics can be determined from the equivalent circuit shown in Figure 2. The input capacitance will charge with a time constant of $R_S \times C_{IN}$. It is critical, in determining errors caused by the input charging current, that C_{IN} be fully charged during the "active" time.

For $R_S \leq 10k\Omega$

For R_S less than or equal to 10kΩ, C_{IN} fully charges and no error is caused by the charging current.

For $R_S > 10k\Omega$

For source resistances greater than 10kΩ, C_{IN} cannot fully charge, causing voltage errors. To minimize these errors an input bypass capacitor, C_S, should be used. Charge is shared between C_{IN} and C_S, causing a voltage error. The magnitude of this error is $\Delta V = V_{IN} \times C_{IN}/(C_{IN} + C_S)$. This error can be made arbitrarily small by increasing C_S.

The averaging effect of the bypass capacitor C_S causes another error term. Each time the input switches cycle between the plus and minus inputs, C_{IN} is charged and discharged. The average input current due to this is $I_{AVG} = V_{IN} \times C_{IN} \times f_S$, where f_S is the sampling frequency. Because the input current is directly proportional to the differential input voltage, the LTC1042 can be said to have an average input resistance of $R_{IN} = V_{IN}/I_{AVG} = 1/(f_S \times C_{IN})$.

Since two comparator inputs are connected in parallel, R_{IN} is one half this value (see typical curve of R_{IN} vs Sampling Frequency). This finite input resistance causes an error due to voltage divider between R_S and R_{IN}.

The input error caused by both of these effects is $V_{ERROR} = V_{IN}[2C_{IN}/(2C_{IN} + C_S) + R_S/(R_S + R_{IN})]$.

EXAMPLE: Assume $f_S = 10Hz$, $R_S = 1M\Omega$, $C_S = 1\mu F$ and $V_{IN} = 1V$. Then $V_{ERROR} = 1V(66\mu V + 660\mu V) = 726\mu V$. If the sampling frequency is reduced to 1Hz, the voltage error from input impedance effects is reduced to 136μV.

Input Voltage Range

The input switches of the LTC1042 are capable of switching either to the V^+ supply or ground. Consequently, the input voltage range includes both supply rails. This is a further benefit of the input sampling structure.

Error Specifications

The only measurable errors on the LTC1042 are the deviations from "ideal" of the upper and lower window limits [Figure 1(B)]. The critical parameters for a window comparator are the width and center of the window. These errors may be expressed in terms of V_U and V_L.

$$\text{center error} = [(V_U + V_L)/2] - \text{CENTER}$$
$$\text{width error} = (V_U - V_L) - 2 \times (\text{WIDTH}/2)$$

The specified error limits (see Electrical Characteristics) include error due to offset, power supply variation, gain, time and temperature.

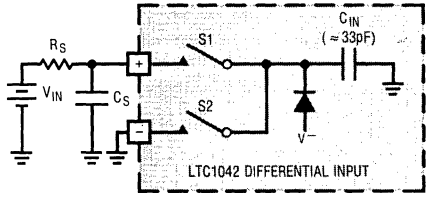
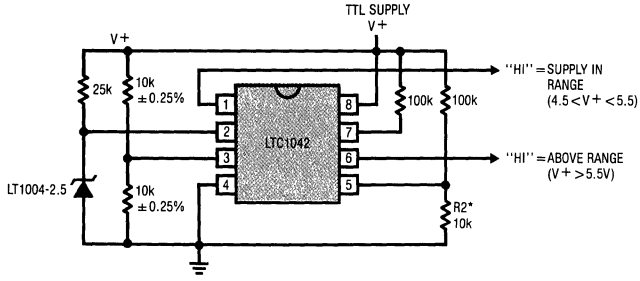


Figure 2. Equivalent Input Circuit

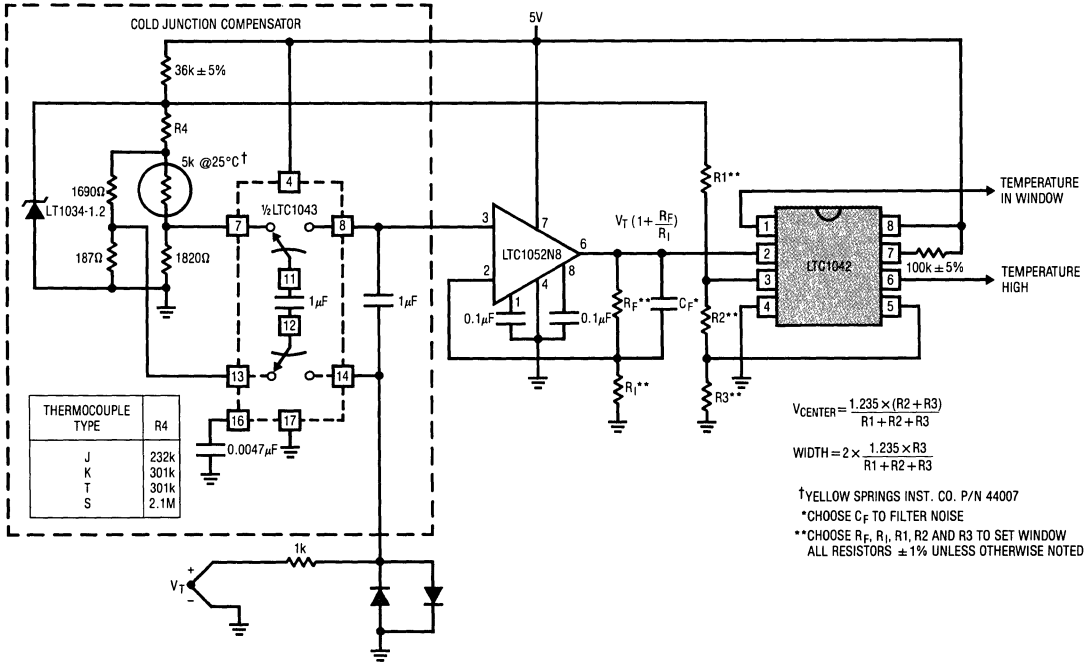
APPLICATIONS INFORMATION

TTL Power Supply Monitor



ALL RESISTORS ±5% UNLESS OTHERWISE NOTED.
*SUPPLY TOLERANCE EQUALS R2 IN kΩ. I.E., 10k = ±10%.

Single 5V Thermocouple Over Temperature Alarm



†YELLOW SPRINGS INST. CO. P/N 44007
*CHOOSE C_F TO FILTER NOISE
**CHOOSE R_F, R_I, R1, R2 AND R3 TO SET WINDOW
ALL RESISTORS ±1% UNLESS OTHERWISE NOTED

APPLICATIONS INFORMATION

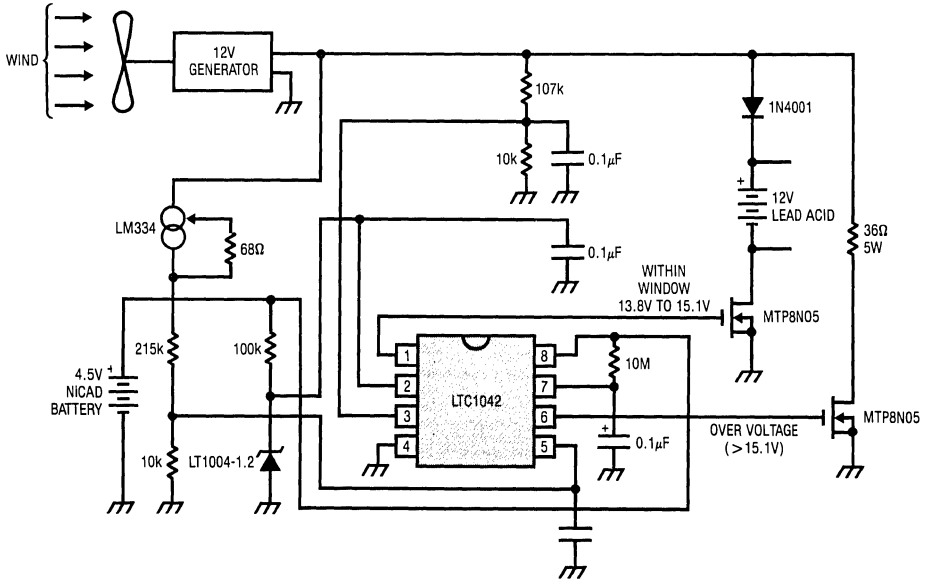
Wind Powered Battery Charger

A simple wind powered battery charger can be constructed using the new LTC1042, a 12V DC permanent magnet motor, and low cost power FET transistor.

The DC motor is used as a generator with the voltage output being proportional to its RPM. The LTC1042 monitors the voltage output and provides the following control functions.

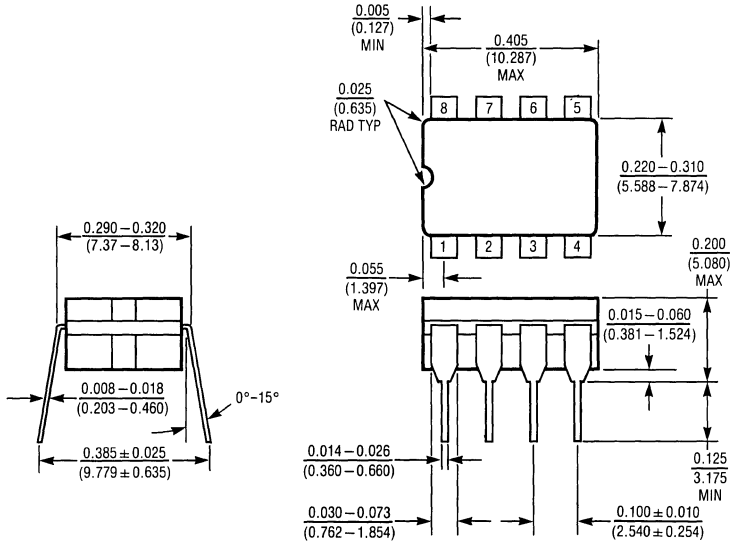
1) If generator voltage output is below 13.8V, the control circuit is active and the NiCad battery is charging through the LM334 current source. The lead acid battery is not being charged.
2) If the generator voltage output is between 13.8V and 15.1V, the 12V lead acid battery is being charged at about a 1 amp/hour rate (limited by the power FET).
3) If generator voltage exceeds 15.1V (a condition caused by excessive wind speed or 12V battery being fully charged) then a fixed load is connected thus limiting the generator RPM to prevent damage.

This charger can be used as a remote source of power where wind energy is plentiful such as on sailboats or remote radio repeater sites. Unlike solar powered panels, this system will function in bad weather and at night.



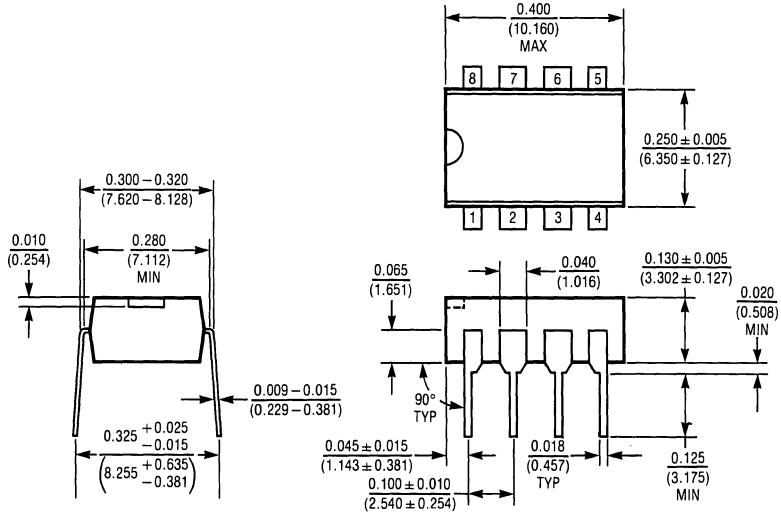
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8 Lead Hermetic DIP



T_{jmax}	θ_{JA}
150°C	100°C/W

N8 Package
8 Lead Plastic



T_{jmax}	θ_{JA}
110°C	150°C/W

Programmable Micropower Hex Translator / Receiver / Driver

FEATURES

- Efficiently Translate Voltage Levels
- Internal Hysteresis for Noise Immunity
- Output Latches Included
- Three-State Outputs
- Programmable Power/Speed
- Power can be Completely Shut Off
- ±50V on Inputs with External 100kΩ Limit Resistor
- 1.2μs Response at 100μA Supply Current

APPLICATIONS

- TTL/CMOS to ±5V Analog Switch Drive
- TTL to CMOS (3V to 15V V_{CC})
- ECL to CMOS (3V to 15V V_{CC})
- Ground Isolation Buffer
- Low Power RS232 Line Receiver

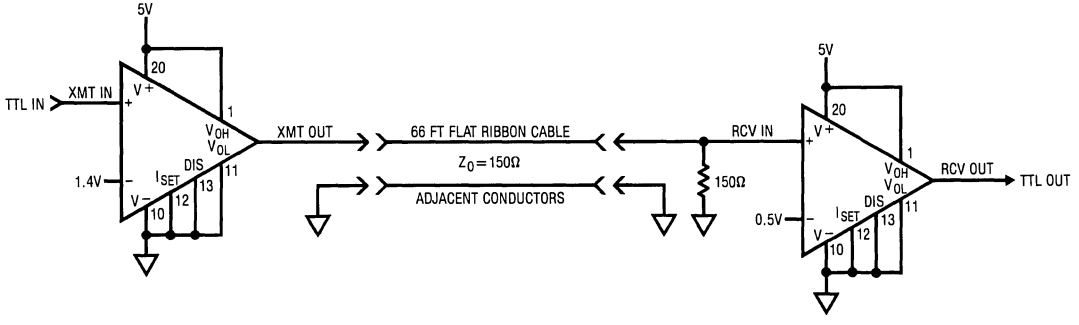
DESCRIPTION

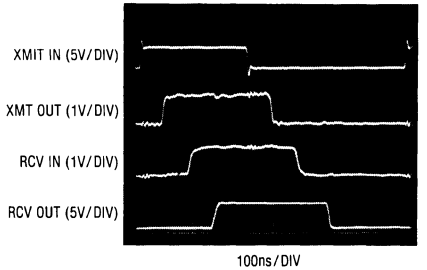
The LTC1045 is a hex level translator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. It consists of six high speed comparators with output latches and three-state capability. Each comparator's plus input is brought out separately. The minus inputs of comparators 1-4 are tied to V_{TRIP1} and 5-6 are tied to V_{TRIP2}.

The I_{SET} pin has several functions. When taken to V^+ the outputs are latched and power is completely shut off. Power/speed can be programmed by connecting I_{SET} to V^- through an external resistor.

LTCMOS™ is a trademark of Linear Technology Corp.

Flat Ribbon Cable Driver/Receiver



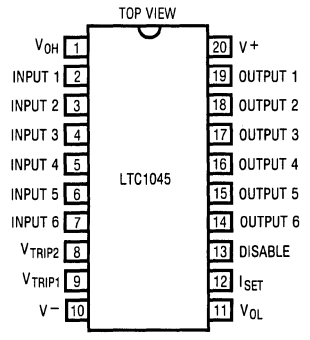


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Total Supply Voltage (V^+, V_{OH} to V^-, V_{OL}) 18V
Output High Voltage (V_{OH}) ..... $\leq V^+$
Input Voltage ..... 18V to V^- – 0.3V
Operating Temperature Range
LTC1045C ..... – 40°C to 85°C
LTC1045M ..... – 55°C to 125°C
Storage Temperature Range ..... – 55°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Output Short Circuit Duration
($V_{OH} – V_{OL} \leq 10V$) ..... Continuous
ESD (MIL-STD-883, Method 3015.1) 2000V

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1045MJ LTC1045CJ LTC1045CN

ELECTRICAL CHARACTERISTICS

(Note 3) $V^+ = V_{OH} = 5V$, $V^- = V_{OL} = 0V$, $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1045M MIN	LTC1045M TYP	LTC1045M MAX	LTC1045C MIN	LTC1045C TYP	LTC1045C MAX	UNITS
I_B	Input Bias Current	$V^- \leq V_{IN} \leq V^+$			±1			±1		nA
			•			1.0			0.5	μA
	Trip Voltage Range (Pin 8 and Pin 9)		•	V^-		$V^+ – 2$	V^-		$V^+ – 2$	V
I_S	V^+ to V^- Supply Current	DISABLE = V^+, R_{SET} = 10k			2.5	3.5		2.5	3.5	mA
			•			5.0			4.5	mA
I_{OFF}	V^+ to V^- Supply Current in Shutdown	DISABLE = $I_{SET} = V^+$			10			10		nA
			•			5			1	μA
V_{REF}	Voltage on I_{SET} (Pin 12)	R_{SET} = 10k			0.9			0.9		V
			•	0.5		1.4	0.6		1.25	V
V_{OH}	TTL Output High Voltage	$I_{OUT} = -360\mu A$, $V^+ = 4.5V$	•	2.4	4.4		2.4	4.4		V
V_{OL}	TTL Output Low Voltage	$I_{OUT} = 1.6mA$, $V^+ = 4.5V$	•		0.2	0.4		0.2	0.4	V
I_{SINK}	Output Short Circuit Sink Current	$V_{IN} = V_{TRIP} – 100mV$, $V_{OUT} = V^+$		8.5	15		7.5	15		mA
			•	5.5			5.5			mA
I_{SOURCE}	Output Short Circuit Source Current	$V_{IN} = V_{TRIP} + 100mV$, $V_{OUT} = V^-$		4.5	8.0		4.0	8.0		mA
			•	3.2			3.2			mA
I_{OZ}	Three-State Leakage Current	DISABLE = V^+			0.005			0.005		μA
		$V_{OL} \leq V_{OUT} \leq V_{OH}$	•			1			1	μA
R_{OH}	Output Resistance to V_{OH}	$\lvert I_{OUT} \rvert \leq 100\mu A$			260	400		260	475	Ω
			•			600			600	Ω
R_{OL}	Output Resistance to V_{OL}	$\lvert I_{OUT} \rvert \leq 100\mu A$			100	150		100	180	Ω
			•			250			250	Ω
	I_{SET} Voltage for Shutdown		•	$V^+ – 0.5$			$V^+ – 0.5$			V
V_{IH}	DISABLE Input Logic Levels	$V^+ = 4.5V$, $V^- = 0V$	•	2.0			2.0			V
V_{IL}		$V^+ = 5.5V$, $V^- = 0V$	•			0.8			0.8	V
	Input Supply Differential ($V^+ – V^-$) (Note 3)		•	4.5		15	4.5		15	V
	Output Supply Differential ($V_{OH} – V_{OL}$) (Note 3)		•	3		15	3		15	V

AC ELECTRICAL CHARACTERISTICS

$V^+ = V_{OH} = 5V, V^- = V_{OL} = 0V, T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1045M MIN	LTC1045M TYP	LTC1045M MAX	LTC1045C MIN	LTC1045C TYP	LTC1045C MAX	UNITS
t_d	Response Time	Test Circuit Figure 1 R_{SET} = 10k, ±100mV Drive	 ●			200 350			250 350	ns ns
t_{SETUP}	Time Before Rising Edge of I_{SET} that Data Must be Present	Test Circuit Figure 2			80			80		ns
t_{HOLD}	Time After Rising Edge of I_{SET} that Data Must be Present	Test Circuit Figure 2			0			0		ns
t_{ACC}	Falling Edge of DISABLE to Logic Level (from Hi-Z State)	Test Circuit Figure 3			165			165		ns
t_{IH}, t_{OH}	Rising Edge of DISABLE to Hi-Z State	Test Circuit Figure 3			200			200		ns

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The maximum differential voltage between any two power pins (V^+, V^-, V_{OH} and V_{OL}) must not exceed 18V. The maximum recommended operating differential is 15V.

Note 3: During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause a supply differential to exceed the absolute maximum rating.

TEST CIRCUITS

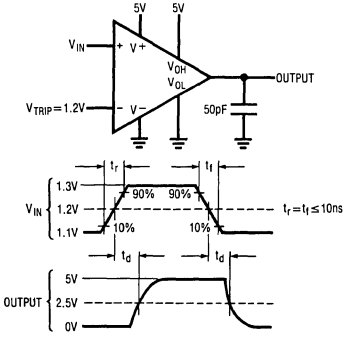


Figure 1. Response Time Test Circuit

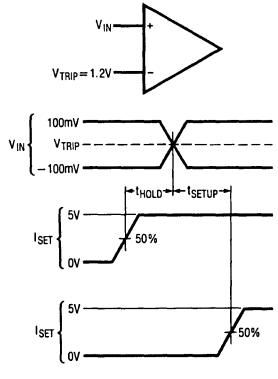


Figure 2. Latch Test Circuit

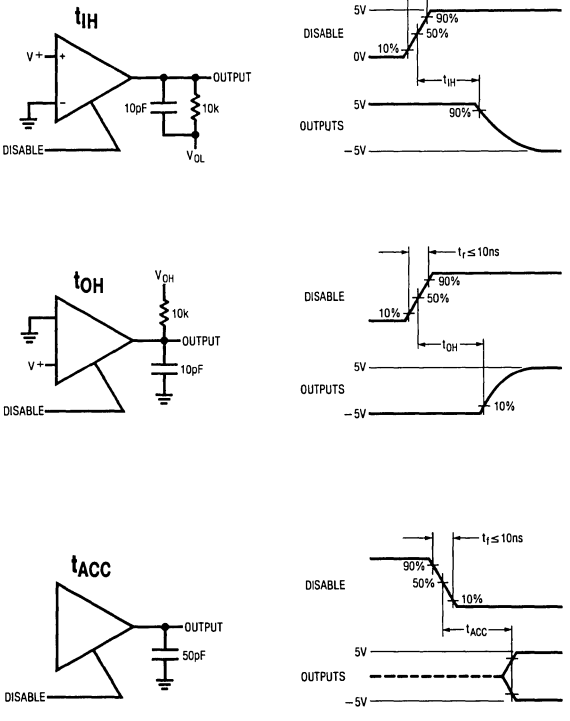
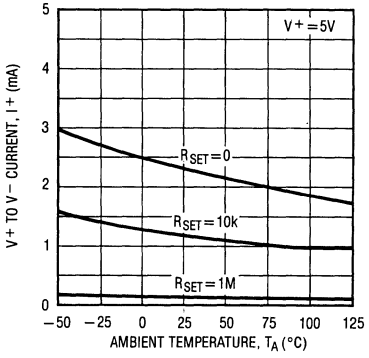


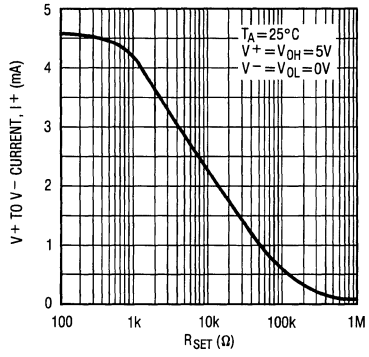
Figure 3. Three-State Output Test Circuit, Conditions: $V^+ = 5V, V^- = 0V, V_{OH} = 5V, V_{OL} = 0V$

TYPICAL PERFORMANCE CHARACTERISTICS

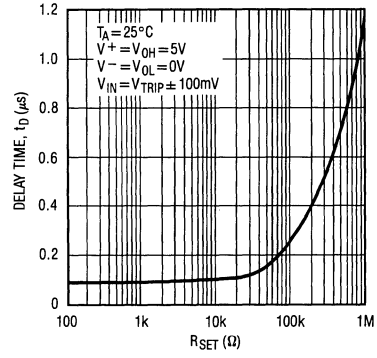
I⁺ vs Temperature



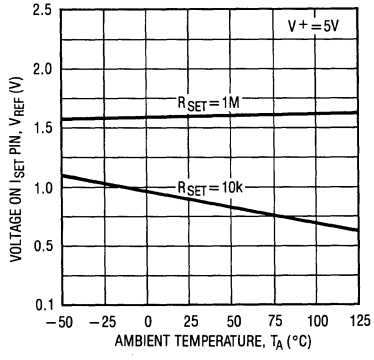
I⁺ vs R_{SET}



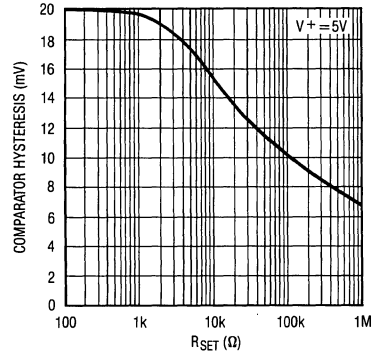
Delay Time vs R_{SET}



V_{REF} vs Temperature



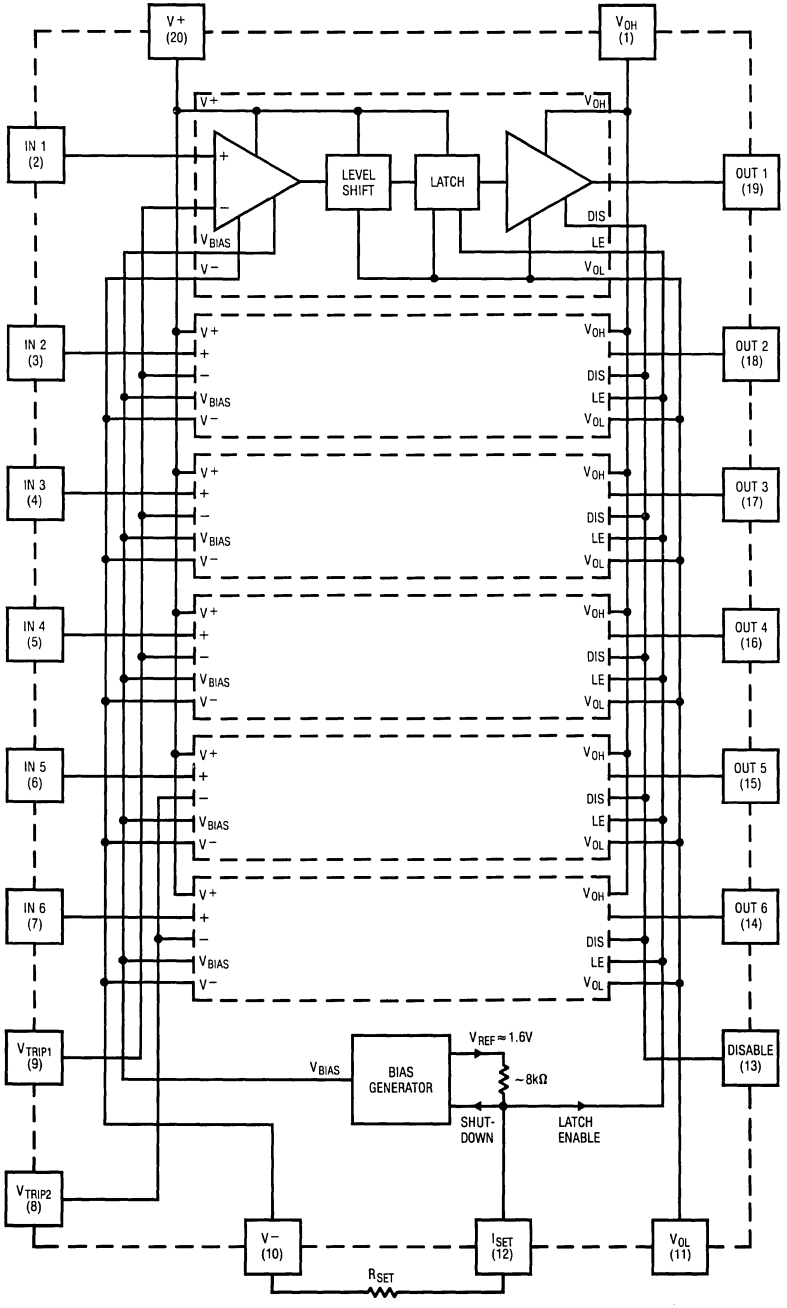
Hysteresis vs R_{SET}



PIN DESCRIPTION

Pin	Name	Description
1	V_{OH}	High level to which the output switches
2-7	INPUT	Six comparator inputs; voltage range = V^- to V^- + 18V
8	V_{TRIP1}	Trip point for first four comparators (inputs 1-4); voltage range = V^- to V^+ – 2V
9	V_{TRIP2}	Trip point for last two comparators (inputs 5-6); voltage range = V^- to V^+ – 2V
10	V^-	Low level to which the output switches
11	V_{OL}	Comparator negative supply
12	I_{SET}	This pin has three functions 1) R_{SET} from this pin to V^- sets bias current 2) When forced to V^+ power is shut off completely 3) When forced to V^+ outputs are latched
13	DISABLE	When high outputs are Hi-Z
14-19	OUTPUT	Six driver outputs
20	V^+	Comparator positive supply

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC1045 consists of six voltage translators and associated control circuitry, see Block Diagram. Each translator has a linear comparator input stage with the positive input brought out separately. The negative inputs of the first four comparators are tied in common to V_{TRIP1} and the negative inputs of the last two comparators are tied in common to V_{TRIP2}. With these inputs the switching point of the comparators can be set anywhere within the common-mode range of V^- to $V^+ - 2V$. To improve noise immunity each comparator has a small built-in hysteresis. Hysteresis varies with bias current from 7mV at low bias current to 20mV at high bias current (see typical curve of Hysteresis vs R_{SET}).

Setting the Bias Current

Unlike CMOS logic, any linear CMOS circuit must draw some quiescent current. The bias generator (Block Diagram) allows the quiescent current of the comparators to be varied. Bias current is programmed with an external resistor (see typical curve of I^+ vs R_{SET}). As the bias current is decreased, the LTC1045 slows down (see typical curve of Delay Time vs R_{SET}).

Shutting Power Off and Latching the Outputs

In addition to setting the bias current, the I_{SET} pin shuts power completely off and latches the translator outputs. To do this, the I_{SET} pin must be forced to $V^+ - 0.5V$. As shown in Figure 4, a CMOS gate or a TTL gate with a resistor pull-up does this quite nicely. Even though power is turned off to the linear circuitry, the CMOS output logic is powered and maintains the output state. With no DC load on the output, power dissipation, for all practical purposes, is zero.

Latching the output is fast—typically 80ns from the rising edge of I_{SET}. Going from the latched to flow through state is much slower—typically 1.5μs from the falling edge of I_{SET}. This time is set by the comparator's power up time. During the power up time, the output can assume false states. To avoid problems, the output should not be considered valid until 2μs to 5μs after the falling edge of I_{SET}.

Putting the Outputs in Hi-Z State

A DISABLE input sets the six outputs to a high impedance state. This allows the LTC1045 to be interfaced to a data bus. When DISABLE = "1" the outputs are high impedance and when DISABLE = "0" they are active. With TTL supplies, $V^+ = 4.5V$ to 5.5V and $V^- = GND$, the DISABLE input is TTL compatible.

Power Supplies

There are four power supplies on the LTC1045: V^+, V^-, V_{OH} and V_{OL}. They can be connected almost arbitrarily, but there are a few restrictions. A minimum differential must exist between V^+ and V^- and V_{OH} and V_{OL}. The V^+ to V^- differential must be at least 4.5V and the V_{OH} to V_{OL} differential must be at least 3.0V. Another restriction is caused by the internal parasitic diode D1 (see Figure 5).

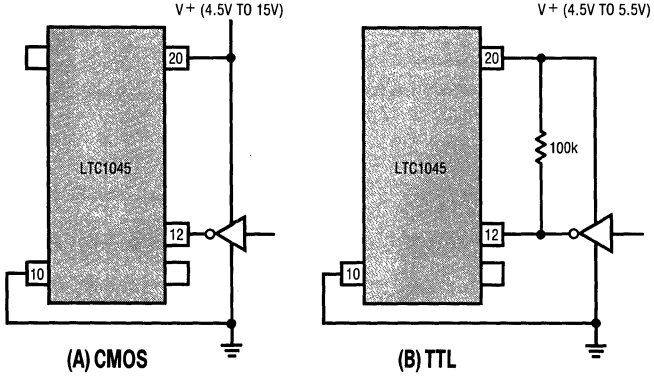


Figure 4. Driving the I_{SET} Pin with Logic

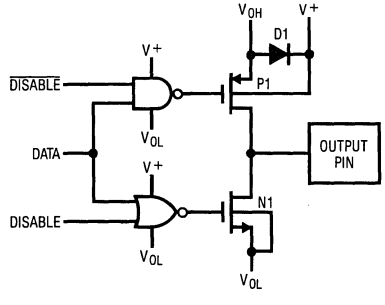


Figure 5. Output Driver

APPLICATIONS INFORMATION

Because of this diode, V_{OH} must not be greater than V^+. Lastly the maximum voltage between any two power supply pins must not exceed 15V operating or 18V absolute maximum. For example, if $V^+ = 5V$, V^- or V_{OL} should be no more negative than $-10V$. Note that V_{OL} should not be more negative than $-10V$ even if the V_{OH} to V_{OL} differential does not exceed the 15V maximum. In this case the V^+ to V_{OL} differential sets the limit.

Input Voltage

The LTC1045 has no upper clamp diodes as do conventional CMOS circuits. This allows the inputs to exceed the V^+ supply. The inputs will break down approximately 30V above the V^- supply. If the input current is limited with 100kΩ, the input voltage can be driven to at least ±50V with no adverse effects for any combination of allowed power supply voltages. Output levels will be correct even under these conditions (i.e., if the input voltage is above the trip point, the output will be high and if it is below, the output will be low).

Output Drive

Output drive characteristics of the LTC1045 will vary with the power supply voltages that are chosen. Output impedance is affected by V^+, V_{OH} and V_{OL}. V^- has no effect on output impedance. Guaranteed drive characteristics are specified in the table of electrical characteristics for $V^+ = V_{OH} = 5V$ and $V^- = V_{OL} = 0V$. Figures 6 and 7 show relative output impedance for other supply combinations. In general, output impedance is minimized if V^+ to V_{OH} is minimized and V_{OH} to V_{OL} is maximized.

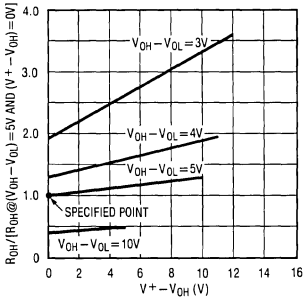


Figure 6. Relative Output Sourcing Resistance (R_{OH}) vs $V^+ - V_{OH}$

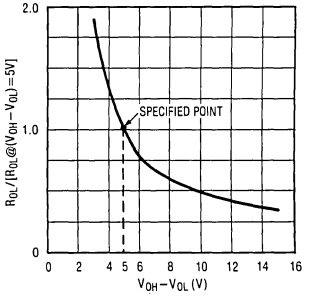
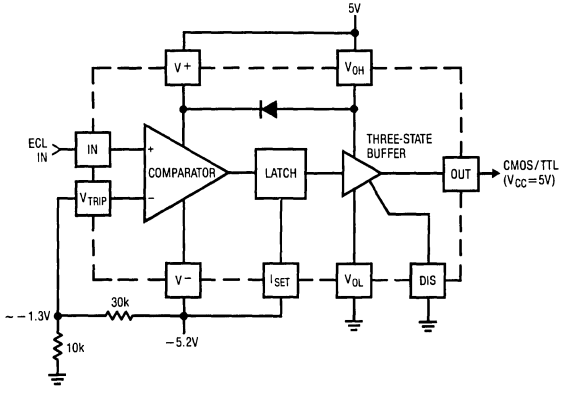


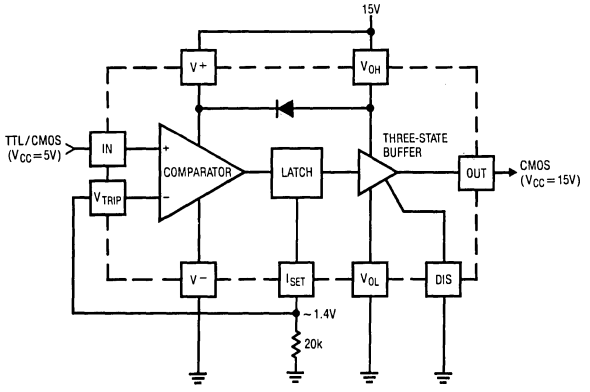
Figure 7. Relative Output Sinking Resistance (R_{OL}) vs $V_{OH} - V_{OL}$

TYPICAL APPLICATIONS

ECL to CMOS/TLL Logic

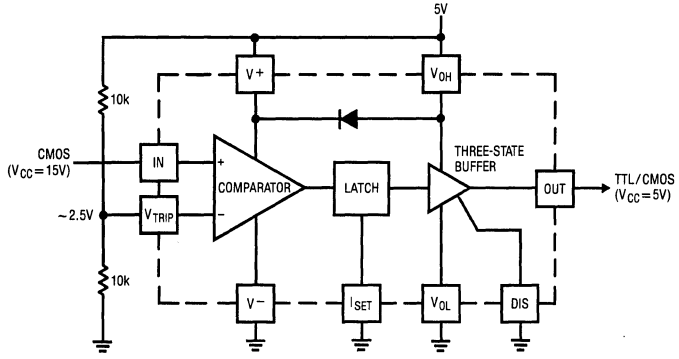


TTL/CMOS (V_{CC} = 5V) to High Voltage CMOS (V_{CC} = 15V)

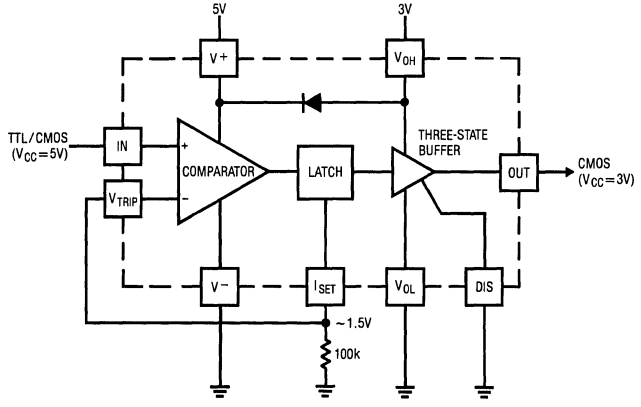


TYPICAL APPLICATIONS

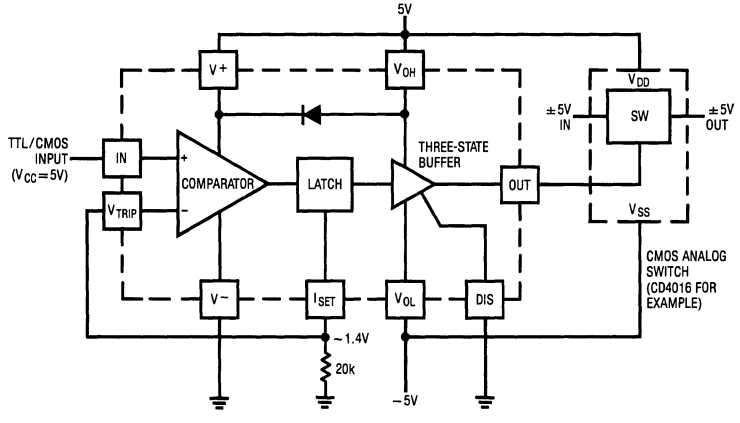
High Voltage CMOS (V_{CC} = 15V) to TTL/CMOS (V_{CC} = 5V)



TTL/CMOS (V_{CC} = 5V) to Low Voltage CMOS (V_{CC} = 3V)

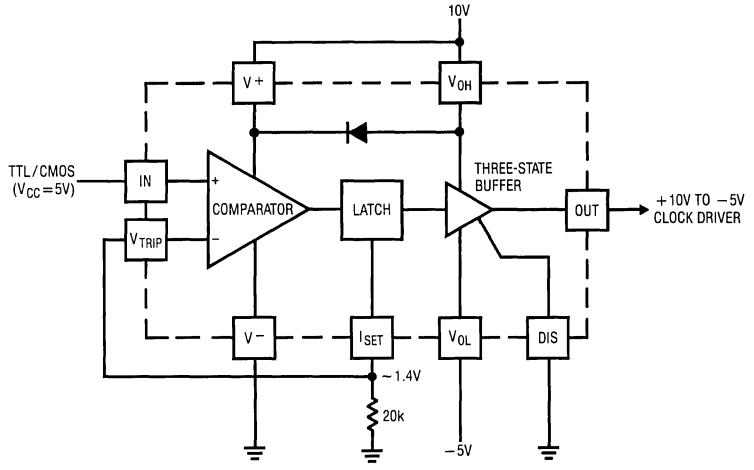


TTL/CMOS Logic Levels to ±5V Analog Switch Driver

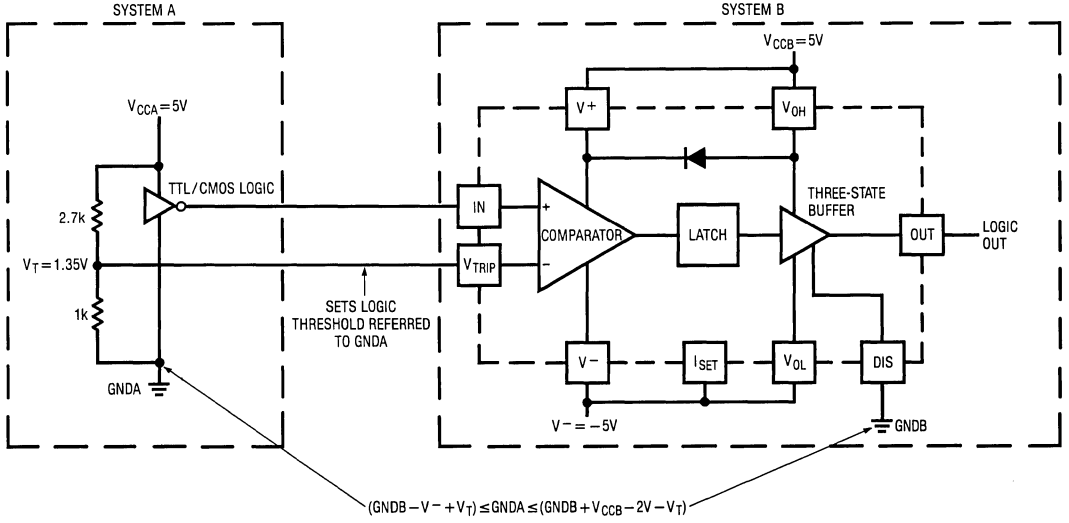


TYPICAL APPLICATIONS

TTL/CMOS (V_{CC} = 5V) to +10V/–5V Clock Driver

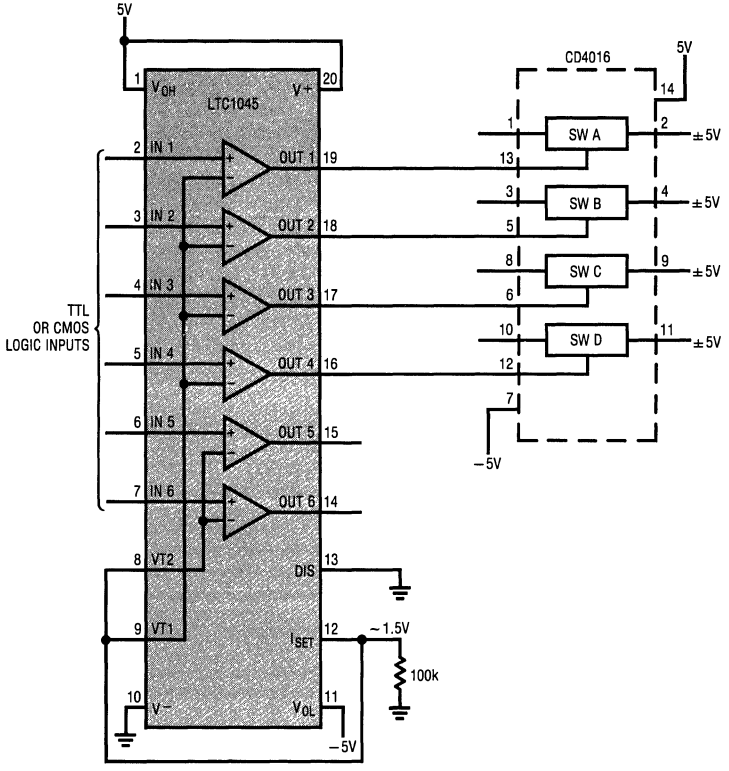


Logic Ground Isolation when Two Grounds are within LTC1045 Common-Mode Range

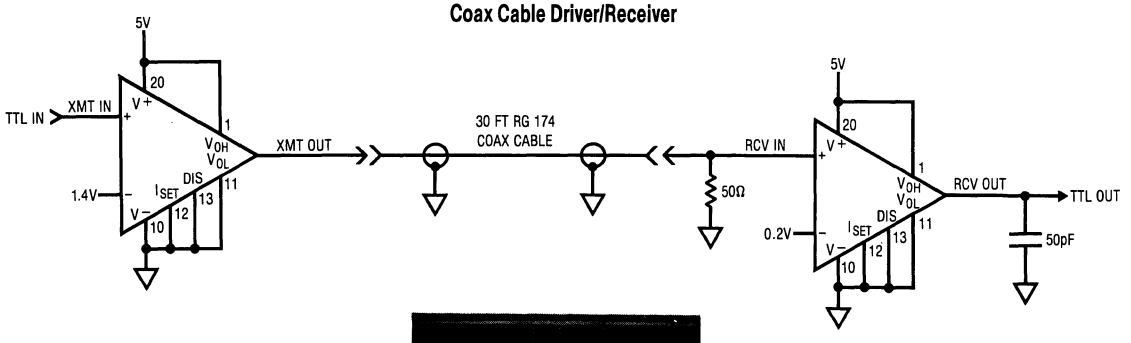


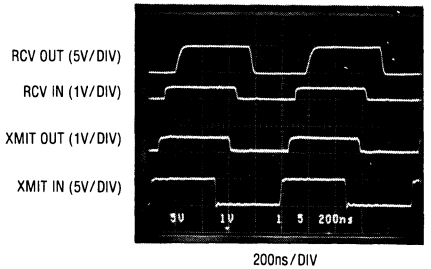
TYPICAL APPLICATIONS

±5V Analog Switch Driver



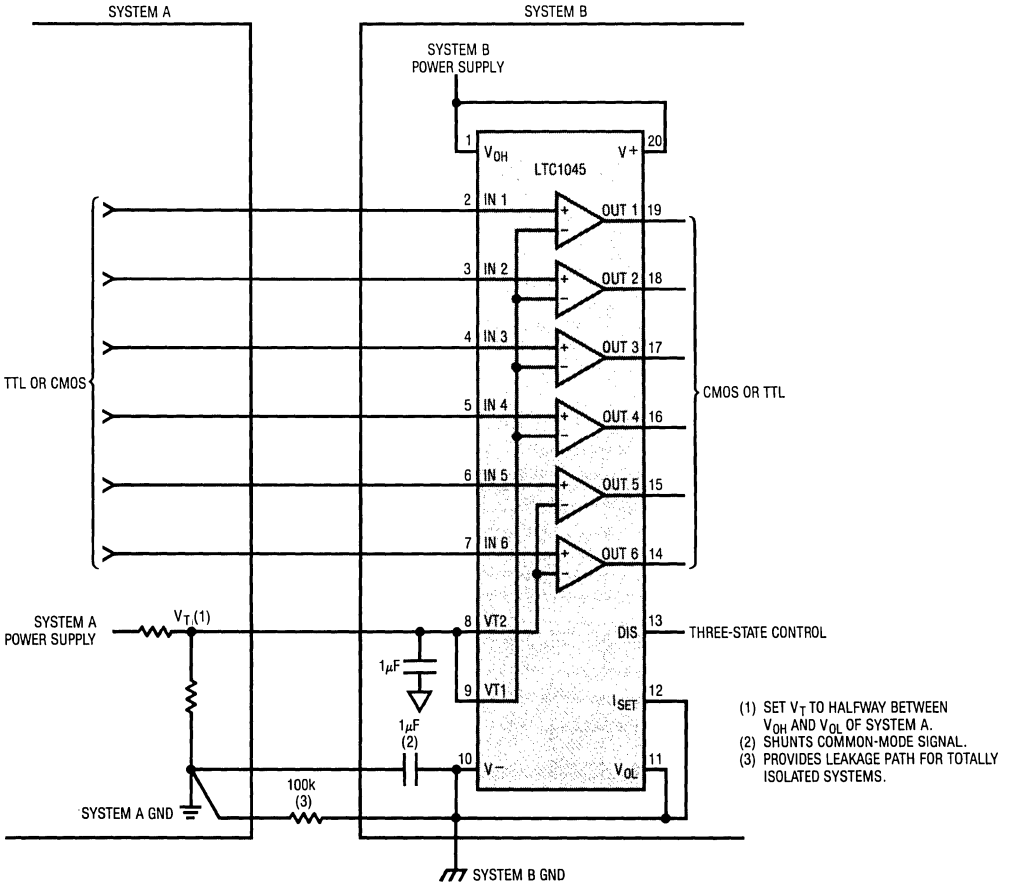
Coax Cable Driver/Receiver



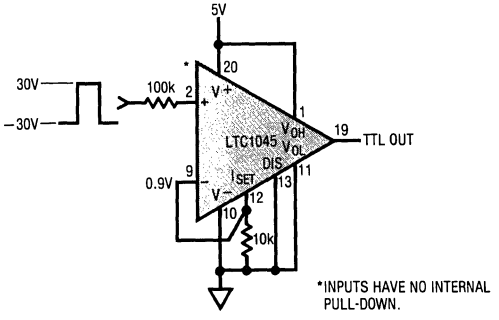


TYPICAL APPLICATIONS

Logic Systems DC Isolation

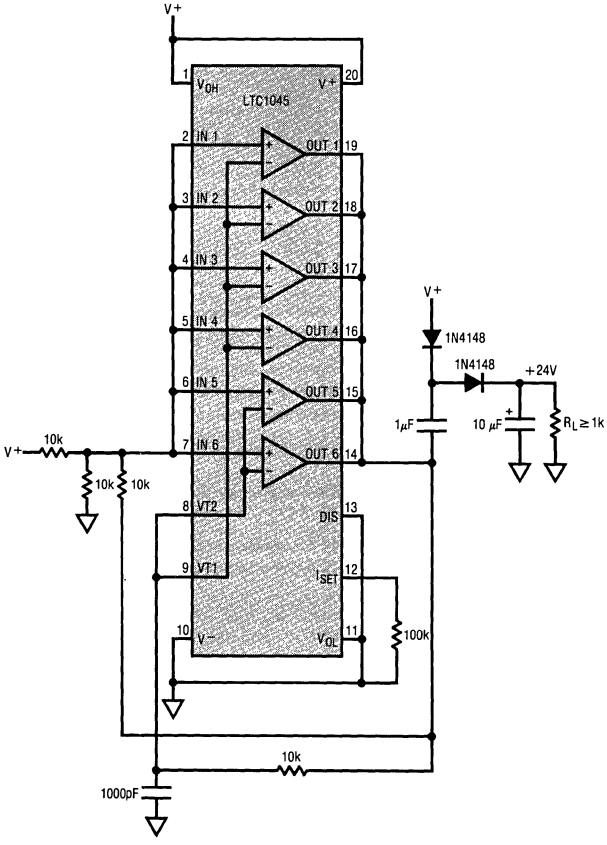


RS232 Receiver

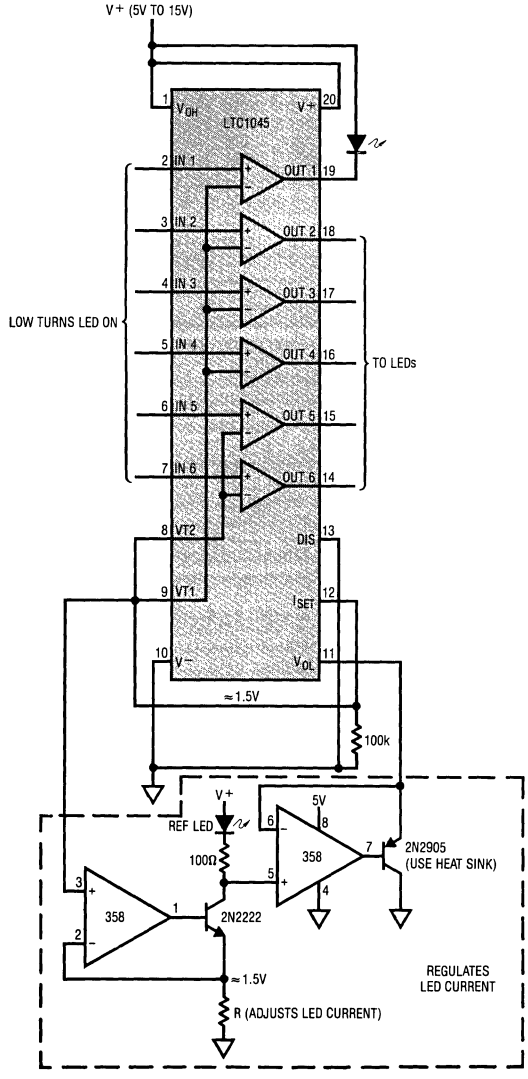


TYPICAL APPLICATIONS

24V Relay Supply from +12V/+15V Supply

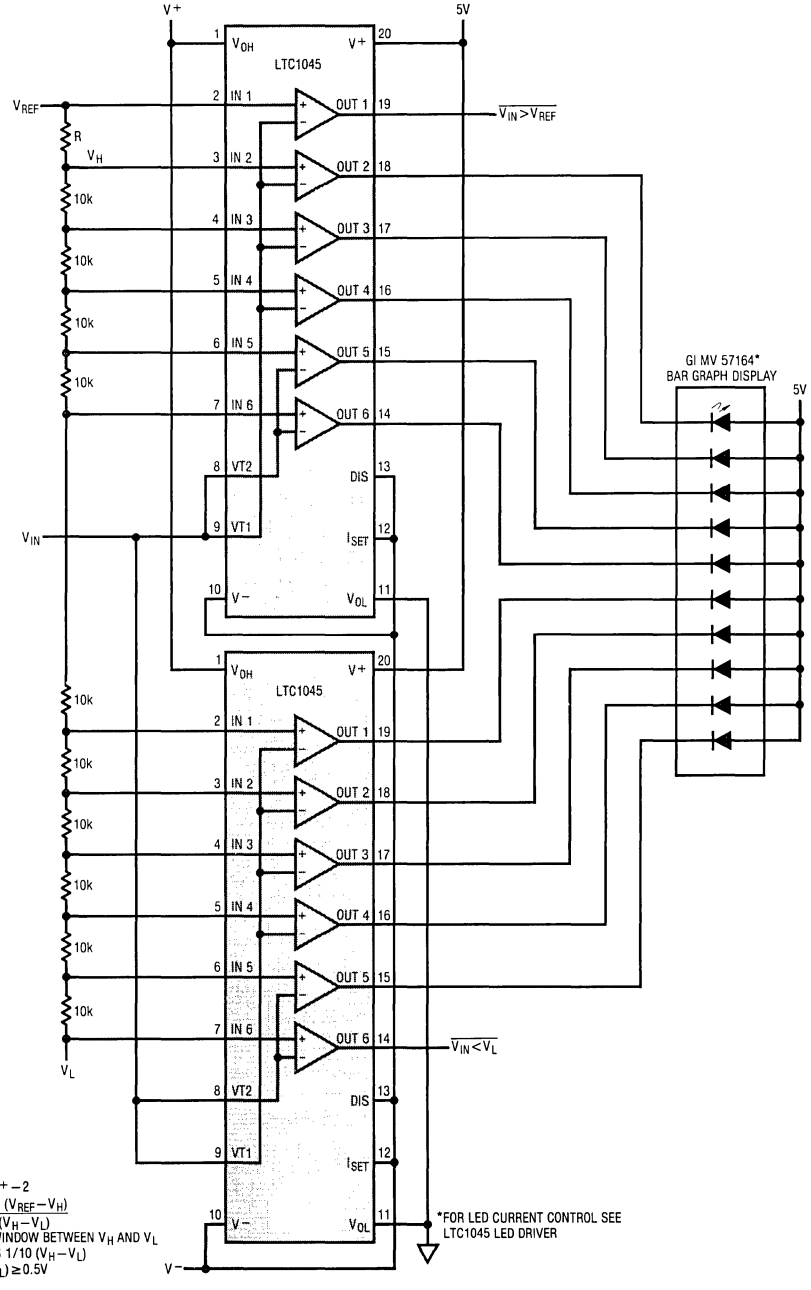


LED Driver



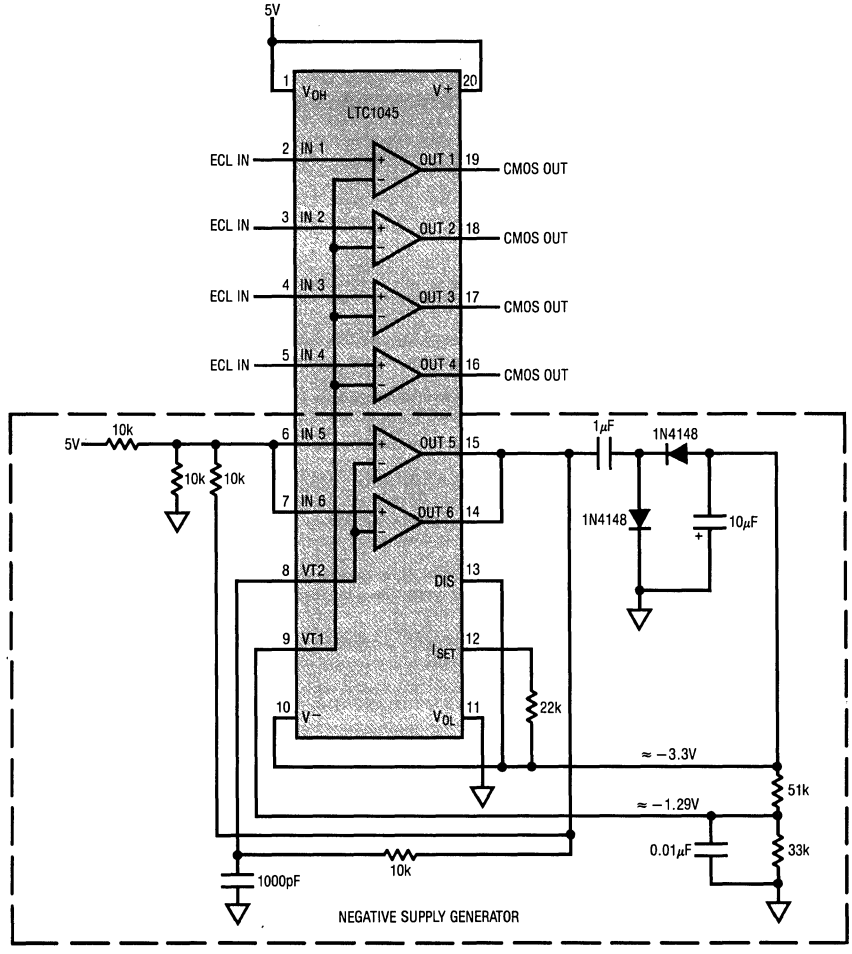
TYPICAL APPLICATIONS

Multi-Window Comparator and Display



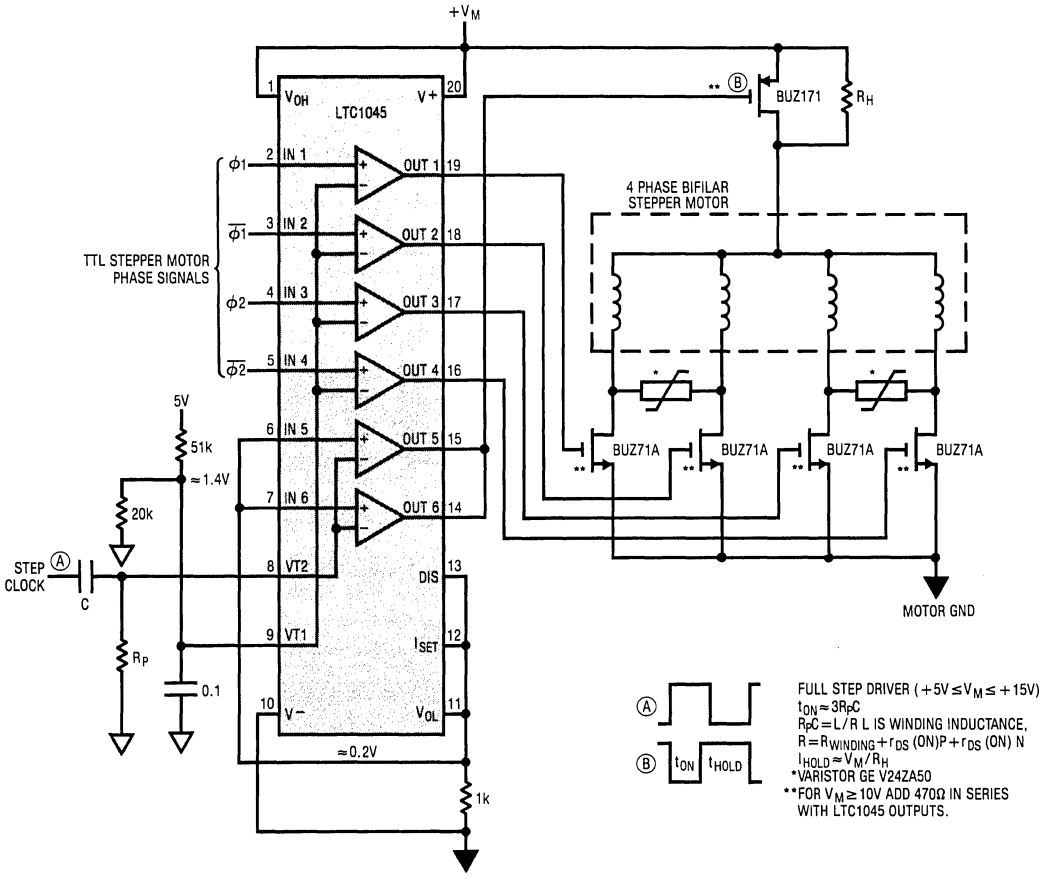
TYPICAL APPLICATIONS

ECL to CMOS from Single +5V Supply



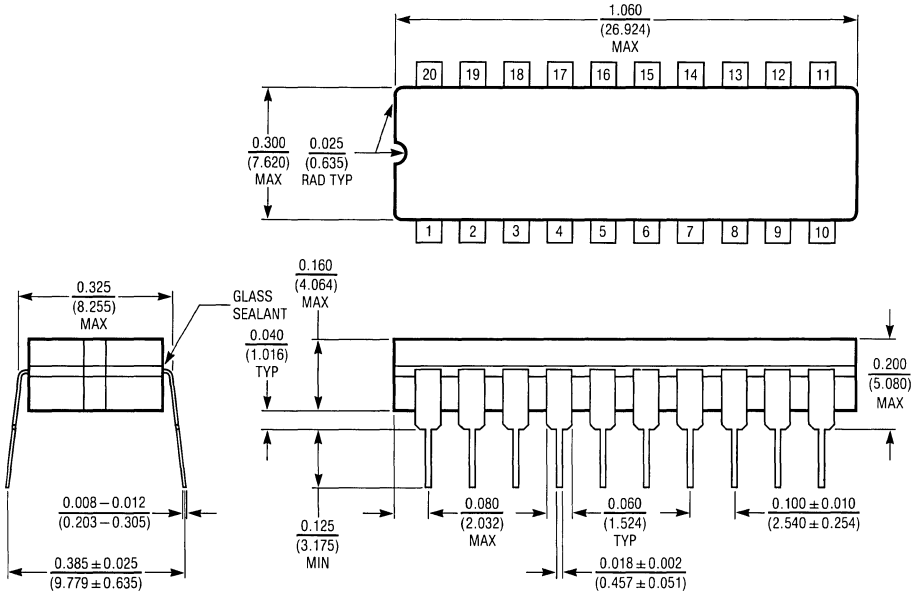
TYPICAL APPLICATIONS

Power MOSFET Driver Low Power Consumption Stepper Motor Driver



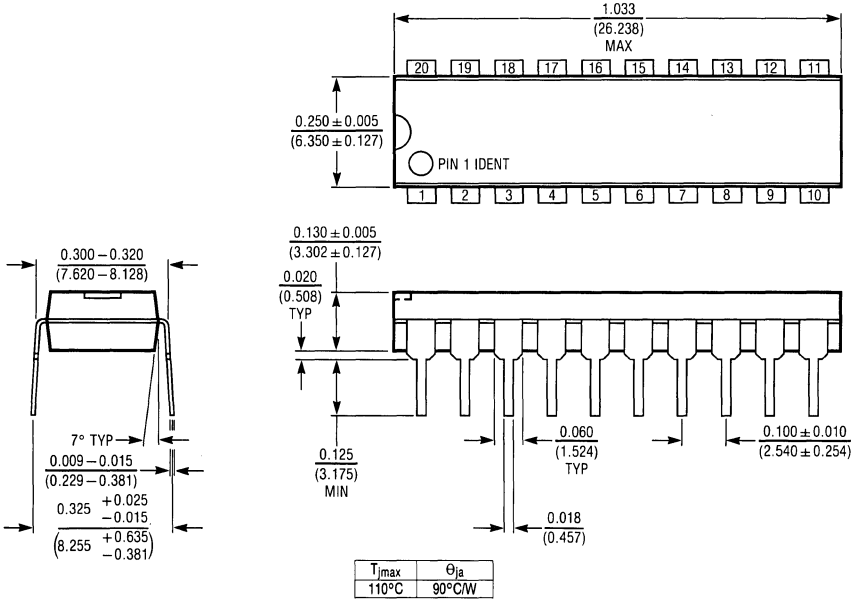
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J20 Package Ceramic DIP



T_{jmax}	θ_{ja}
150°C	70°C/W

N20 Package Molded DIP



T_{jmax}	θ_{ja}
110°C	90°C/W

SECTION 6—FILTERS

SECTION 6—FILTERS

High Performance Triple Universal Filter Building Block

FEATURES

- Up to 6th Order Filter Functions with a Single 20 Pin 0.3″ Wide Package
- Center Frequency Range up to 35kHz
- $f_0 \times Q$ Product Up to 1 MHz
- *Guaranteed* Center Frequency and Q Accuracy Over Temperature
- *Guaranteed* Low Offset Voltages Over Temperature
- 90dB Signal to Noise Ratio
- Filter Operates From Single 4.7V Supply and Up to ±8V Supplies
- *Guaranteed* Filter Specifications with ±5V Supply and ±2.37V Supply
- Low Power Consumption with Single 5V Supply
- Clock Inputs T^2L and CMOS Compatible

APPLICATIONS

- High Order, Wide Frequency Range Bandpass, Lowpass, Notch Filters
- Low Power Consumption, Single 5V Supply Clock Tunable Filters
- Tracking Filters
- Antialiasing Filters

LTCMOS™ is a trademark of Linear Technology Corp.

DESCRIPTION

The LTC1061 consists of three high performance, universal filter building blocks. Each filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce highpass or notch or allpass. The center frequency of these functions can be tuned with an external clock or an external clock and a resistor ratio. For Q<5, the center frequency ranges from 0.1Hz to 35kHz. For Q's of 10 or above, the center frequency ranges from 0.1Hz to 28kHz.

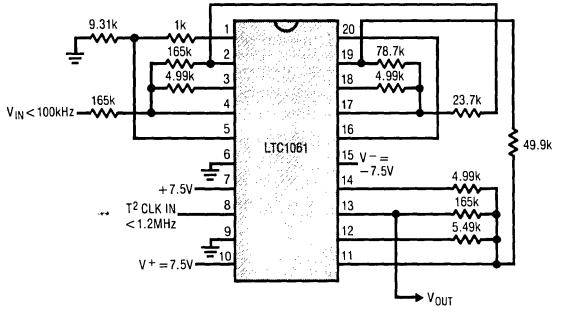
The LTC1061 can be used with single or dual supplies ranging from ±2.37V to ±8V (or 4.74V to 16V). When the filter operates with supplies of ±5V and above, it can handle input frequencies up to 100kHz.

The LTC1061 is compatible with the LTC1059 single universal filter and the LTC1060 dual. Higher than 6th order functions can be obtained by cascading the LTC1061 with the LTC1059 or LTC1060. Any classical filter realization can be obtained.

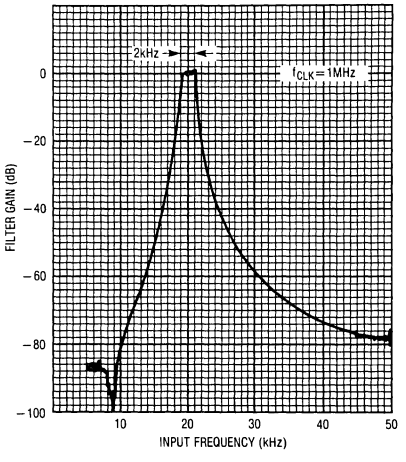
The LTC1061 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

TYPICAL APPLICATION

6th Order, Clock Tunable, 0.5dB Ripple Chebyshev BP Filter



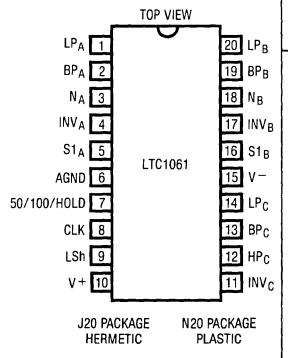
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Power Dissipation 500mW
Operating Temperature Range
LTC1061AC, LTC1061C ..... $-40°C \le T_A \le 85°C$
LTC1061AM, LTC1061M ..... $-55°C \le T_A \le 125°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1061AMJ, LTC1061MJ
LTC1061ACJ, LTC1061CJ
LTC1061ACN, LTC1061CN

(ALSO AVAILABLE IN SO PACKAGE)

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_0	$f_0 \times Q \le 175kHz$, Mode 1, $V_S = \pm 7.5V$			0.1-35k		Hz
	$f_0 \times Q \le 1.6MHz$, Mode 1, $V_S = \pm 7.5V$			0.1-25k		Hz
	$f_0 \times Q \le 75kHz$, Mode 3, $V_S = \pm 7.5V$			0.1-25k		Hz
	$f_0 \times Q \le 1MHz$, Mode 3, $V_S = \pm 7.5V$ (Note 1)			0.1-17k		Hz
Input Frequency Range				0-200k		Hz
Clock to Center Frequency Ratio, f_{CLK}/f_0						
LTC1061A	Sides A, B: Mode 1, R1 = R3 = 50kΩ	●			50 ± 0.6%	
LTC1061	R2 = 5kΩ, Q = 10, f_{CLK} = 250kHz Pin 7 High. Side C: Mode 3, R1 = R3 = 50k R2 = R4 = 5k, f_{CLK} = 250kHz	●			50 ± 1.2%	
LTC1061A	Same as Above, Pin 7 at	●			100 ± 0.6%	
LTC1061	Mid-Supplies, f_{CLK} = 500kHz	●			100 ± 1.2%	
Clock to Center Frequency Ratio, Side to Side Matching						
LTC1061A		●			0.6%	
LTC1061		●			1.2%	
Q Accuracy						
LTC1061A	Sides A, B, Mode 1	●		±2	3	%
LTC1061	Side C, Mode 3 $f_0 \times Q \le 50kHz$, $f_0 \le 5kHz$	●		±3	5	%
f_0 Temperature Coefficient	Mode 1, 50:1, $f_{CLK} < 300kHz$			±1		ppm/°C
Q Temperature Coefficient	Mode 1, 100:1, $f_{CLK} < 500kHz$			±5		ppm/°C
	Mode 3, $f_{CLK} < 500kHz$			±5		ppm/°C

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Offset Voltage						
V_{OS1}, Figure 23		●		2	15	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1	●		3	20	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1	●		6	40	mV
V_{OS3}	$f_{CLK} = 250kHz$, 50:1	●		3	20	mV
V_{OS3}	$f_{CLK} = 500kHz$, 100:1	●		6	40	mV
Clock Feedthrough	$f_{CLK} < 1MHz$			0.4		mV_{RMS}
Max. Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5V$			2.5		MHz
Power Supply Current			6	8	12	mA
		●			16	mA

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25°C$ unless otherwise specified

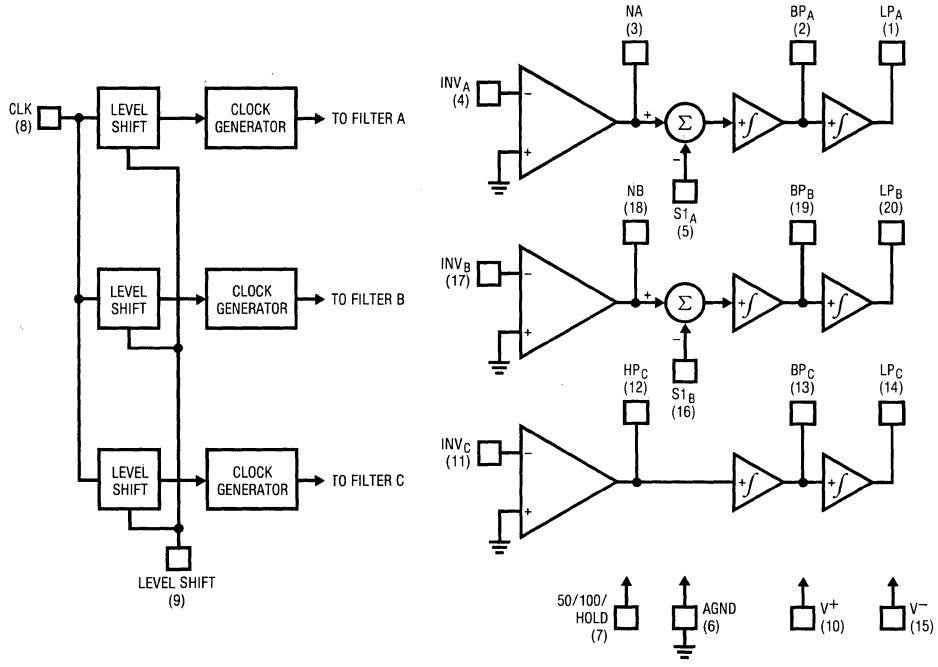
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 120kHz$, Mode 1, 50:1			0.1-12k		Hz
	$f_o \times Q \leq 120kHz$, Mode 3, 50:1			0.1-10k		Hz
Input Frequency Range				0-20k		Hz
Clock to Center Frequency Ratio	50:1, $f_{CLK} = 250kHz$, $Q = 10$					
LTC1061A	Sides A, B: Mode 1	●			50 ± 0.6%	
LTC1061	Side C: Mode 3			50 ± 1%		
LTC1061A	100: 1, $f_{CLK} = 500kHz$, $Q = 10$	●			100 ± 0.6%	
LTC1061	Sides A, B: Mode 1 Side C: Mode 3			100 ± 1%		
Q Accuracy						
LTC1061A	Same as Above			±2		%
LTC1061				±3		%
Max. Clock Frequency				700k		Hz
Power Supply Current				4.5	6	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			±2.37		±9	V
Voltage Swings						
LTC1061A	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 13, 14, 19, 20)		±4	±4.2		V
LTC1061	$R_L = 3.5k$ (Pins 3, 12, 18)		±3.8	±4.2		V
LTC1061, LTC1061A		●	±3.6			V
Output Short Circuit Current Source/Sink	$V_S = \pm 5V$			40/3		mA
DC Open Loop Gain	$V_S = \pm 5V$, $R_L = 5k$			80		dB
GBW Product	$V_S = \pm 5V$			3		MHz
Slew Rate	$V_S = \pm 5V$			7		V/μs

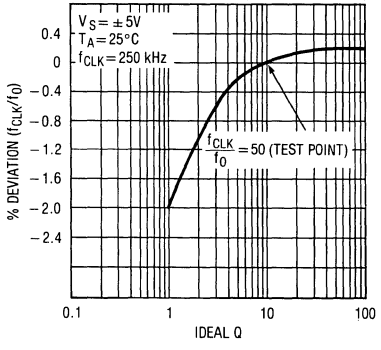
The ● denotes the specifications which apply over the full operating temperature range.

BLOCK DIAGRAM

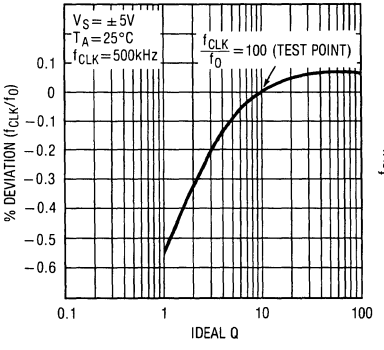


TYPICAL PERFORMANCE CHARACTERISTICS

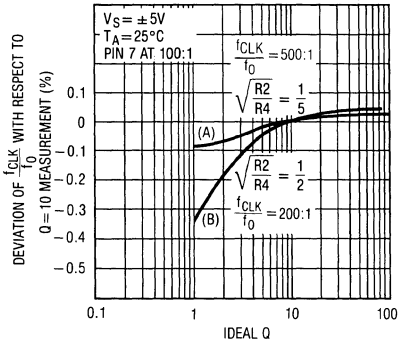
Graph 1. Mode 1, Mode 3 (f_{CLK}/f_o) Deviation vs Q



Graph 2. Mode 1, Mode 3 (f_{CLK}/f_o) Deviation vs Q

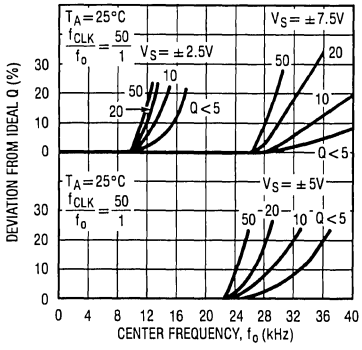


Graph 3. Mode 3: Deviation of (f_{CLK}/f_o) with Respect to Q = 10 Measurement

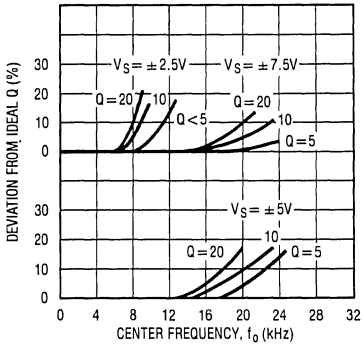


TYPICAL PERFORMANCE CHARACTERISTICS

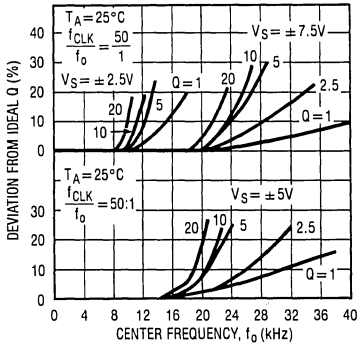
Graph 4. Mode 1: (f_{CLK}/f_o) = 50:1



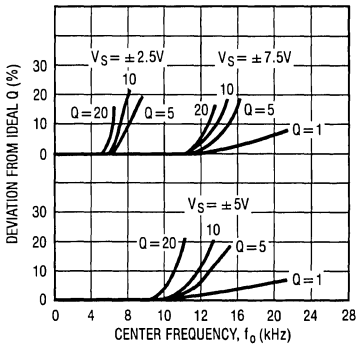
Graph 5. Mode 1: (f_{CLK}/f_o) = 100:1



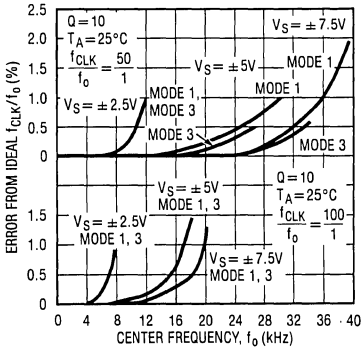
Graph 6. Mode 3: (f_{CLK}/f_o) = 50:1



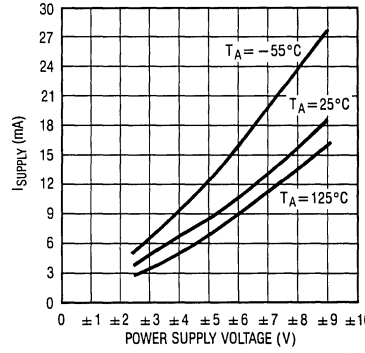
Graph 7. Mode 3: (f_{CLK}/f_o) = 100:1



Graph 8. f_{CLK}/f_o vs f_o



Graph 9. Power Supply Current vs Supply Voltage



PIN DESCRIPTION AND APPLICATION HINTS

Power Supplies (Pins 10, 15)

They should be bypassed with 0.1μF disc ceramic. Low noise, non-switching, power supplies are recommended. The device operates with a single 5V supply, Figure 1, and with dual supplies. The absolute maximum operating power supply voltage is ±9V.

Clock and Level Shift (Pins 8, 9)

When the LTC1061 operates with symmetrical dual supplies the level shift Pin 9 should be tied to analog ground. For single 5V supply operation the level shift pin should be tied to Pin 15 which will be the system ground. The typical logic threshold levels of the clock pin are as follows: 1.65V above the level shift pin for ±5V supply operation, 1.75V for ±7.5V and above, and 1.4V for single 5V supply operation. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 300ns. The maximum clock frequency for ±5V supplies and above is 2.4MHz.

PIN DESCRIPTION AND APPLICATION HINTS

$S1_A$, $S1_B$ (Pins 5, 16)

These are voltage input pins. If used, they should be driven with a source impedance below 5kΩ. When they are not used, they should be tied to the analog ground Pin 6.

AGND (Pin 6)

When the LTC1061 operates with dual supplies, Pin 6 should be tied to system ground. When the LTC1061 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply, Figure 1. The positive input of all the internal op amps, as well as the common reference of all the internal switches, are internally tied to the analog ground pin. Because of this, a "clean" ground is recommended.

50/100/Hold (Pin 7)

By tying Pin 7 to V^+, the filter operates with a clock to center frequency internally set at 50:1. When Pin 7 is at mid-supplies, the filter operates with a 100:1 clock to center frequency ratio. Table 1 shows the allowable variation of the potential at Pin 7 when the 100:1 mode is sought. When Pin 7 is shorted to the negative supply pin, the filter operation is stopped and the bandpass and lowpass output act as a sample and hold circuit holding the last sample of the input voltage. The hold step is around 2mV and the droop rate is 150μV/sec.

Table 1

Total Power Supply	Voltage Range of Pin 7 for 100:1 Operation
5V	2.5V ± 0.5V
10V	5V ± 1V
15V	7.5V ± 1.5V

Clock Feedthrough

This is defined as the amplitude of the clock frequency appearing at the output pins of the device, Figure 2. Clock feedthrough is measured with all three sides of the LTC1061 connected as filters. The clock feedthrough mainly depends on the magnitude of the power supplies and it is independent from the input clock levels, clock frequency and modes of operation.

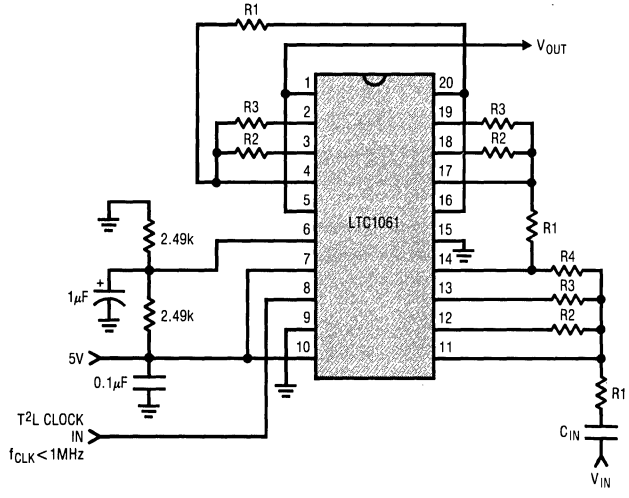


Figure 1. The 6th order LP Butterworth Filter of Figure 5 Operating with a Single 5V Supply.

PIN DESCRIPTION AND APPLICATION HINTS

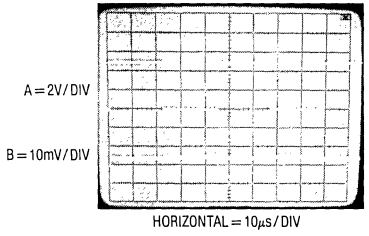


Figure 2. Typical Clock Feedthrough of the LTC1061 Operating with ±5V Supplies. Top Trace is the Input Clock Swinging 0-5V and Bottom Trace is One of the Lowpass Outputs with Zero or DC Input Signals.

Table 2 illustrates the typical clock feedthrough numbers for various power supplies.

Table 2

Power Supply	Clock Feedthrough
±2.5V	$0.2mV_{RMS}$
±5V	$0.4mV_{RMS}$
±8V	$0.8mV_{RMS}$

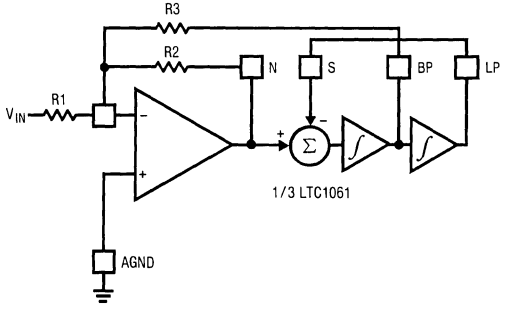
Definition of Filter Functions

Refer to LTC1060 datasheet.

MODES OF OPERATION

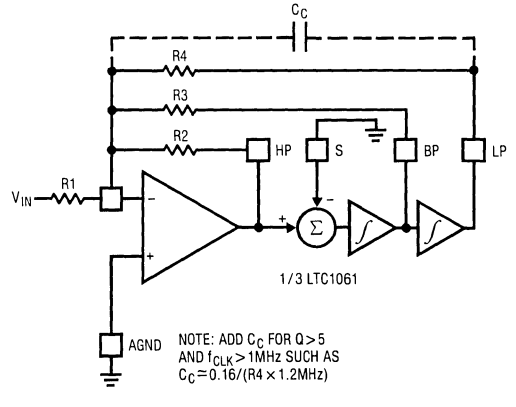
Description and Applications

1. Primary Modes: There are two basic modes of operation, Mode 1 and Mode 3. In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 50:1 or 100:1. In Mode 3, this ratio can be adjusted above or below 50:1 or 100:1. The side C of the LTC1061 can be connected only in Mode 3. Figure 3 illustrates Mode 1 providing 2nd order notch, lowpass, and bandpass outputs (for definition of filter functions refer to the LTC1060 datasheet). Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency and with unity gain. Mode 3, Figure 4, is the classical state variable configuration providing highpass, bandpass and lowpass second order filter functions.



$$f_o = \frac{f_{CLK}}{100(50)};\ f_n = f_o;\ H_{OLP} = -\frac{R2}{R1};\ H_{OBP} = -\frac{R3}{R1};\ H_{ON1} = -\frac{R2}{R1}\quad Q = \frac{R3}{R2}$$

Figure 3. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass.



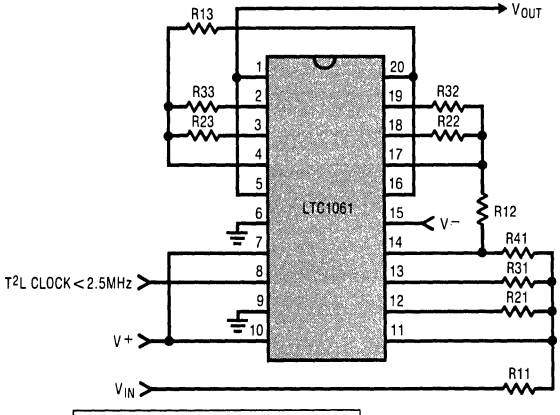
$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}};\ H_{OHP} = -R2/R1;\ H_{OBP} = -R3/R1;\ H_{OLP} = -R4/R1$$

Figure 4. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass.

MODES OF OPERATION

Since the input amplifier is within the resonant loop, its phase shift affects the high frequency operation of the filter and therefore, Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass, highpass and notch filters. Mode 3 as well as Mode 1 is a straightforward mode to use and the filter's dynamics can easily be optimized. Figure 5 illustrates a 6th order lowpass Butterworth filter operating with up to 40kHz cutoff frequency and with up to 200kHz input frequency. Sides A, B are connected in Mode 1 while side C is connected in Mode 3. The lower Q section was placed in side C, Mode 3, to eliminate any early Q enhancement. This could happen when the clock approaches 2MHz. The measured frequency response is shown in Figure 6. The attenuation floor is limited by the crosstalk between the three different sections operating with a clock frequency above 1MHz. The measured wideband noise was $150\mu V_{RMS}$. For limited temperature range the filter of Figure 5 works up to 2.5MHz clock frequency thus yielding a 50kHz cutoff.

2. Secondary Modes: Mode 1b—It is derived from Mode 1. In Mode 1b, Figure 7, two additional resistors, R5 and R6, are added to attenuate the amount of voltage fed back from the lowpass output into the input of the S_A (S_B) switched capacitor summer. This allows the filter clock to center frequency ratio to be adjusted beyond 50:1 (or 100:1). Mode 1b still maintains the speed advantages of Mode 1. Figure 8 shows the 3 lowpass sections of the LTC1061 in cascade resulting in a Chebyshev lowpass filter. The side A of the IC is connected in Mode 1b to provide the first resonant frequency below the cutoff frequency of the filter. The practical ripple, obtained by using a non-A version of the LTC1061 and 1% standard resistor values, was 0.15dB. For this 6th order lowpass, the textbook Q's and center frequencies normalized to the ripple bandwidth are: $Q1 = 0.55$, $f_o1 = 0.71$, $Q2 = 1.03$, $f_o2 = 0.969$, $Q3 = 3.4$, $f_o3 = 1.17$. The design was done with speed in mind. The higher (Q3, f_o3) section was in Mode 1 and placed in the side B of the LTC1061. The remaining two center frequencies were then normalized with respect to the center frequency of side B; this changes the ratio of clock to cutoff frequency from 50:1 to $50 \times 1.17 = 58.5:1$. As shown in Figure 9, the maximum cutoff frequency is about 33kHz. The total wideband output noise is $220\mu V_{RMS}$ and the measured output DC offset voltage is 60mV. Another example of Mode 1b is illustrated on the front page of the datasheet. The cascading sequence of this 6th order bandpass filter is shown in block diagram form, Figure 10A. The filter is geometrically centered around the



HARMONIC DISTORTION WITH $f_{CLK} = 2MHz$	
f_{IN}	2ND HARMONIC
10kHz, $1V_{RMS}$	–74dB
20kHz, $1V_{RMS}$	–62dB
30kHz, $1V_{RMS}$	–62dB
40kHz, $1V_{RMS}$	–62dB

STANDARD 1% RESISTOR VALUES

R11 = 20k	R21 = 20k
R31 = 11k	R41 = 20k
R12 = 20k	R22 = 20k
R32 = 14k	R23 = 10k
R13 = 10k	R33 = 17.8k

Figure 5. 6th Order Butterworth Lowpass Filter with Cutoff Frequency up to 45kHz.

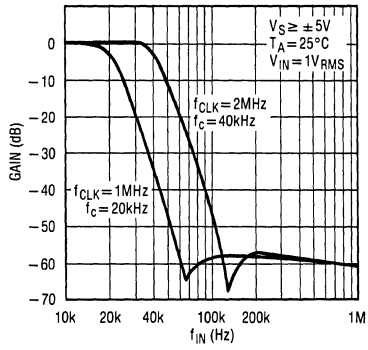
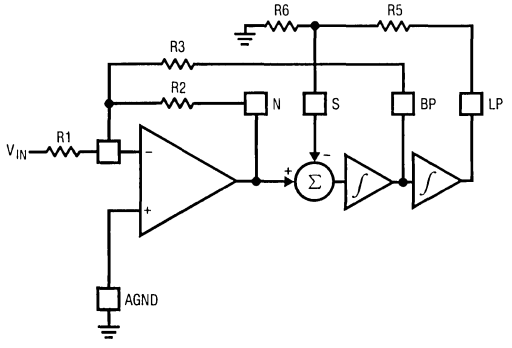


Figure 6. Measures Frequency Response of the Lowpass Butterworth Filter of Figure 3.

MODES OF OPERATION

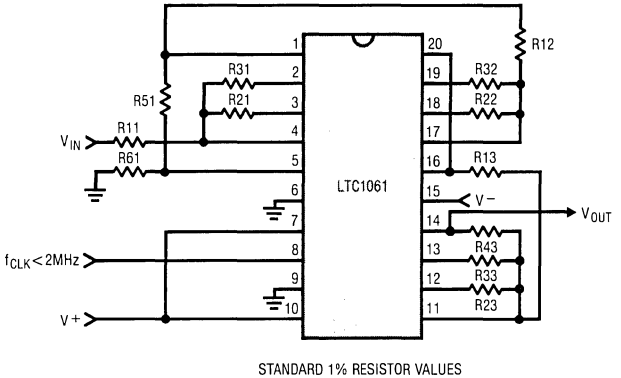
side B of the LTC1061 connected in Mode 1. This dictates a clock to center frequency ratio of 50:1 or 100:1. The side A of the IC operates in Mode 1b to provide the lower center frequency of 0.95 and still share the same clock with the rest of the filter. With this approach the bandpass filter can operate with center frequencies up to 24kHz. The speed of the filter could be further improved by using Mode 1 to lock the higher resonant frequency of 1.05 and higher Q of 31.9 to the clock, Figure 10B, thus changing the clock to center frequency ratio to 52.6:1.



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}};\ f_n = f_o;\ Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}};$$

$$H_{ON1}(f \rightarrow 0) = H_{ON2}\left(f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1};\ H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)};\ H_{OBP} = -\frac{R3}{R1};\ (R5//R6) < 5k\Omega$$

Figure 7. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass.



STANDARD 1% RESISTOR VALUES

R11 = 35.7k	R33 = 13k
R31 = 11.5k	R21 = 12.1k
R51 = 5.49k	R61 = 2.87k
R12 = 11k	R22 = 11k
R32 = 36.5k	R23 = 10.5k
R13 = 15.8k	R43 = 15.8k

Figure 8. 6th Order Chebyshev, Lowpass Filter using 3 Different Modes of Operation for Speed Optimization.

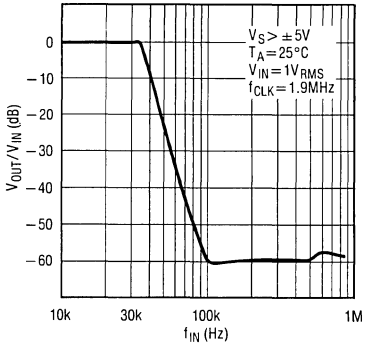


Figure 9. Amplitude Response of the 6th Order Chebyshev Lowpass Filter of Figure 8.

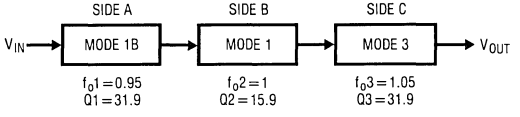


Figure 10A. Cascading Sequence of the Bandpass Filter Shown on the Front Page, with (f_{CLK}/f_o) = 50:1 or 100:1.

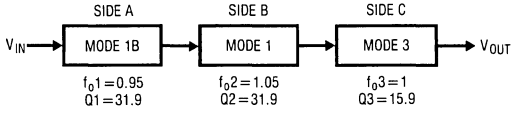
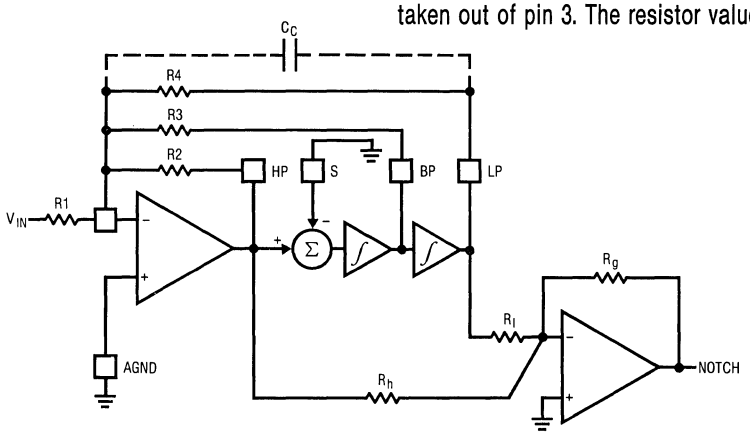


Figure 10B. Cascading Sequence of the Same Filter for Speed Optimization, and with (f_{CLK}/f_o) = 52.6:1.

MODES OF OPERATION

Mode 3a—This is an extension of Mode 3 where the highpass and lowpass outputs are summed through two external resistors R_h and R_l to create a notch, Figure 11. Mode 3a is very versatile because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 11 is not always required. When cascading the sections of the LTC1061, the highpass and lowpass outputs can be summed directly into the inverting input of the next section. Figure 12 shows an LTC1061 providing a 6th order elliptic bandpass or notch response. Sides C and B are connected in Mode 3a while side A is connected in Mode 1 and uses only two resistors. The resulting filter response is then geometrically symmetrical around either the center frequency of side A (for bandpass responses) or the notch frequency of side A (for notch responses). Figure 13 shows the measured frequency response of the circuit Figure 12 configured to provide a notch function. The filter output is taken out of pin 3. The resistor values are standard 1%.



$$f_o = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R2}{R4}};\ f_n = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R_h}{R_l}};\ H_{OHP} = -R2/R1;\ H_{OBP} = -R3/R1,\ H_{OLP} = -R4/R1$$

$$H_{ON1}(f \to 0) = \frac{R_g}{R_l} \times \frac{R4}{R1};\ H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times \frac{R2}{R1};\ H_{ON}(f = f_o) = Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right);\ Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}$$

Figure 11. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch.

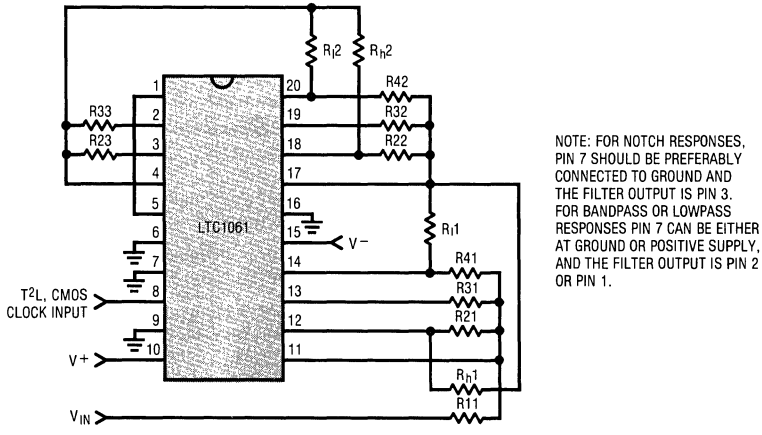


Figure 12. 6th Order Elliptic Bandpass, Lowpass or Notch Topology.

MODES OF OPERATION

The ratio of the 0dB width, BW1, to the notch width BW2, is 5:1 and matches the theoretical design value. The measured notch depth was –53dB versus –56dB theoretical and the clock to center notch frequency ratio is 100:1.

Figure 14 shows the measured frequency response of the circuit topology, Figure 12, but with pole/zero locations configured to provide a high Q, 6th order elliptic bandpass filter operating with a clock to center frequency ratio of 50:1 or 100:1. The theoretical passband ripple, stopband attenuation and stopband to ripple bandwidth ratio are 0.5dB, 56dB, 5:1 respectively. The obtained results with 1% standard resistor values closely match the theoretical frequency response. For this application, the normalized center frequencies, Q's, and notch frequencies are ($f_o1 = 0.969$, $Q1 = 54.3$, $f_n1 = 0.84$, $f_o2 = 1.031$, $Q2 = 54.3$, $f_n2 = 1.187$, $f_o3 = 1$, $Q3 = 26.2$). The output of the filter is the BP output of Side A, Pin 2.

Lowpass filters with stopband notches can also be realized by using Figure 12 provided that 6th order lowpass filter approximations with 2 stopband notches can be synthesized. Literature describing elliptic double terminated (RLC) passive ladder filters provide enough data to synthesize the above filters. The measured amplitude response of such a lowpass is shown in Figure 15 where the filter output is taken out of side A's Pin 1, Figure 12. The clock to center frequency ratio can be either 50:1 or 100:1 because the last stage of the LTC1061 operates in Mode 1 with a center frequency very close to the overall cutoff frequency of the lowpass filter.

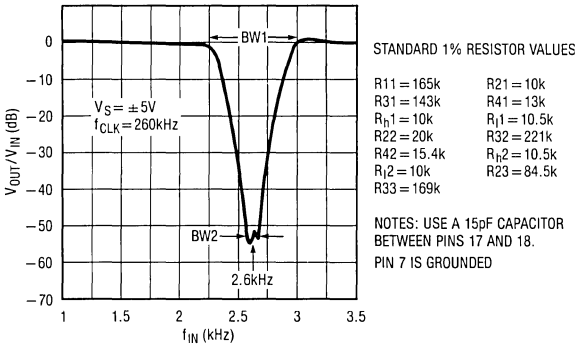


Figure 13. Resistor Values and Amplitude Response of Figure 12 Topology. The Notch is Centered at 2600Hz.

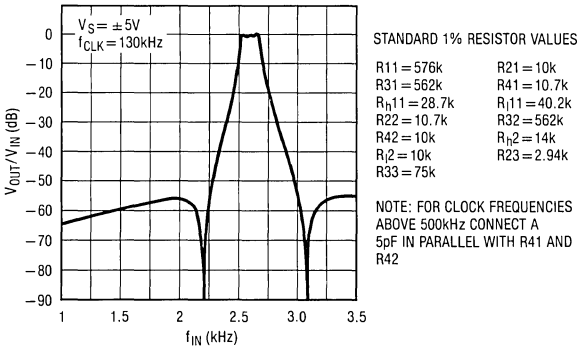


Figure 14. Resistor Values and Amplitude Response of Figure 12 Topology. The Bandpass Filter is Centered Around 2600Hz when Operating with a 130kHz Clock.

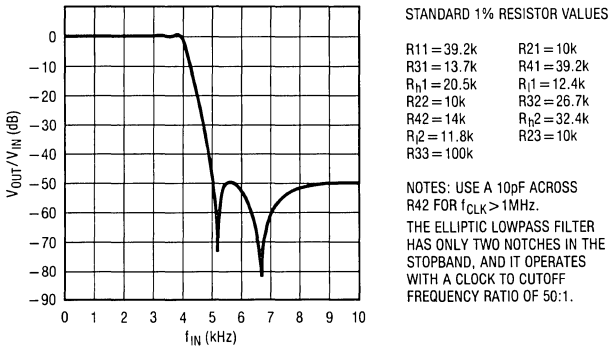


Figure 15. Resistor Values and Amplitude Response of the Topology of Figure 12.

MODES OF OPERATION

In Figure 16, all three sides of the LTC1061 are connected in Mode 3a. This topology is useful for elliptic highpass and notch filters with clock to cutoff (or notch) frequency ratio higher than 100:1. This is often required to extend the allowed input signal frequency range and to avoid premature aliasing. Figure 16 is also a versatile, general purpose architecture providing 3 notches and 3 pole pairs, and there is no restriction on the location of the poles with respect to the notch frequencies. The drawbacks, when compared to Figure 12, are the use of an external op amp and the increased number of the required external resistors. Figure 17 shows the measured frequency of a 6th order highpass elliptic filter operating with 250:1 clock to cutoff frequency ratio. With a 1MHz clock, for instance, the filter yields a 4kHz cutoff frequency, thus allowing an input frequency range beyond 100kHz. Band limiting can be easily added by placing a capacitor across the feedback resistor of the external op amp of Figure 16.

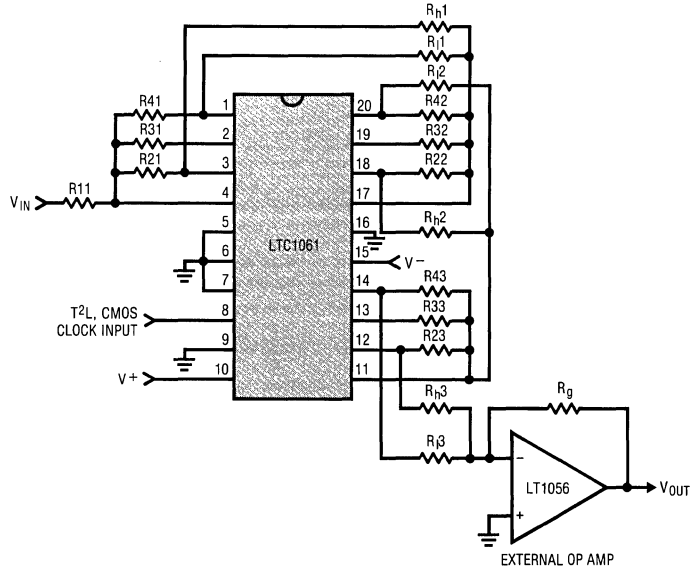
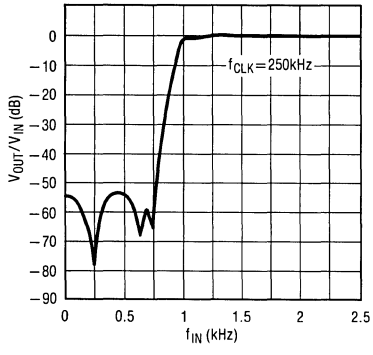


Figure 16. Using an External Op Amp to Connect all 3 Sides of the LTC1061 in Mode 3a.



STANDARD 1% RESISTOR VALUES

R11 = 105k	R21 = 10k
R31 = 47.5k	R41 = 45.3k
$R_{h}1$ = 10k	$R_{i}1$ = 1.07M
R22 = 32.4k	R32 = 28.7k
R42 = 52.3k	$R_{h}2$ = 42.2k
$R_{i}2$ = 750k	R23 = 10k
R33 = 255k	R43 = 63.4k
$R_{h}3$ = 10k	$R_{i}3$ = 110k
R_{g} = 140k	

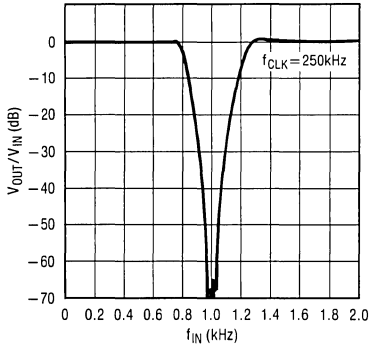
NOTE: FOR CLOCK FREQUENCIES BELOW 500kHz, USE A CAPACITOR IN PARALLEL WITH R21 SUCH AS $(1/2\pi R21C) \simeq f_{CLK}/3$

Figure 17. Measured Amplitude Response of the Topology of Figure 16, Configured to Provide a 6th Order Elliptic Highpass Filter Operating with a Clock to Cutoff Frequency Ratio of 250:1.

MODES OF OPERATION

Figure 18 shows the plotted amplitude responses of a 6th order notch filter operating again with a clock to center notch frequency ratio of 250:1. The theoretical notch depth is 70dB and when the notch is centered at 1kHz its width is 50Hz. Two small, noncritical capacitors were used across the R21 and R22 resistors of Figure 16, to bandlimit the first two highpass outputs such that the practical notch depth will approach the theoretical value. With these two fixed capacitors, the notch frequency can be swept within a 3:1 range.

When the circuit of Figure 16 is used to realize lowpass elliptic filters, a capacitor across R_g raises the order of the filter and at the same time eliminates any small clock feedthrough. This is shown in Figure 19 where the amplitude response of the filter is plotted for 3 different cutoff frequencies. When the clock frequency equals or exceeds 1MHz, the stopband notches lose their depth due to the finite bandwidth of the internal op amps and to the small crosstalk between the different sides of the LTC1061. The lowpasss filter, however, does not lose its passband accuracy and it maintains nearly all of its attenuation slope. The theoretical performance of the 7th order lowpass filter of Figure 19 is 0.2dB passband ripple, 1.5:1 stopband to cutoff frequency ratio, and 73dB stopband attenuation. Without any tuning, the obtained results closely approximate the textbook response.

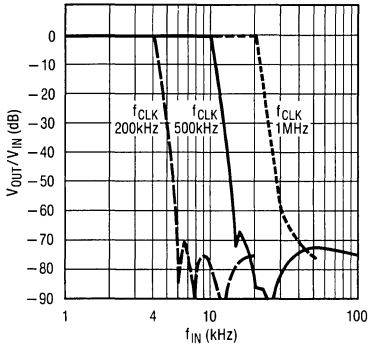


STANDARD 1% RESISTOR VALUES

R11 = 84.5k	R21 = 10.2k
R31 = 31.6k	R41 = 63.4k
$R_{h}1$ = 48.7k	$R_{l}1$ = 287k
R22 = 10k	R32 = 232k
R42 = 97.6k	$R_{h}2$ = 10.2k
$R_{l}2$ = 66.5k	R23 = 20k
R33 = 300k	R43 = 80.6k
$R_{h}3$ = 10.2k	$R_{l}3$ = 63.4k
R_g = 210k	

NOTE: CONNECT 39pF AND 100pF ACROSS R21 AND R22 RESPECTIVELY.

Figure 18. 6th Order Band Reject Filter Operating with a Clock to Center Notch Frequency Ratio of 250:1. The Ratio of 0dB to the –65dB Notch Width is 8:1.



STANDARD 1% RESISTOR VALUES

R11 = 30.9k	R21 = 10k
R31 = 16.2k	R41 = 26.7k
$R_{h}1$ = 45.3k	$R_{l}1$ = 19.6k
R22 = 10.5k	R32 = 100k
R42 = 10k	$R_{h}2$ = 52.3k
$R_{l}2$ = 15.8k	R23 = 10k
R33 = 28.7k	R43 = 12.7k
$R_{h}3$ = 95.3k	$R_{l}3$ = 10k
R_g = 28k	

NOTE: ADD A CAPACITOR C ACROSS R_g TO CREATE A 7TH ORDER LOWPASS SUCH AS $(1/2\pi R_g C)$ = (CUTOFF FREQUENCY) × 0.38

Figure 19. Frequency Responses of a 7th Order Lowpass Elliptic Filter Realized with Figure 16 Topology.

MODES OF OPERATION

Mode 2—This is a combination of Mode 1 and Mode 3, Figure 20. With Mode 2, the clock to center frequency ratio, f_{CLK}/f_0, is always less than 50:1 or 100:1. When compared to Mode 3 and for applications requiring 2nd order sections with f_{CLK}/f_0 slightly less than 100 or 50:1, Mode 2 provides less sensitivity to resistor tolerances. As in Mode 1, Mode 2 has a notch output which directly depends on the clock frequency and therefore the notch frequency is always less than the center frequency, f_0, of the 2nd order section. Figure 21 shows the side A of the LTC1061 connected in Mode 2 while sides B and C are in Mode 3a. This topology can be used to synthesize elliptic bandpass, highpass and notch filters. The elliptic highpass of Figure 17 is synthesized again, Figure 22, but the clock is now locked onto the higher frequency notch provided by the side A of the LTC1061. As shown in Figure 22, the highpass corner frequency is 3.93kHz and the higher notch frequency is 3kHz while the filter operates with a 300kHz clock. The center frequencies, Q's, and notches of Figure 22, when normalized to the highpass cutoff frequency, are ($f_0 1 = 1.17$, $Q1 = 2.24$, $f_n 1 = 0.242$, $f_0 2 = 1.96$, $Q2 = 0.7$, $f_n 2 = 0.6$, $f_0 3 = 0.987$, $f_n 3 = 0.753$, $Q = 10$). When compared with the topology of Figure 16, this approach uses lower and more restricted clock frequencies. The obtained notch in Mode 2 is shallower; however, this topology is more efficient.

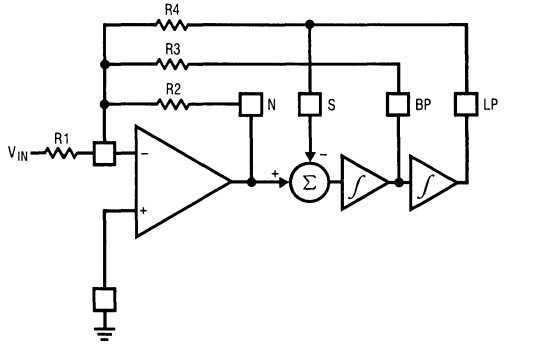


Figure 20. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass.

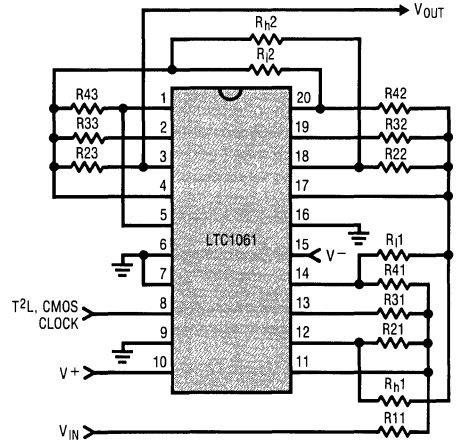
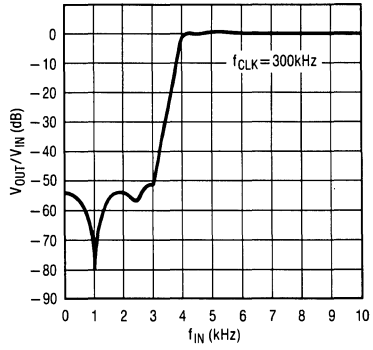


Figure 21. LTC1061 with Side A is Connected in Mode 2 while Sides B, C are in Mode 3a. Topology is Useful for Elliptic Highpass, Notch and Bandpass Filters.



STANDARD 1% RESISTOR VALUES

R11 = 54.9k	R21 = 24.3k
R31 = 34.8k	R41 = 10k
R_h1 = 28.7k	R_l1 = 280k
R22 = 68.1k	R32 = 18.2k
R42 = 10k	R_h2 = 10.2k
R_l2 = 16.2k	R23 = 10k
R33 = 75k	R43 = 14k

NOTE: FOR CLOCK FREQUENCIES ABOVE 300kHz ADD A CAPACITOR, C, ACROSS R21 AND R22 SUCH AS $(1/2\pi R21C) = f_{CLK}$

Figure 22. 6th Order Elliptic Highpass Filter Operating with a Clock to Cutoff Frequency Ratio of 75:1, and Using the Topology of Figure 21.

MODES OF OPERATION

Output Noise

The wideband RMS noise of the LTC1061 outputs is nearly independent from the clock frequency. The LTC1061 noise when operating with ±2.5V supply is lower, as Table 3 indicates. The noise at the bandpass and lowpass outputs increases roughly as the $\sqrt{Q}$. Also the noise increases when the clock to center frequency ratio is altered with external resistors to exceed the internally set 100:1 or 50:1 ratios. Under this condition, the noise increases square root-wise.

Output Offsets

The equivalent input offsets of the LTC1061 are shown in Figure 23. The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 4 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Q's decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

Table 3. Wideband RMS Noise

V_s	$\frac{f_{CLK}}{f_o}$	Notch/HP (μV_{RMS})	BP (μV_{RMS})	LP (μV_{RMS})	CONDITIONS
±5V	50:1	45	55	70	Mode 1, R1 = R2 = R3
±5V	100:1	65	65	85	Q = 1
±2.5V	50:1	30	30	45	
±2.5V	100:1	40	40	60	
±5V	50:1	18	150	150	Mode 1, Q = 10
±5V	100:1	20	200	200	R1 = R3 for BP out
±2.5V	50:1	15	100	100	R1 = R2 for LP out
±2.5V	100:1	17	140	140	
±5V	50:1	57	57	62	Mode 3, R1 = R2 = R3 = R4
±5V	100:1	72	72	80	Q = 1
±2.5V	50:1	40	40	42	
±2.5V	100:1	50	50	53	
±5V	50:1	135	120	140	Mode 3, R2 = R4, Q = 10
±5V	100:1	170	160	185	R3 = R1 for BP out
±2.5V	50:1	100	88	100	R4 = R1 for LP and HP out
±2.5V	100:1	125	115	130	

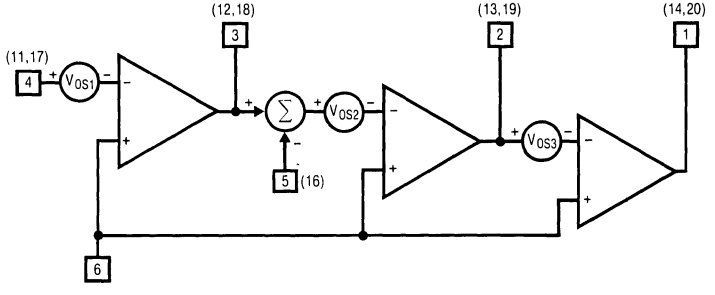


Figure 23. Equivalent Input Offsets of 1/3 LTC1061 Filter Building Block.

MODES OF OPERATION

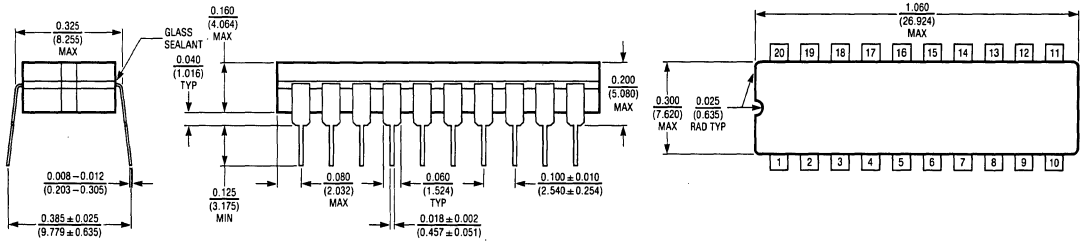
Table 4

Mode	V_{OSN} Pin 3 (18)	V_{OSBP} Pin 2 (19)	V_{OSLP} Pin 1 (20)
1	$V_{OS1}[(1/Q) + 1 + \|H_{OLP}\|] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times$ $\times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1}\left[1 + \frac{R4}{R1} + \frac{R4}{R2} + \frac{R4}{R3}\right] - V_{OS2}\left(\frac{R4}{R2}\right)$ $- V_{OS3}\left(\frac{R4}{R3}\right)$

PACKAGE DESCRIPTION

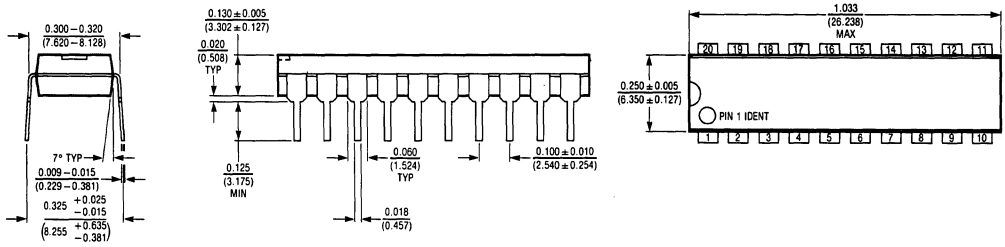
Dimensions in inches (millimeters) unless otherwise noted.

J20 Package Ceramic DIP



T_{jmax}	θ_{ja}
125°C	100°C/W

N20 Package Molded DIP



T_{jmax}	θ_{ja}
100°C	100°C/W

SECTION 7—PULSE WIDTH MODULATORS

SECTION 7—PULSE-WIDTH MODULATORS

SECTION 8—CMOS/ DATA CONVERSION/ INTERFACE

SECTION 8—CMOS/DATA CONVERSION/INTERFACE

Quad Low Power Line Driver

FEATURES

- Low Operating Voltage ±5V to ±15V
- 500μA Supply Current
- Zero Supply Current when Shut Down
- Outputs Can Be Driven ±30V
- Output "Open" when Off (3-State)
- 10mA Output Drive
- Pinout Similar to 1488*
- Output of Several Devices can be Paralleled

APPLICATIONS

- RS232 Driver
- Micropower Interface
- Level Translator

* Check compatibility, some pins different

DESCRIPTION

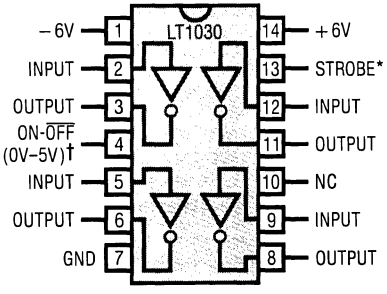
The LT1030 is an RS232 line driver that operates over a ±5V to ±15V range on low supply current and can be shut down to zero supply current. Outputs are fully protected from externally applied voltages of ±30V by current limiting. Since the output swings to within 200mV of the positive supply and 1V of the negative supply, power supply needs are minimized.

A major advantage of the LT1030 is the high impedance output state when off or powered down, which allows several different drivers on the same bus.

Our RS232 product line includes other high-performance devices. The LT1039 is a triple low-power driver/receiver with shutdown that can be powered from a 5V supply. The LT1080 is a 5V powered dual driver/receiver with on-chip ±9V power generator, and shutdown.

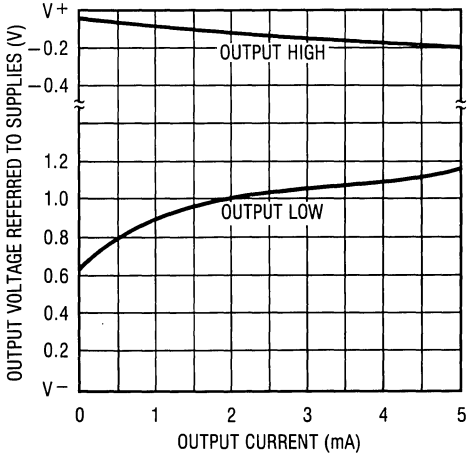
TYPICAL APPLICATION

RS232 Line Driver



*NO CONNECTION NEEDED WHEN NOT USED.
†5V = ON.

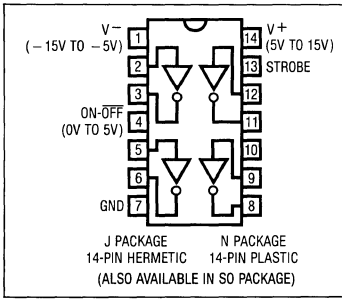
Output Swing vs Output Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±15V
Logic Input Pins ..... V^- to 25V
On-$\overline{\text{Off}}$ Pin ..... GND to 12V
Output (Forced) ..... V^- +30V, V^+ −30V
Short Circuit Duration (to ±30V) ..... Indefinite
Operating Temperature Range
LT1030C ..... 0°C to 70°C
Guaranteed Functional by Design ... −25°C to 85°C
Storage Temperature ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE 14-PIN HERMETIC
N PACKAGE 14-PIN PLASTIC
(ALSO AVAILABLE IN SO PACKAGE)

ORDER PART NUMBER
LT1030CJ LT1030CN FOR MILITARY APPLICATIONS USE LT1032MJ

ELECTRICAL CHARACTERISTICS (Supply Voltage = ±5V to ±15V)

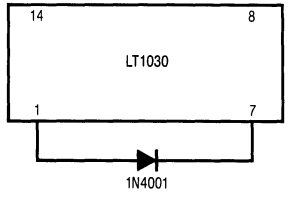
PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current	$V_{ON-\overline{OFF}} \geq 2.4V$, $I_{OUT} = 0$, All Outputs Low		●		500	1000	μA
Power Supply Leakage Current	$V_{ON-\overline{OFF}} \leq 0.4V$				1	10	μA
	$V_{ON-\overline{OFF}} \leq 0.1V$		●		10	150	μA
Output Voltage Swing	Load = 2mA	Positive		$V^+ - 0.3V$	$V^+ - 0.1V$		V
		Negative			$V^- + 0.9V$	$V^- + 1.4V$	V
Output Current	V_{SUPPLY} ±5V to ±15V			5	12		mA
Output Overload Voltage (Forced)	Operating or Shutdown		●	$V^+ - 30V$		$V^- + 30V$	V
Output Current	Shutdown $V_{OUT} = \pm 30V$				2	100	μA
Input Overload Voltage (Forced)	Operating or Shutdown		●	V^-		15	V
Logic Input Levels	Low Input (V_{OUT} = High)		●		1.4	0.8	V
	High Input (V_{OUT} = Low)		●	2	1.4		V
Logic Input Current	$V_{IN} > 2.0V$				2	20	μA
	$V_{IN} < 0.8V$				10	20	μA
On-$\overline{\text{Off}}$ Pin Current	$0 \leq V_{IN} \leq 5V$		●	−10	30	65	μA
Slew Rate				4	15	30	V/μS

The ● denotes specifications which apply over the operating temperature range.

Note 1: 3V applied to the strobe pin will force all outputs low. Strobe pin input impedance is about 2k to ground. Leave open when not used.

PIN FUNCTIONS

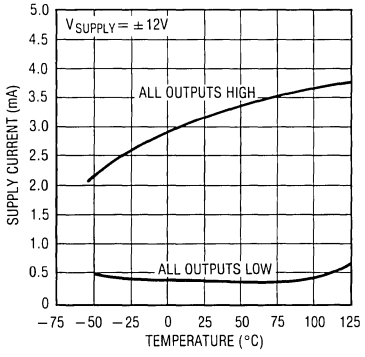
PIN	FUNCTION	COMMENT
1	Minus Supply	Operates −2V to −15V
2,5,9,12	Logic Input	Operates properly on TTL or CMOS levels. Output valid from $(V^- + 2V) \leq V_{IN} \leq 15V$. Connect to 5V when not used.
3,6,8,11	Output	Line drive output.
4	On-$\overline{\text{Off}}$	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect between 5V-10V.
7	Ground	Ground must be more positive than V^-
13	Strobe	Forces all outputs low. Drive with 3V.
14		Positive supply 5V to 15V.



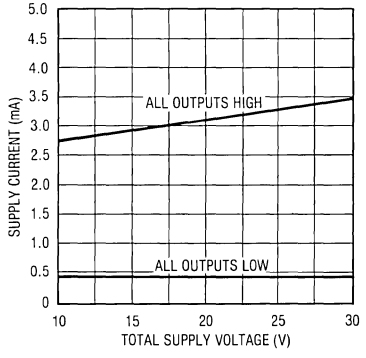
Note: As with other bipolar ICs, forward biasing the substrate diode can cause problems. The LT1030 will draw high current from V^+ to ground if the V^- pin is open circuited or pulled above ground. If this is possible, connecting a diode from V^- to ground will prevent the high current state. Any low cost diode can be used.

TYPICAL PERFORMANCE CHARACTERISTICS

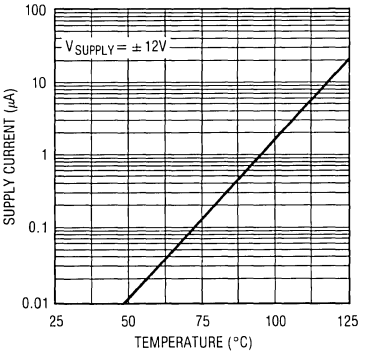
On Supply Current vs Temperature



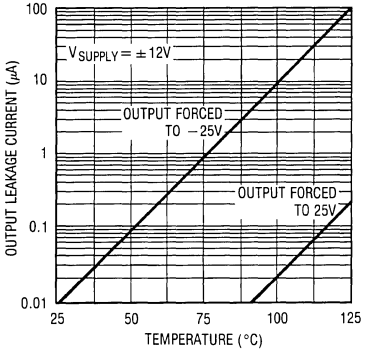
On Supply Current vs Supply Voltage



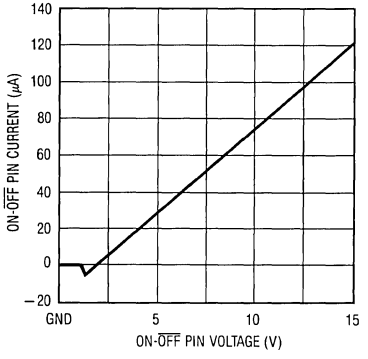
Off Supply Current vs Temperature



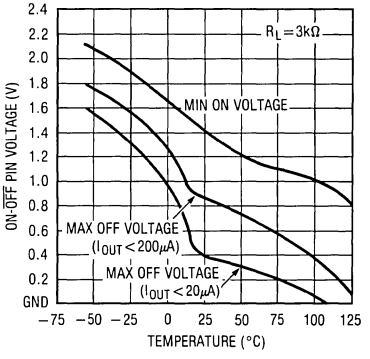
Off Output Leakage vs Temperature



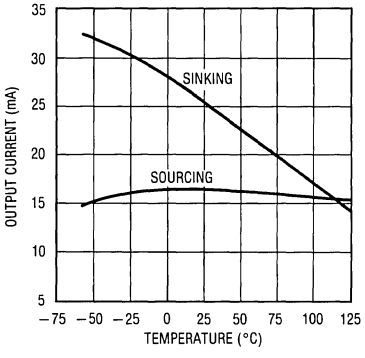
On-$\overline{\text{Off}}$ Pin Current vs Voltage



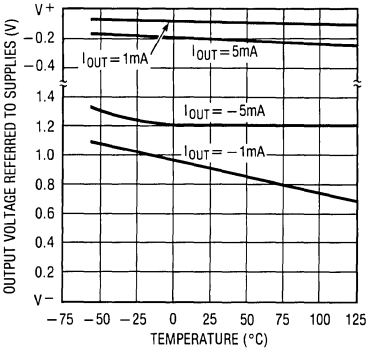
Shutdown Voltage vs Temperature



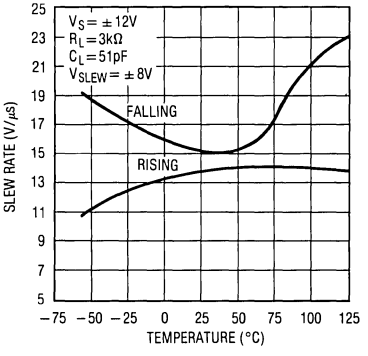
Current Limit vs Temperature



Output Swing vs Temperature

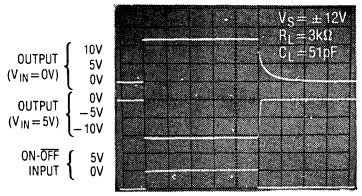


Slew Rate vs Temperature



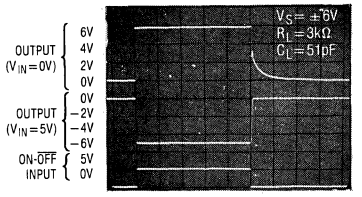
TYPICAL PERFORMANCE CHARACTERISTICS

On-$\overline{Off}$ Response Time



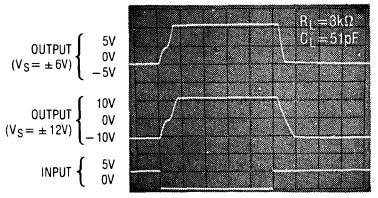
H = 100μs/DIV

On-$\overline{Off}$ Response Time



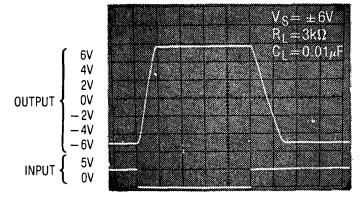
H = 100μs/DIV

Output Waveform



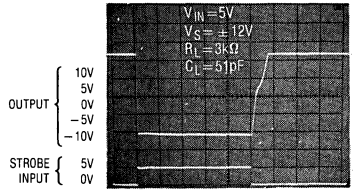
H = 2μs/DIV

Output Waveform Driving Capacitive Load



H = 10μs/DIV

Strobe Pin Response Time

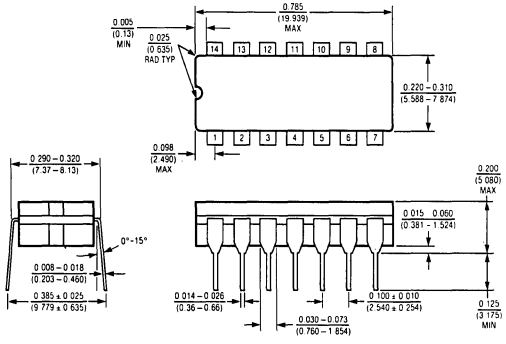


H = 2μs/DIV

PACKAGE DESCRIPTION

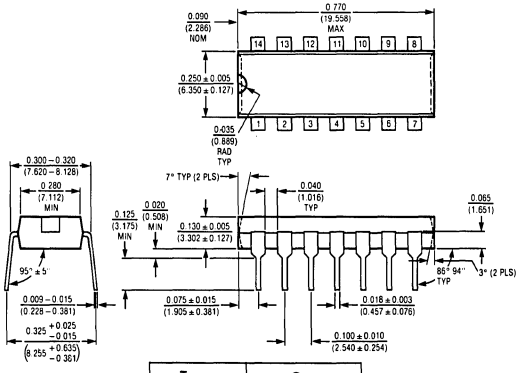
Dimensions in inches (millimeters) unless otherwise noted.

J Package
14-Lead Hermetic DIP



T_{jmax}	Θ_{JA}
150°C	80°C/W

N Package
14-Lead Plastic



T_{jmax}	Θ_{JA}
110°C	130°C/W

RS232 Driver/Receiver with Shutdown

FEATURES

- Operates from ±5V to ±15V Supplies
- Fully Protected Against Overload
- Outputs can be Driven ±30V without Damage
- Three-State Outputs; Outputs Open when Off
- Bipolar Circuit—No Latch Up
- ±30V Input Range
- Triple Driver/Receiver
- No Supply Current in Shutdown
- 30kΩ Input Impedance
- Meets All RS232 Specifications
- 16 Pin Version

APPLICATIONS

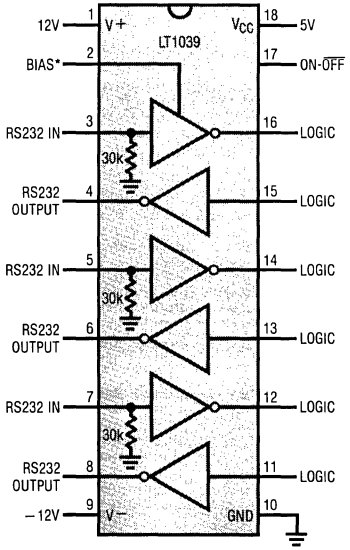
- RS232 Interface
- Terminals
- Modems

DESCRIPTION

The LT1039 is a triple RS232 driver/receiver which includes SHUTDOWN. Each receiver will accept up to ±30V input and can drive either TTL or CMOS logic. The RS232 drivers accept TTL logic inputs and output RS232 voltage levels. The outputs are fully protected against overload and can be shorted to ground or up to ±30V without damage to the drivers. Additionally, when the system is shut down or power is off, the outputs are in a high impedance state allowing data line sharing. Bipolar circuitry makes this driver/receiver exceptionally rugged against overloads or **ESD** damage.

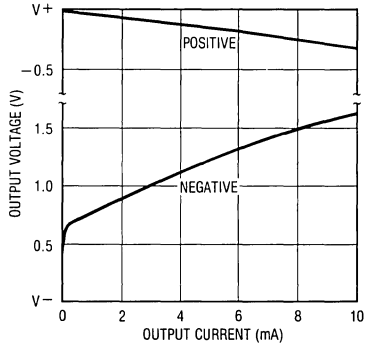
A bias pin allows one receiver to be kept on while the rest of the part is shut down.

TYPICAL APPLICATION



*BIAS PIN USED TO KEEP THE RECEIVER ON WHILE IN SHUTDOWN.

Driver Output Swing



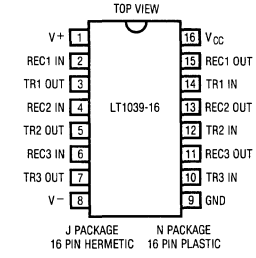
ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- Driver (V^+, V^-) ..... ±16V
- Receiver (V_{CC}) 7V

Logic Inputs ..... V^- to 25V
Receiver Inputs ..... ±30V
On-$\overline{\text{Off}}$ Input ..... GND to 12V
Driver Outputs ..... V^- +30V to V^+ −30V
Short Circuit Duration ..... Indefinite
Operating Temperature Range
- LT1039M ..... −55°C to 125°C
- LT1039C ..... 0°C to 70°C
- Guaranteed Functional by Design ..... −25°C to 85°C

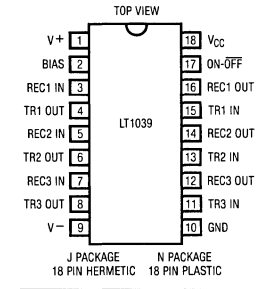
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1039CN16
LT1039CJ16
LT1039MJ16



LT1039CN
LT1039CJ
LT1039MJ

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Driver $V^+ = 12V$; $V^- = -12V$; $V_{ON\text{-}OFF} = 2.5V$							
Output Voltage Swing	Load = 3k to Ground	Positive	●	$V^+ - 0.4$	$V^+ - 0.1$		V
		Negative	●	$V^- + 1.5$	$V^- + 1$		V
Logic Input Voltage Levels	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} \geq 2.0V$				1	20	µA
	$V_{IN} \leq 0.8V$				5	20	µA
Output Short Circuit Current	Sourcing Current, $V_{OUT} = 0V$			5	15		mA
	Sinking Current, $V_{OUT} = 0V$			−5	−15		mA
Output Leakage Current	SHUTDOWN (Notes 1 and 2); $V_{OUT} = \pm 18V$, $V_{IN} = 0$		●		10 (25°C)	200	µA
Supply Leakage Current	SHUTDOWN (Note 1)		●		1 (25°C)	100	µA
Slew Rate	$R_L = 3k\Omega$; $C_L = 51pF$			4	15	30	V/µs
Supply Current	V_{OUT} = Low				4	8	mA
Receiver $V_{CC} = 5V$; $V_{ON\text{-}OFF} = 2.5V$							
Input Voltage Thresholds	Input Low (V_{OUT} = High)		●	0.5	1.3		V
	Input High (V_{OUT} = Low)		●		1.7	2.8	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance			●		30		kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$		●		0.4	0.5	V
	Output High, $I_{OUT} = 160\mu A$		●	3.5	4.8		V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		●	−10			mA
	Sourcing Current, $V_{OUT} = 0V$ (Note 3)		●	0.5	1		mA
Output Leakage Current	SHUTDOWN (Note 1); $0V \leq V_{OUT} \leq V_{CC}$, $V_{IN} = 0$		●		1	10	µA
Supply Current			●		4	7	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Leakage Current	SHUTDOWN (Note 1)	●		1 (25°C)	100	μA
On-Off Pin Current	$0V \le V_{ON-OFF} \le 5V$	●	–15		80	μA

The ● denotes specifications which apply over the operating temperature range.

Note 1: $V_{ON-OFF} = 0.4V$ for $-55°C \le T_A \le 100°C$, and $V_{ON-OFF} = 0.2V$ for $100°C \le T_A \le 125°C$. Does not apply to LT1039-16 part.

Note 2: For $T_A \ge 100°C$, leakage current is 350μA max.

Note 3: For $T_A \le -25°C$, output source current is 0.4 mA.

PIN FUNCTIONS

V+, V– (Pins 1, 9): Driver supply pins. Supply current drops to zero in SHUTDOWN mode. Driver outputs are in a high impedance state when V+ and V– = 0V.

V_{CC} (Pin 18): 5V power for receivers.

GND (Pin 10): Ground pin.

TR IN (Pins 11, 13, 15): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR OUT (Pins 4, 6, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off (V+ and V– = 0V) to allow data line sharing. Outputs are fully short circuit protected from V– +30V to V+ –30V with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than ±45V and higher applied voltages will not damage the device if moderately current limited.

REC IN (Pins 3, 5, 7): Receiver input pins. Accepts RS232 voltage levels (±30V) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 30kΩ.

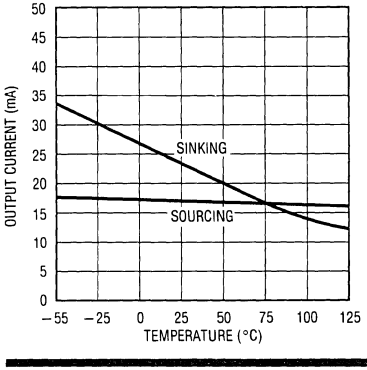
REC OUT (Pins 12, 14, 16): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

ON-$\overline{\text{OFF}}$ (Pin 17): Controls the operation mode of the LT1039 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state.

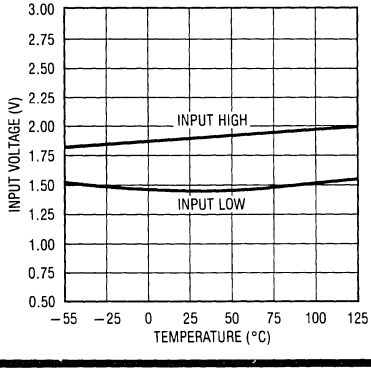
BIAS (Pin 2): Keeps receiver 1 on while the LT1039 is in the SHUTDOWN mode. Leave BIAS pin open when not in use. See Application Hints for proper use.

TYPICAL PERFORMANCE CHARACTERISTICS

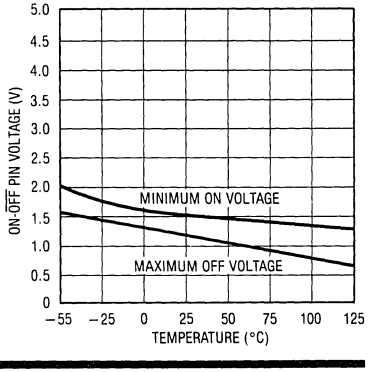
Driver Output Short Circuit Current



Receiver Input Thresholds

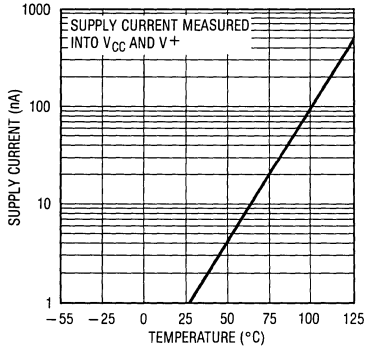


On-$\overline{\text{Off}}$ Pin Thresholds

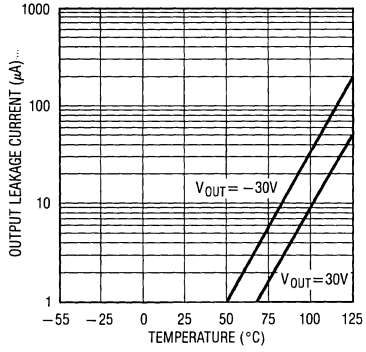


TYPICAL PERFORMANCE CHARACTERISTICS

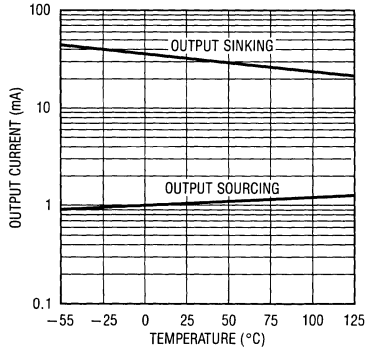
Supply Current in SHUTDOWN



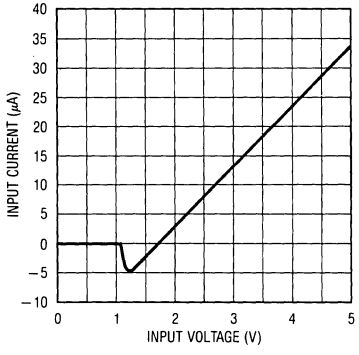
Driver Output Leakage in SHUTDOWN



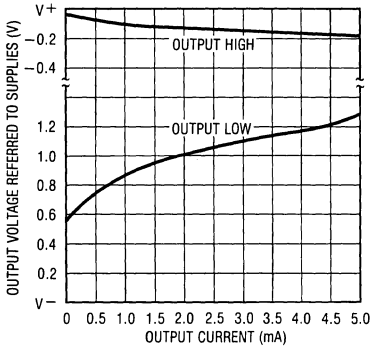
Receiver Output Short Circuit Current



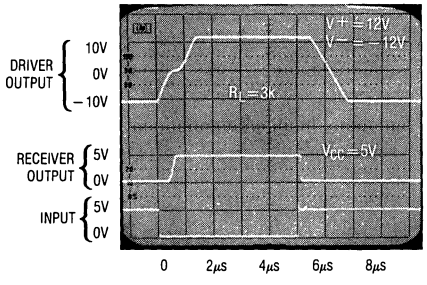
On-$\overline{\text{Off}}$ Pin Current vs Voltage



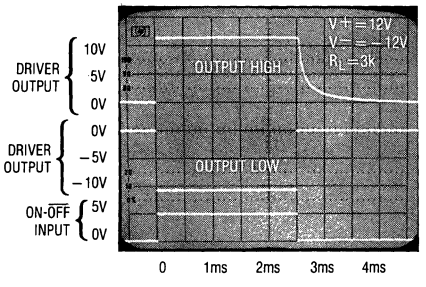
Driver Output Swing vs Current



Output Waveforms

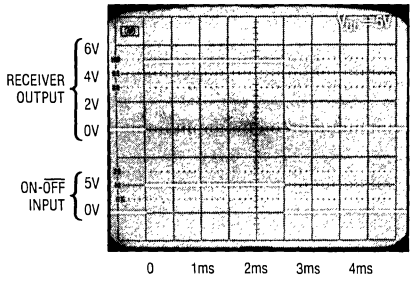


SHUTDOWN to Driver Output

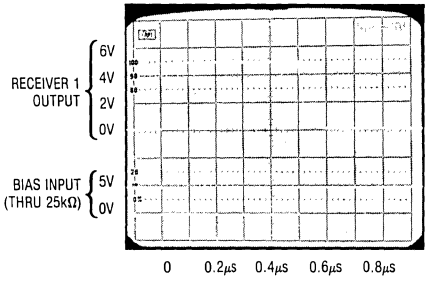


TYPICAL PERFORMANCE CHARACTERISTICS

SHUTDOWN to Receiver Output

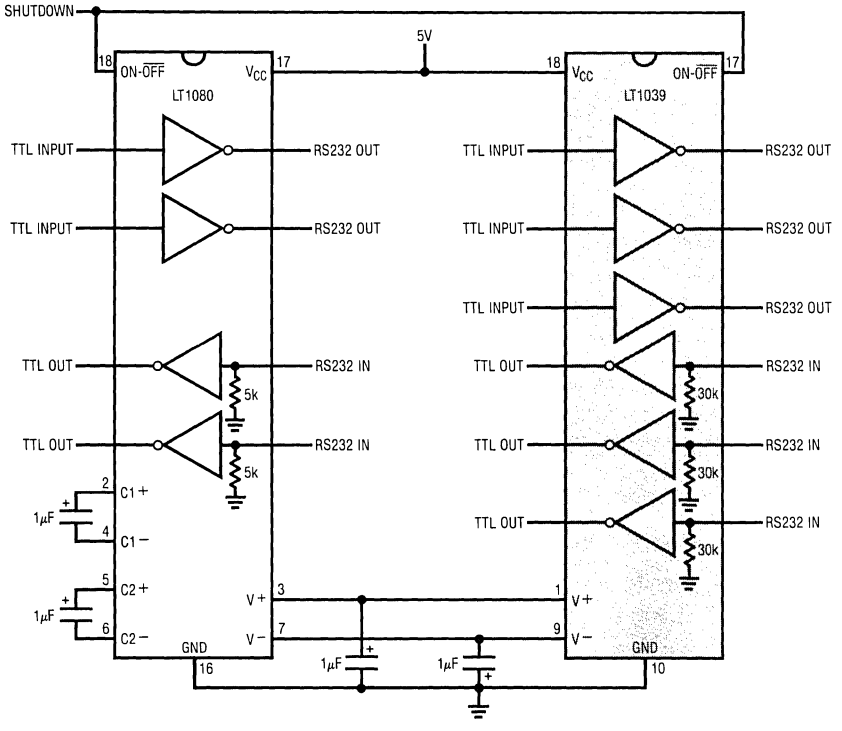


Bias Pin Response Time



TYPICAL APPLICATION

LT1080 (Driver/Receiver with Power Supply) Driving an LT1039



APPLICATION HINTS

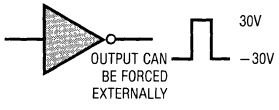
The driver output stage of the LT1039 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to ±30V with no damage or excessive current flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

Placing the LT1039 in the SHUTDOWN mode (Pin 17 low) puts both the driver and receiver outputs in a high impedance state. This allows data line sharing and transceiver applications.

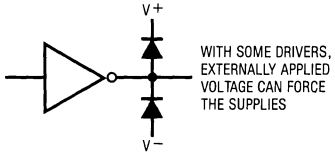
The SHUTDOWN mode also drops all supply currents (V_{CC}, V^+, V^-) to zero for power-conscious systems.

When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.

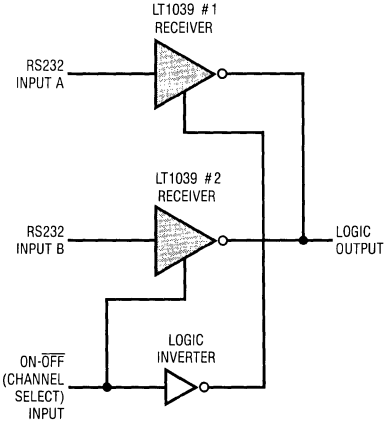
LT1039 Driver



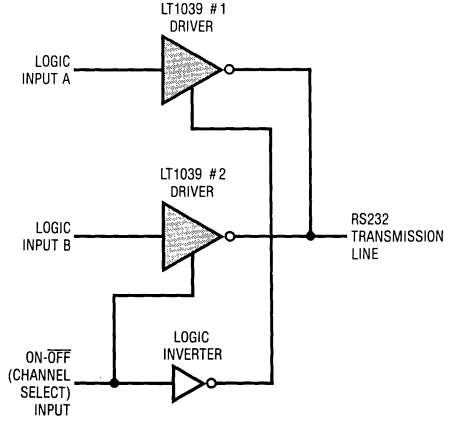
Older RS232 Drivers and Other CMOS Drivers



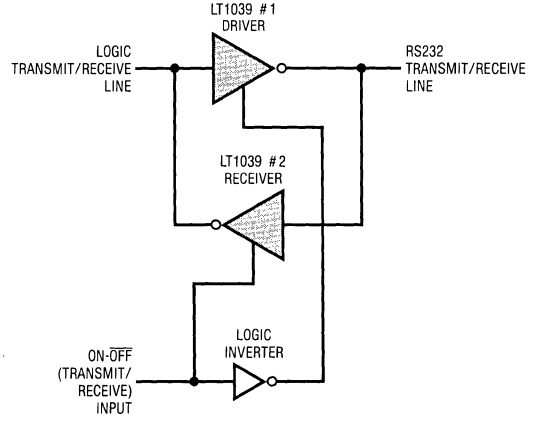
Sharing a Receiver Line



Sharing a Transmitter Line



Transceiver



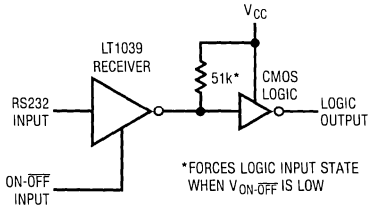
APPLICATION HINTS

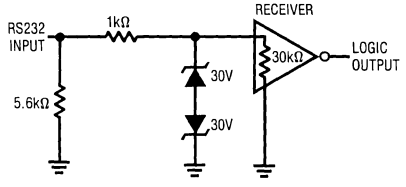
To protect against receiver input overloads in excess of ±30V, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.

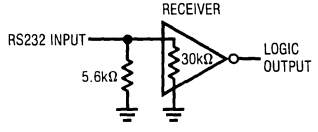
The receiver input impedance of the LT1039 is nominally 30kΩ. For applications requiring a 5kΩ input impedance, a 5.6kΩ resistor can be connected from the receiver input to ground.

Driver inputs should not be allowed to float. Any unused inputs should be tied to V_{CC}.

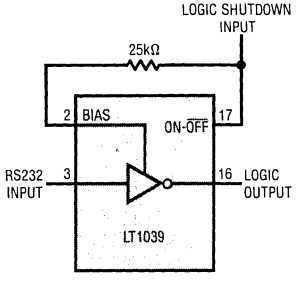
The bias pin is used to "keep alive" one receiver while in the SHUTDOWN mode (all other circuitry being inactive). This allows a system to be in SHUTDOWN and still have one active receiver for transferring data. It can also be used to make an RS232 compatible SHUTDOWN control line. Driving the bias pin low through a resistance of 24kΩ to 30kΩ keeps the receiver active. Do not drive the bias pin directly from a logic output without the series resistor. An unused bias pin should be left open.



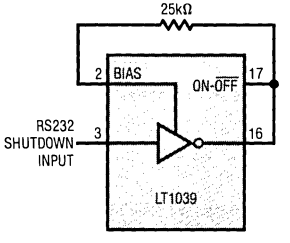




Keeping Alive One Receiver while in SHUTDOWN

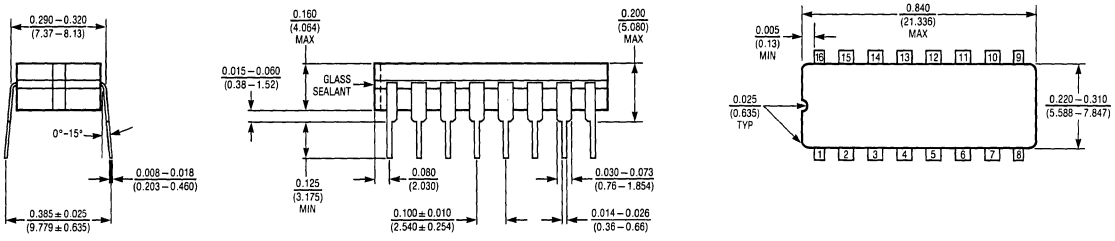


RS232 Compatible SHUTDOWN Control Line



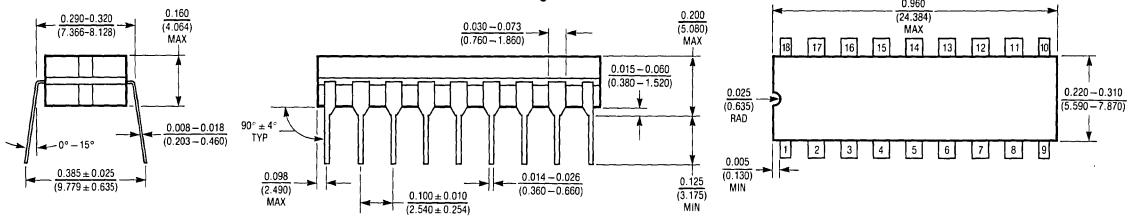
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J16 Package Ceramic DIP



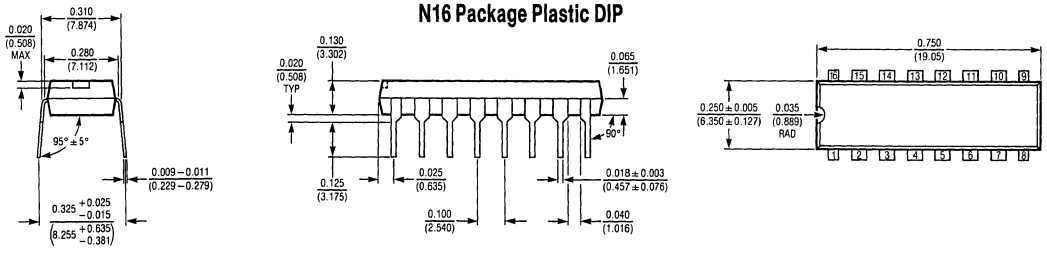
	T_{jmax}	θ_{ja}	θ_{jc}
LT1039MJ16	150°C	100°C/W	30°C/W
LT1039CJ16	150°C	100°C/W	30°C/W

J18 Package Ceramic DIP



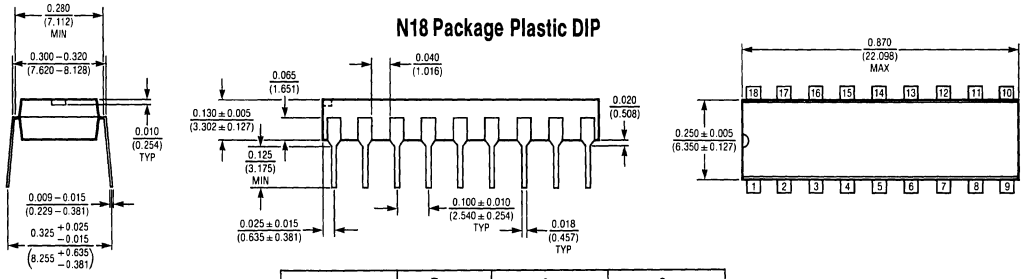
	T_{jmax}	θ_{ja}	θ_{jc}
LT1039MJ	150°C	100°C/W	40°C/W
LT1039CJ	150°C	100°C/W	40°C/W

N16 Package Plastic DIP



	T_{jmax}	θ_{ja}	θ_{jc}
LT1039CN16	85°C	140°C/W	50°C/W

N18 Package Plastic DIP



	T_{jmax}	θ_{ja}	θ_{jc}
LT1039CN	85°C	120°C/W	50°C/W

Switched Capacitor Voltage Converter with Regulator

FEATURES

- 100mA Output Current
- Low Loss—1.1V at 100mA
- Operating Range 3.5V to 15V
- Reference and Error Amplifier for Regulation
- External Shutdown
- External Oscillator Sync
- Can be Paralleled
- Pin Compatible with the LTC1044/7660

APPLICATIONS

- Voltage Inverter
- Negative Voltage Doubler
- Voltage Regulator
- Positive Voltage Doubler

DESCRIPTION

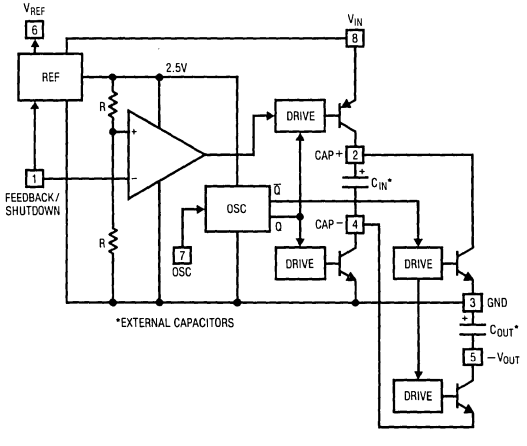
The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. The LT1054 provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5 mA.

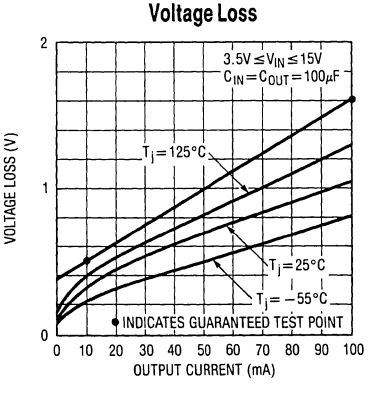
The LT1054 also provides regulation, a feature not previously available in switched capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output will be regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shut down is less than 100μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

The LT1054 is pin compatible with previous converters such as the LTC1044/7660.

BLOCK DIAGRAM

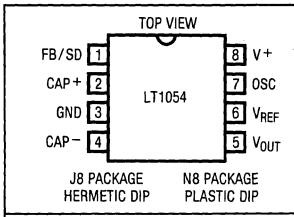




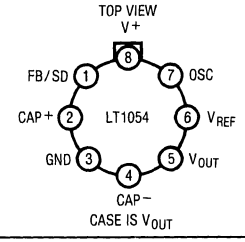
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) 16V
Input Voltage (Pin 1)..... $0V \le V_{PIN1} \le V^+$
Input Voltage (Pin 7) ..... $0V \le V_{PIN7} \le V_{REF}$
Operating Temperature Range
LT1054C ..... 0°C to 70°C
LT1054M ..... –55°C to 125°C
Junction Temperature (Note 2)
LT1054C..... 125°C
LT1054M ..... 150°C
Storage Temperature Range..... –55°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE HERMETIC DIP
N8 PACKAGE PLASTIC DIP



ORDER PART NUMBER
LT1054MJ LT1054CJ LT1054CN
LT1054MH LT1054CH

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	$I_{LOAD} = 0mA$					
	$V_{IN} = 3.5V$	●		2.5	3.5	mA
	$V_{IN} = 15V$	●		3.0	4.5	mA
Supply Voltage Range		●	3.5		15	V
Voltage Loss ($V_{IN} - \lvert V_{OUT} \rvert$)	$C_{IN} = C_{OUT} = 100\mu F$ Tantalum (Note 3)					
	$I_{OUT} = 10mA$	●		0.35	0.55	V
	$I_{OUT} = 100mA$	●		1.10	1.60	V
Output Resistance	$\Delta I_{OUT} = 10mA$ to 100mA (Note 4)	●		10	15	Ω
Oscillator Frequency	$3.5V \le V_{IN} \le 15V$	●	15	25	35	kHz
Reference Voltage	$I_{REF} = 60\mu A$					
	$T_j = 25°C$		2.35	2.50	2.65	V
		●	2.25		2.75	V
Regulated Voltage	$V_{IN} = 7V, T_j = 25°C$ (Note 5)		–4.70	–5.00	–5.20	V
Line Regulation	$7V \le V_{IN} \le 12V$ (Note 5)	●		5	25	mV
Load Regulation	$V_{IN} = 7V$					
	$500 \le R_L \le 100\Omega$ (Note 5)	●		10	50	mV
Maximum Switch Current				300		mA
Supply Current In Shutdown	$V_{PIN1} = 0V$	●		100	150	μA

The ● denotes specifications which apply over the full operating temperature range. For C grade parts these specifications also apply up to a junction temperature of 100°C.

Note 1: The absolute maximum supply voltage rating of 16V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \le 15V$ at Pin 5, this rating may be increased to 20V.

Note 2: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

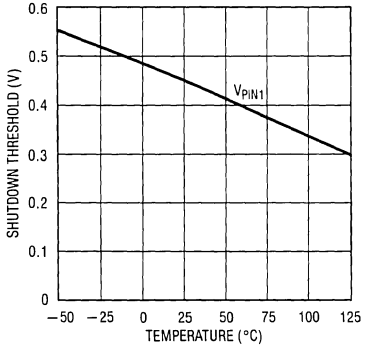
Note 3: For voltage loss tests, the device is connected as a voltage inverter, with Pins 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations.

Note 4: Output resistance is defined as the slope of the curve, (ΔV_{OUT} vs ΔI_{OUT}), for output currents of 10 to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents <10mA due to the characteristics of the switch transistors.

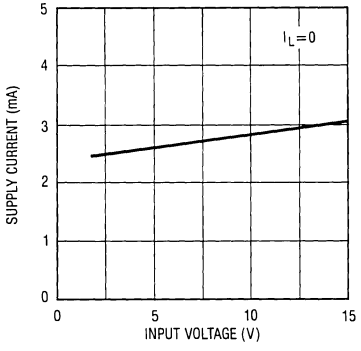
Note 5: All regulation specifications are for a device connected as a positive to negative converter/regulator with R1 = 20k, R2 = 102.5k, C1 = 0.05μF, C_{IN} = 10μF tantalum, C_{OUT} = 100μF tantalum.

TYPICAL PERFORMANCE CHARACTERISTICS

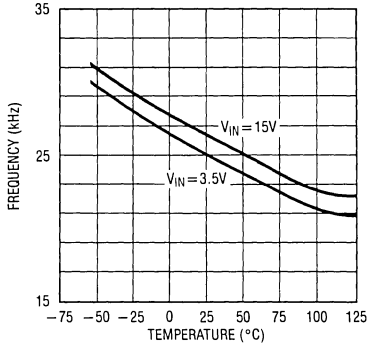
Shutdown Threshold



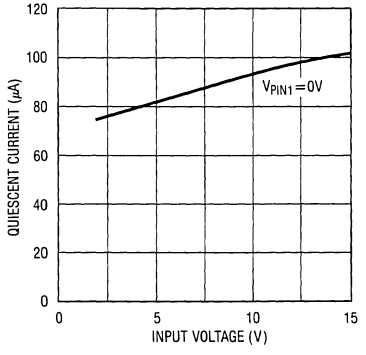
Supply Current



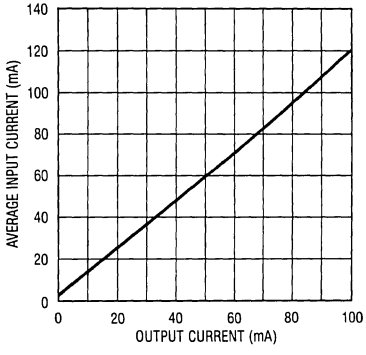
Oscillator Frequency



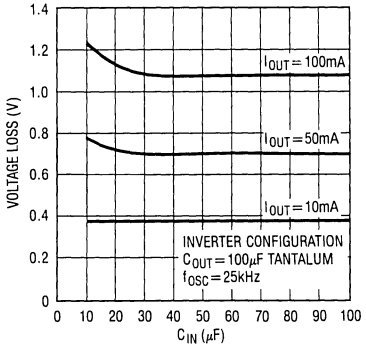
Supply Current in Shutdown



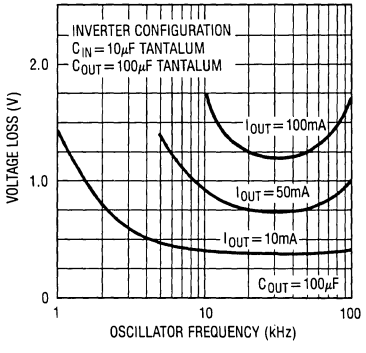
Average Input Current



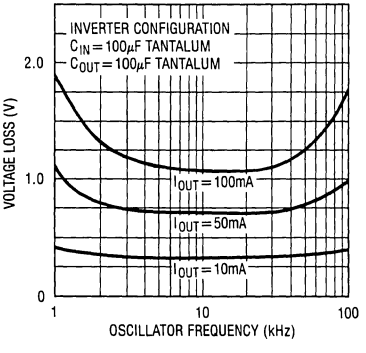
Output Voltage Loss



Output Voltage Loss

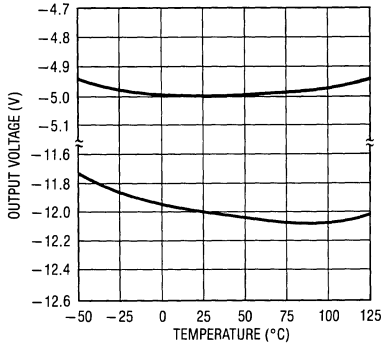


Output Voltage Loss

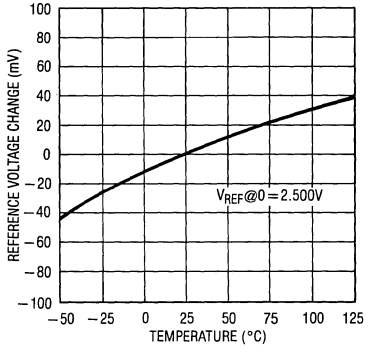


TYPICAL PERFORMANCE CHARACTERISTICS

Regulated Output Voltage



Reference Voltage Temperature Coefficient



APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LT1054, a review of a basic switched capacitor building block is helpful.

In Figure 1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be $q1 = C1V1$. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is $q2 = C1V2$. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2).$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

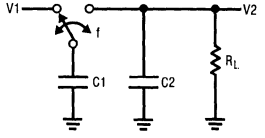


Figure 1. Switched Capacitor Building Block

A new variable, R_{EQUIV}, is defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure 2. The LT1054 has the same switching action as the basic switched capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency (see typical curve). As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and voltage losses will rise.

Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

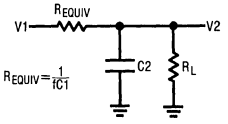


Figure 2. Switched Capacitor Equivalent Circuit

APPLICATIONS INFORMATION

Pin Functions

V^+ (Pin 8): Input supply pin. The LT1054 alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply, and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that C_{IN} is delivering charge to C_{OUT} the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054, and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2μF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example when the actual input supply is connected to the LT1054 through long leads, or when the pulse currents drawn by the LT1054 might affect other circuitry through supply coupling.

V_{OUT} (Pin 5): In addition to being the output pin, the pin is also tied to the substrate of the device. **Special care must be taken in LT1054 circuits to avoid pulling this pin positive with respect to any of the other pins.** For circuits with the output load connected from V^+ (Pin 8) to V_{OUT} (Pin 5), or from some external positive supply to V_{OUT} (Pin 5), an external transistor must be added as shown in Figure 3. This will prevent V_{OUT} (Pin 5) from being pulled above the ground pin (Pin 3) during start-up. Any small, general purpose transistor such as 2N2222 or 2N2219 can be used. R_X should be chosen to provide enough base drive to the external transistor, so that it is saturated under nominal output voltage and maximum output current conditions.

$$R_X \leq \frac{(|V_{OUT}| - V^+)\beta}{I_{OUT}}$$

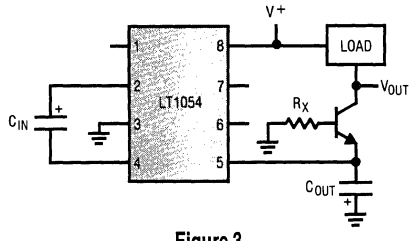


Figure 3

V_{REF} (Pin 6): Reference output pin. This pin provides a 2.5V reference point for use in LT1054 based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This non-zero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60μA. The reference pin will draw ≈100μA when shorted to ground, and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

CAP^+/CAP^- (Pin 2/Pin 4): Pin 2, the positive side of the input capacitor (C_{IN}) is alternately driven between V^+ and ground. When driven to V^+, Pin 2 sources current from V^+. When driven to ground, Pin 2 sinks current to ground. Pin 4, the negative side of the input capacitor is driven alternately between ground and V_{OUT}. When driven to ground, Pin 4 sinks current to ground. When driven to V_{OUT}, Pin 4 sources current from C_{OUT}. In all cases current flow in the switches is unidirectional, as should be expected using bipolar switches.

OSC (Pin 7): Oscillator pin. This pin can be used to raise or lower the oscillator frequency, or to synchronize the device to an external clock. Internally, Pin 7 is connected to the oscillator timing capacitor ($C_t \approx 150pF$) which is alternately charged and discharged by current sources of ±7μA, so that the duty cycle is ≈50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered or synchronized to an external system clock if necessary.

APPLICATIONS INFORMATION

The frequency can be lowered by adding an external capacitor (C1 Figure 4) from Pin 7 to ground. This will increase the charge and discharge times, which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C2 Figure 4, in the range of 5pF-20pF) from Pin 2 to Pin 7. This capacitor will couple charge into C_t at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from Pin 7 to the reference pin (Pin 6). A 20k pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 4.

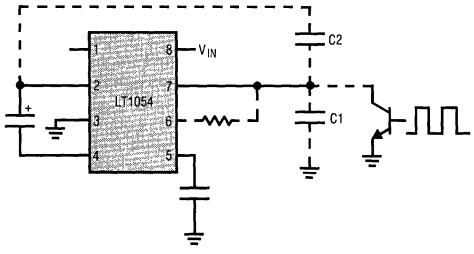


Figure 4

Feedback/Shutdown (Pin 1): This pin has two functions. Pulling Pin 1 below the shutdown threshold (≈0.45V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100μA (see typical curves). Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation the device will start back up when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pull-down to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 would be run intermittently, this does not present a problem because the discharge time of the output capacitor will be short compared to the off time of the device. In applications where the device has to start-up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to Pin 1 of the LT1054. Using the circuit of Figure 5, the restart signal can be either a pulse ($t_p > 100\mu s$) or a logic high. Diode coupling the restart signal into Pin 1 will allow the output voltage to come up and regulate without overshoot. The resistor divider R3/R4 in Figure 5 should be chosen to provide a signal level at Pin 1 of 0.7V-1.1V.

Pin 1 is also the inverting input of the LT1054's error amplifier, and as such can be used to obtain a regulated output voltage.

Regulation

The error amplifier of the LT1054 servoes the drive to the PNP switch to control the voltage across the input capacitor (C_{IN}), which in turn will determine the output voltage. Using the reference and error amplifier of the LT1054, an external resistive divider is all that is needed to set the regulated output voltage. Figure 5 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. The recommended value for R1 is 20k for all output voltages. Frequency compensation is accomplished by adjusting the ratio of C_{IN}/C_{OUT}.

For best results, this ratio should be ≈1/10. C1, required for good load regulation, should be 0.05μF for all output voltages.

It can be seen from the circuit block diagram that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground pin of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations such as the negative doubler can provide higher output voltages at reduced output currents (see typical applications).

APPLICATIONS INFORMATION

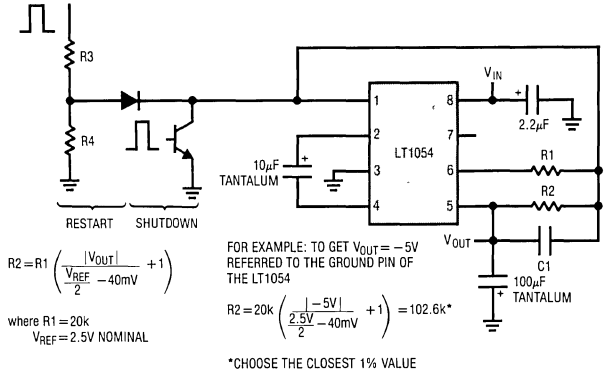


Figure 5

Capacitor Selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good quality, low ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN} the effect of the ESR of the capacitor will be multiplied by four, due to the fact that switch currents are approximately two times higher than output current, and losses will occur on both the charge and discharge cycle. This means that using a capacitor with 1Ω of ESR for C_{IN} will have the same effect as increasing the output impedance of the LT1054 by 4Ω. This represents a significant increase in the voltage losses. For C_{OUT} the affect of ESR is less dramatic. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current, and the ESR of the capacitor will cause a step function to occur, in the output ripple, at the switch transitions. This step function will degrade the output regulation for changes in output load current, and should be avoided. Realizing that large value tantalum capacitors can be expensive, a technique that can be used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost.

Output Ripple

The peak-to-peak output ripple is determined by the value of the output capacitor and the output current. Peak-to-peak output ripple may be approximated by the formula:

$$dV = \frac{I_{OUT}}{2fC_{OUT}}$$

where dV = p-p ripple
f = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is, approximately equal to:

$$(2I_{OUT})(\text{ESR of } C_{OUT})$$

Power Dissipation

The power dissipation of any LT1054 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation must be calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the LT1054 can be calculated from:

$$P \approx (V_{IN} - |V_{OUT}|)(I_{OUT}) + (V_{IN})(I_{OUT})(0.2)$$

where both V_{IN} and V_{OUT} are referred to the ground pin (Pin 3) of the LT1054. For LT1054 regulator circuits, the power dissipation will be equivalent to that of a linear regulator. Due to the limited power handling capability of the LT1054 packages, the user will have to limit output current requirements or take steps to dissipate some power external to the LT1054 for large input/output differentials.

APPLICATIONS INFORMATION

This can be accomplished by placing a resistor in series with C_{IN} as shown in Figure 6. A portion of the input voltage will then be dropped across this resistor, without affecting the output regulation. Because switch current is approximately 2.2 times the output current, and the resistor will cause a voltage drop when C_{IN} is both charging and discharging, the resistor should be chosen as:

$$R_X = V_X/(4.4\ I_{OUT})$$

where

$$V_X \approx V_{IN} - [(\text{LT1054 voltage loss})\ (1.3) + |V_{OUT}|]$$

and I_{OUT} = maximum required output current. The factor of 1.3 will allow some operating margin for the LT1054.

For example: assume a +12V to −5V converter at 100mA output current. First calculate the power dissipation without an external resistor:

$$P = (12V - |-5V|)\ (100mA) + (12V)\ (100mA)\ (0.2)$$
$$P = 700mW + 240mW = 940mW$$

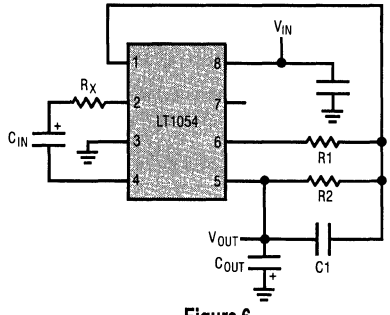


Figure 6

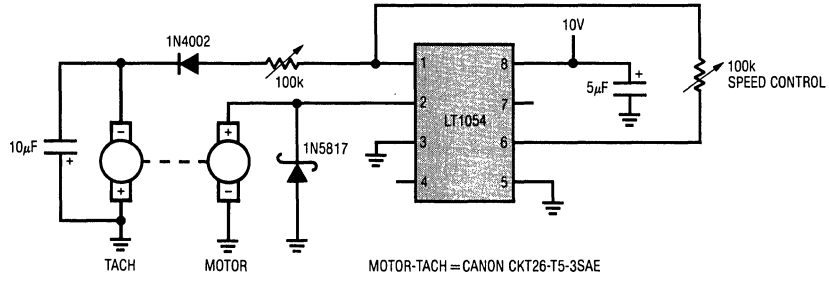
At Θ_{JA} of 130°C/W for a commercial plastic device this would cause a junction temperature rise of 122°C, so that the device would exceed the maximum junction temperature at an ambient temperature of 25°C. Now calculate the power dissipation with an external-resistor (R_X). First find how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100mA output current is 1.6V, so

$$V_X = 12V - [(1.6V)\ (1.3) + |-5V|] = 4.9V \text{ and}$$
$$R_X = 4.9V/(4.4)\ (100mA) = 11\Omega.$$

This resistor will reduce the power dissipated by the LT1054 by (4.9V) (100mA) = 490mW. The total power dissipated by the LT1054 would then be = (940mW − 490mW) = 450mW. The junction temperature rise would now be only 58°C. Although commercial devices are guaranteed to be functional up to a junction temperature of 125°C, the specifications are only guaranteed up to a junction temperature of 100°C, so ideally you should limit the junction temperature to 100°C. For the above example this would mean limiting the ambient temperature to 42°C. Other steps can be taken, however, to allow higher ambient temperatures. The thermal resistance numbers for the LT1054 packages represent worst-case numbers with no heat-sinking and still air. Small clip-on type heat sinks can be used to lower the thermal resistance of the LT1054 package. In some systems there may be some available airflow which will help to lower the thermal resistance. Wide PC board traces from the LT1054 leads can also help to remove heat from the device. This is especially true for plastic packages.

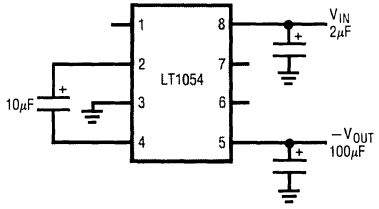
TYPICAL APPLICATIONS

Motor Speed Servo

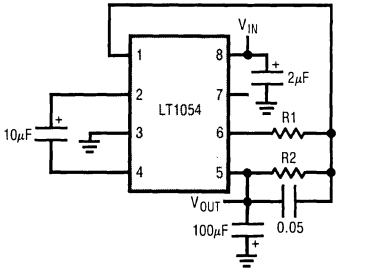


TYPICAL APPLICATIONS

Basic Voltage Inverter

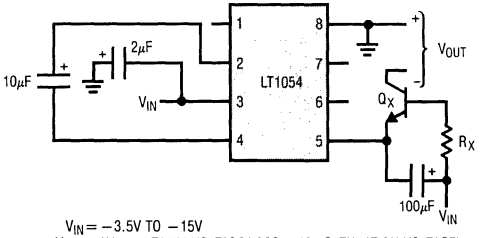


Basic Voltage Inverter/Regulator



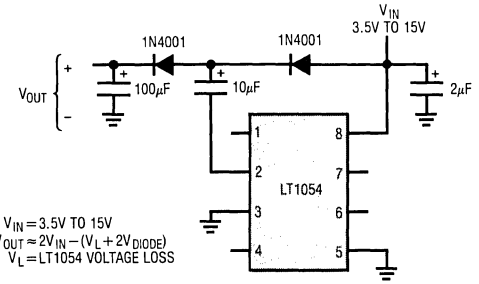
$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = 20k\left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

Negative Voltage Doubler



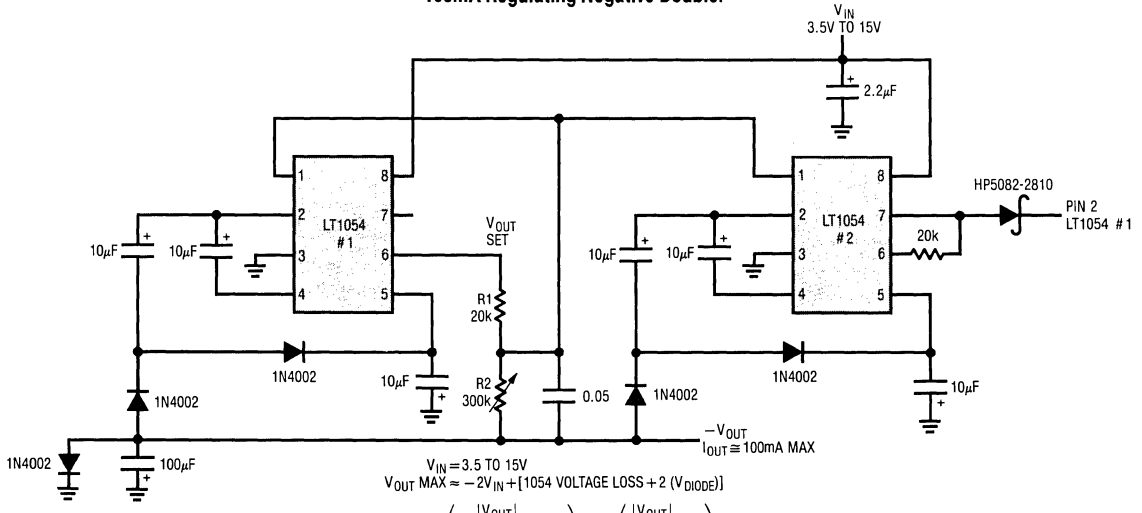
$V_{IN} = -3.5V$ TO $-15V$
$V_{OUT} = 2V_{IN} + (LT1054\ VOLTAGE\ LOSS) + (Q_X\ SATURATION\ VOLTAGE)$

Positive Doubler



$V_{IN} = 3.5V$ TO $15V$
$V_{OUT} \approx 2V_{IN} - (V_L + 2V_{DIODE})$
$V_L = LT1054\ VOLTAGE\ LOSS$

100mA Regulating Negative Doubler

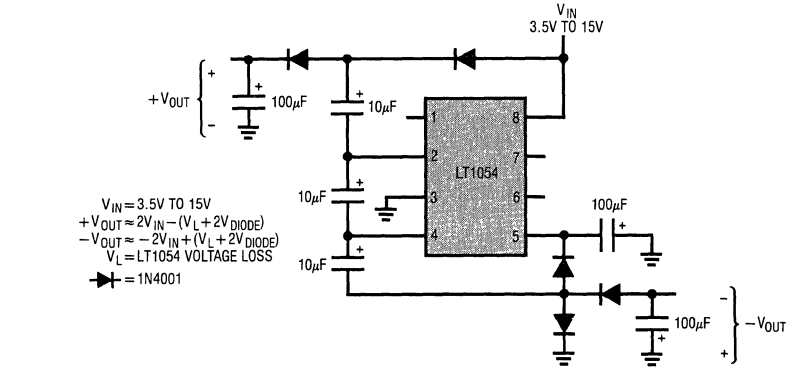


$V_{IN} = 3.5$ TO $15V$
$V_{OUT}\ MAX \approx -2V_{IN} + [1054\ VOLTAGE\ LOSS + 2\ (V_{DIODE})]$

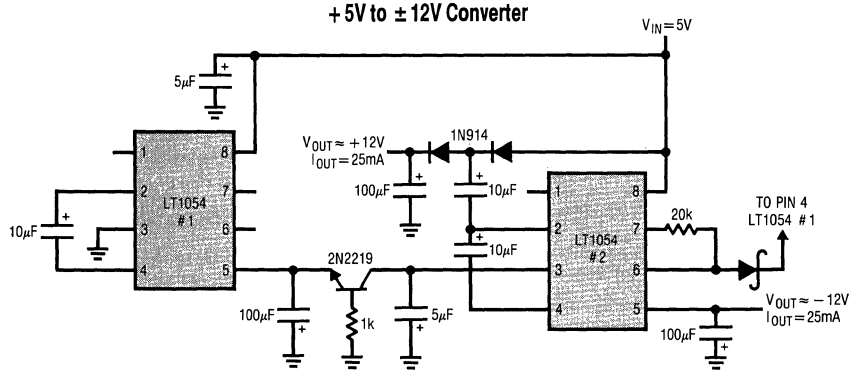
$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

TYPICAL APPLICATIONS

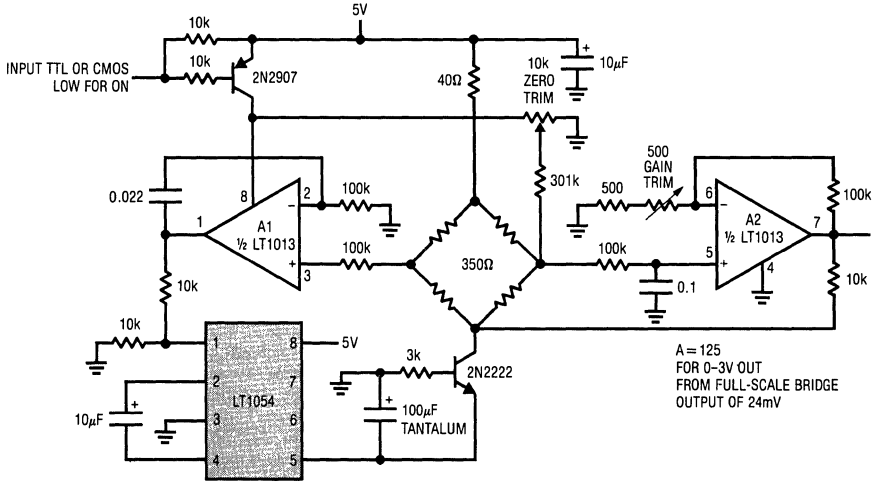
Dual Output Voltage Doubler



+5V to ±12V Converter

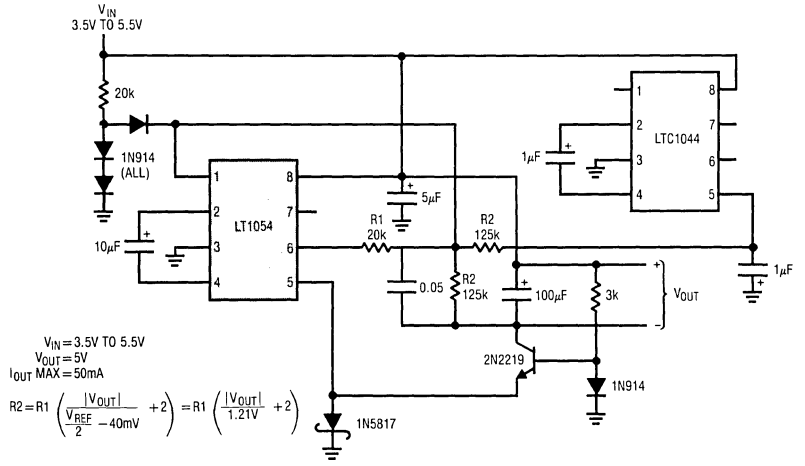


Strain Gage Bridge Signal Conditioner

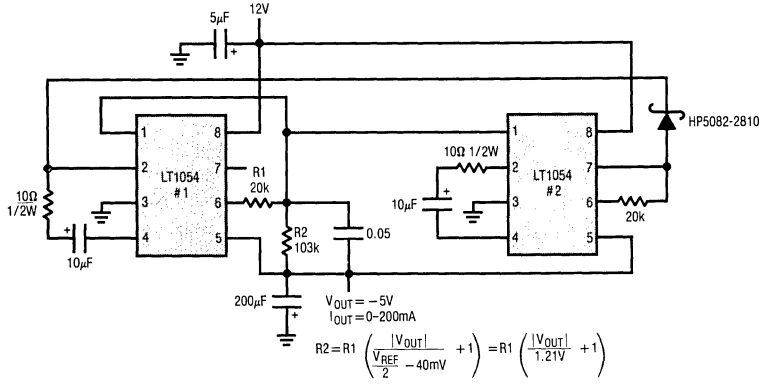


TYPICAL APPLICATIONS

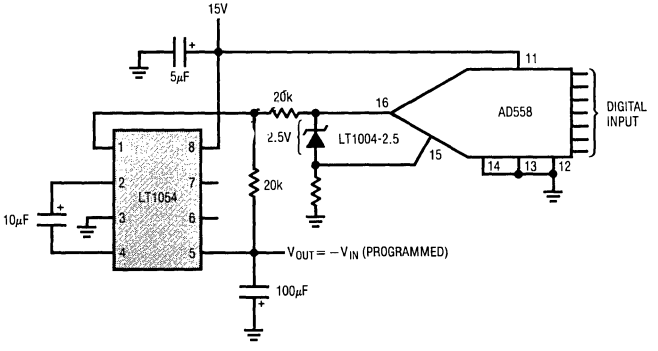
3.5V to 5V Regulator



Regulating 200mA + 12V to − 5V Converter

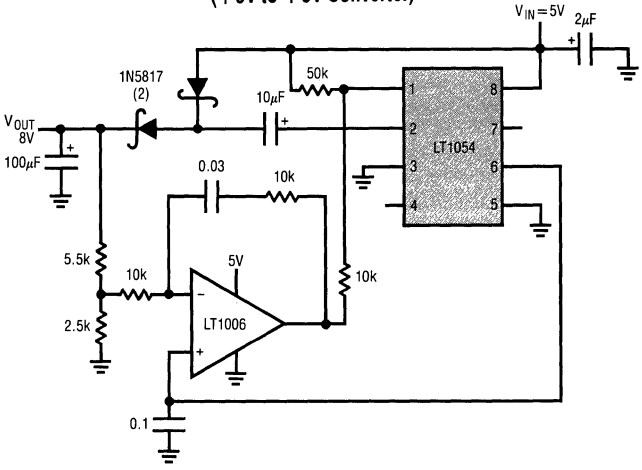


Digitally Programmable Negative Supply

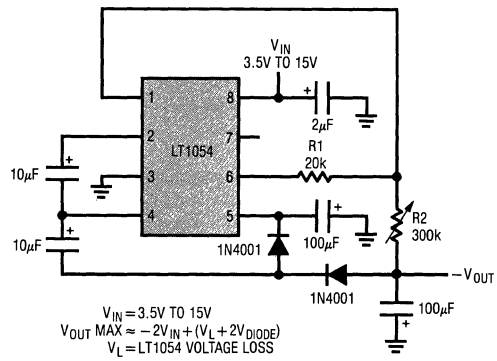


TYPICAL APPLICATIONS

Positive Doubler with Regulation (+5V to +8V Converter)



Negative Doubler with Regulator



$V_{IN} = 3.5V$ TO $15V$

V_{OUT} MAX $\approx -2V_{IN} + (V_L + 2V_{DIODE})$

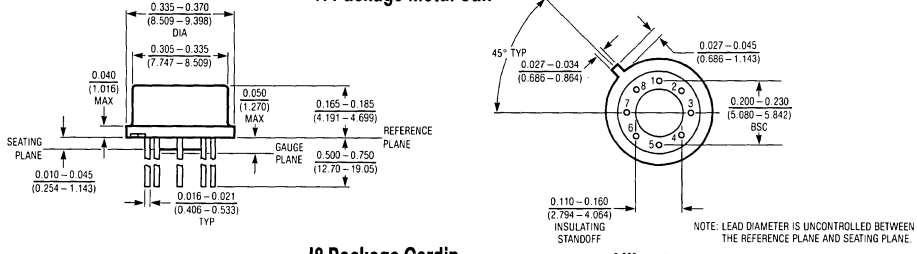
V_L = LT1054 VOLTAGE LOSS

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21V} + 1\right)$$

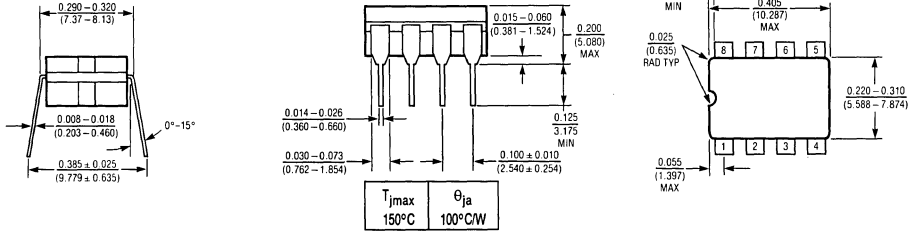
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can

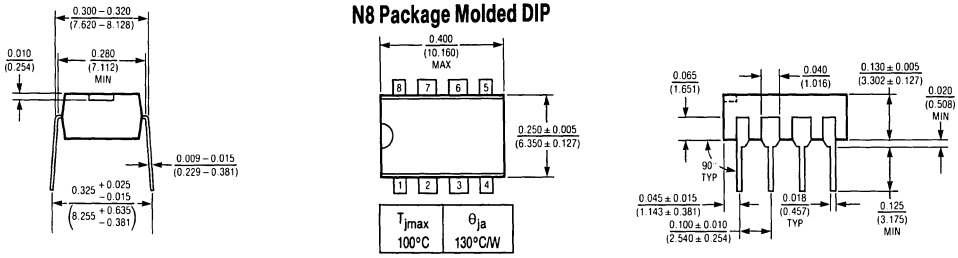


J8 Package Cerdip



T_{jmax}	θ_{ja}
150°C	100°C/W

N8 Package Molded DIP



T_{jmax}	θ_{ja}
100°C	130°C/W

5V Powered RS232 Driver/ Receiver with Shutdown

FEATURES

- Operates on Single 5V Power Supply
- Generates ±9V Supplies with Only 1μF Capacitors
- Fully Protected Against Output Overloads
- RS232 Outputs can be Forced ±30V without Damage
- Three-state Outputs are High Impedance when Off
- Bipolar Circuitry; No Latch Up
- ±30V Receiver Input Range
- Can Power Additional RS232 Drivers such as LT1039
- No Supply Current in Shutdown
- Meets All RS232 Specifications
- 16 Pin Version without Shutdown Available
- Available in SO Package

APPLICATIONS

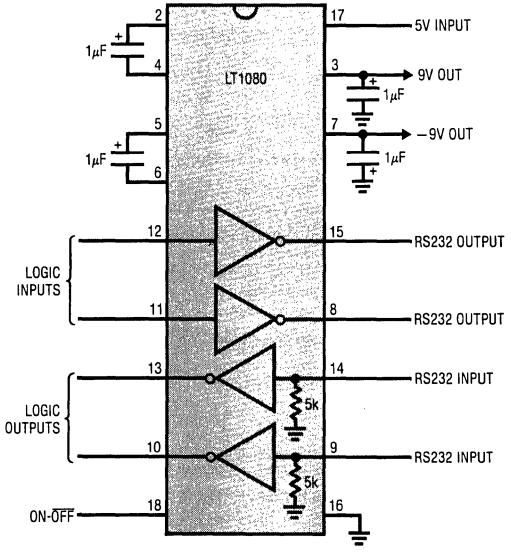
- Portable Computers
- Battery Powered RS232 Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

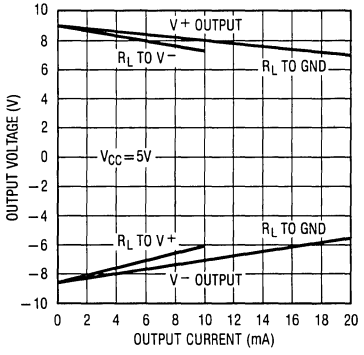
The LT1080 is a dual RS232 driver/receiver which includes a capacitive voltage generator to supply RS232 voltage levels from a single 5V supply. Each receiver will accept up to ±30V input and can drive either TTL or CMOS logic. The RS232 drivers accept logic inputs and output RS232 voltage levels. The driver outputs are fully protected against overload and can be shorted to ground or up to ±30V without damage. Additionally, when the system is in the SHUTDOWN mode the driver and receiver outputs are at a high impedance allowing data line sharing. Bipolar circuitry makes this driver/receiver exceptionally rugged against overloads or ESD damage.

The power supply generator doubles the 5V input supply to obtain 9V, and then inverts the 9V to obtain −8.5V. Up to 15mA of external current is available to power additonal RS232 drivers or other external circuitry. The SHUTDOWN mode disables the supply generators and reduces input supply current to zero. A version of the LT1080, the LT1081, is available without shutdown for 16 pin applications.

TYPICAL APPLICATION



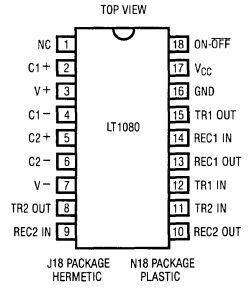
Supply Generator Outputs

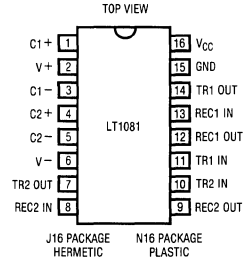


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
V^+ 12V
V^- ..... −12V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
  On-$\overline{Off}$ Pin ..... GND to 12V
Output Voltage
  Driver ..... V^- + 30V to V^+ − 30V
  Receiver ..... −0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 Seconds
  V^- ..... 30 Seconds
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1080M ..... −55°C to 125°C
  LT1080C ..... 0°C to 70°C
  Guaranteed Functional ..... −25°C to 85°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION





ORDER PART NUMBER
LT1080MJ LT1080CJ LT1080CN
LT1081MJ LT1081CJ LT1081CN AVAILABLE IN SO PACKAGE

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5.0	7.3		V
	Both Outputs.	Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} \geq 2.0V$		●		5	20	μA
	$V_{IN} \leq 0.8V$		●		5	20	μA
Output Short Circuit Current	Sourcing Current, V_{OUT} = 0V			7	12		mA
	Sinking Current, V_{OUT} = 0V			−7	−12		mA
Output Leakage Current	SHUTDOWN (Note 2), V_{OUT} = ±30V		●		10	100	μA
Slew Rate	R_L = 3kΩ, C_L = 51pF			4	15	30	V/μs
Receiver							
Input Voltage Thresholds	Input Low Threshold, (V_{OUT} = High)		●	0.2	1.3		V
	Input High Threshold, (V_{OUT} = Low)		●		1.7	3.0	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance				3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA		●		0.2	0.4	V
	Output High, I_{OUT} = 160μA (V_{CC} = 5V)		●	3.5	4.8		V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−10	−20		mA
	Sourcing Current, V_{OUT} = 0V			0.6	1		mA
Output Leakage Current	SHUTDOWN (Note 2), $0V \leq V_{OUT} \leq V_{CC}$		●		1	10	μA

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Generator (Note 3)							
V+ Output Voltage	I_{OUT} = 0mA			8	9		V
	I_{OUT} = 10mA			7	8		V
	I_{OUT} = 15mA			6.5	7.5		V
V− Output Voltage	I_{OUT} = 0mA			−7.5	−8.5		V
	I_{OUT} = −10mA			−5.5	−6.5		V
	I_{OUT} = −15mA			−5	−6		V
Supply Current			●		10	22	mA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 2)	(LT1080 Only)	●		1	100	μA
On-$\overline{Off}$ Pin Current	$0V \le V_{ON\text{-}\overline{OFF}} \le 5V$	(LT1080 Only)	●	−15		80	μA
Supply Rise Time	(Note 4)	(LT1080 Only)			1		ms

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade or $-55°C \le T_A \le 125°C$ for military grade devices). The LT1080/LT1081 is guaranteed functional by design for $-25°C \le T_A \le 85°C$.

Note 1: These parameters apply for $4.5V \le V_{CC} \le 5.5V$ and $V_{ON\text{-}\overline{OFF}} = 3V$, unless otherwise specified.

Note 2: $V_{ON\text{-}\overline{OFF}} = 0.4V$ for $-55°C \le T_A \le 100°C$, and $V_{ON\text{-}\overline{OFF}} = 0.2V$ for $100°C \le T_A \le 125°C$. (LT1080 only)

Note 3: Unless otherwise specified, $V_{CC} = 5V$, external loading of V+ and V− equals zero and the driver outputs are low (inputs high).

Note 4: Time from either SHUTDOWN high or power on until $V+ \ge 6V$ and $V- \le -6V$. All external capacitors are 1μF.

PIN FUNCTIONS

V_{CC} (Pin 17): Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND (Pin 16): Ground pin.

On-$\overline{Off}$ (Pin 18): Controls the operation mode of the LT1080 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V+ (Pin 3): Positive supply for RS232 drivers. $V+ \approx 2V_{CC} - 1.5V$. Requires an external capacitor (≥1μF) for charge storage. May be loaded (up to 15mA) for external system use. Loading does reduce V+ voltage (see graphs.) Capacitor may be tied to ground or +5V input supply.

V− (Pin 7): Negative supply for RS232 drivers. $V- \approx -(2V_{CC} - 2.5V)$. Requires an external capacitor (≥1μF) for charge storage. May be loaded (up to −15mA) for external system use. Loading does reduce V− voltage (see graphs).

TR1 IN; TR2 IN (Pins 12, 11): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT; TR2 OUT (Pins 15, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off ($V_{CC} = 0V$) to allow data line sharing. Outputs are fully short circuit protected from V− +30V to V+ −30V with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than ±45V and higher applied voltages will not damage the device if moderately current limited.

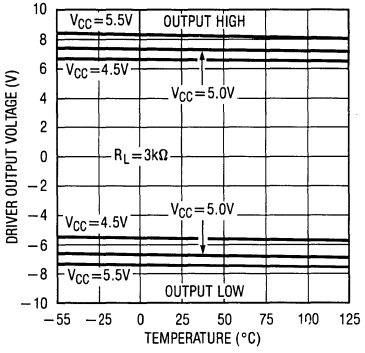
REC1 IN; REC2 IN (Pins 14, 9): Receiver inputs. Accepts RS232 voltage levels (±30V) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5kΩ.

REC1 OUT; REC2 OUT (Pins 13, 10): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

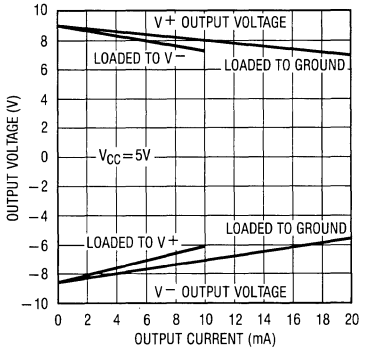
C1+; C1−; C2+; C2− (Pins 2, 4, 5, 6): No user applications. Requires an external capacitor (≥1μF) from C1+ to C1− and another from C2+ to C2−.

TYPICAL PERFORMANCE CHARACTERISTICS

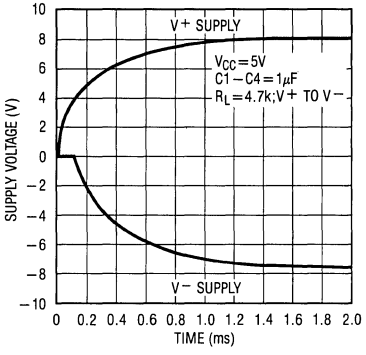
Driver Output Voltage



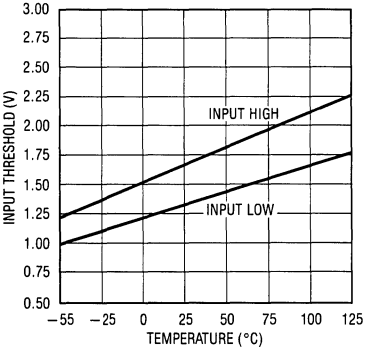
Supply Generator Outputs



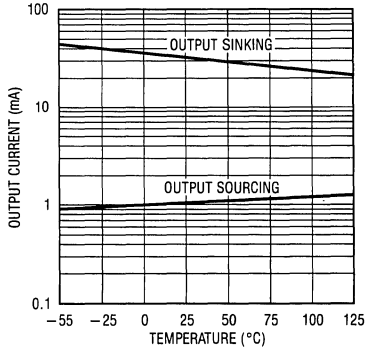
Supply Generation from V_{CC} or Shutdown



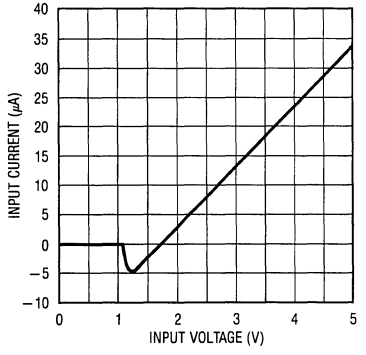
Receiver Input Thresholds



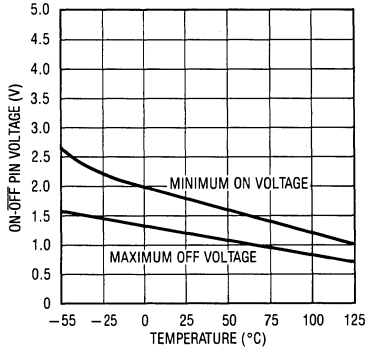
Receiver Output Short Circuit Current



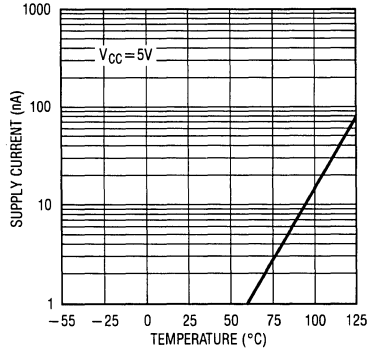
On-$\overline{\text{Off}}$ Pin Current vs Voltage



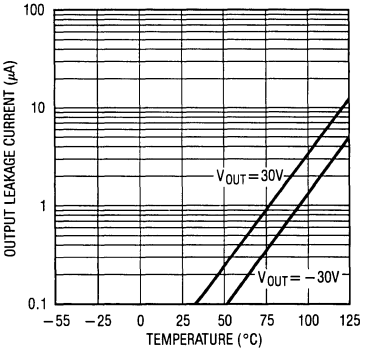
On-$\overline{\text{Off}}$ Pin Thresholds



Supply Current in Shutdown

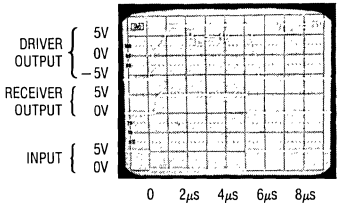


Driver Output Leakage in Shutdown

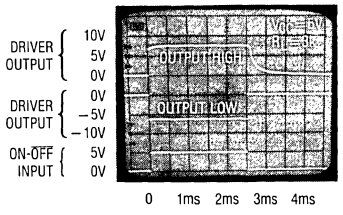


TYPICAL PERFORMANCE CHARACTERISTICS

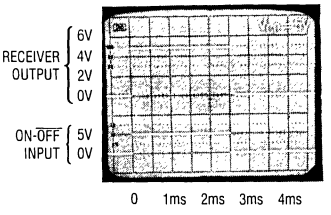
Output Waveforms



Shutdown to Driver Output

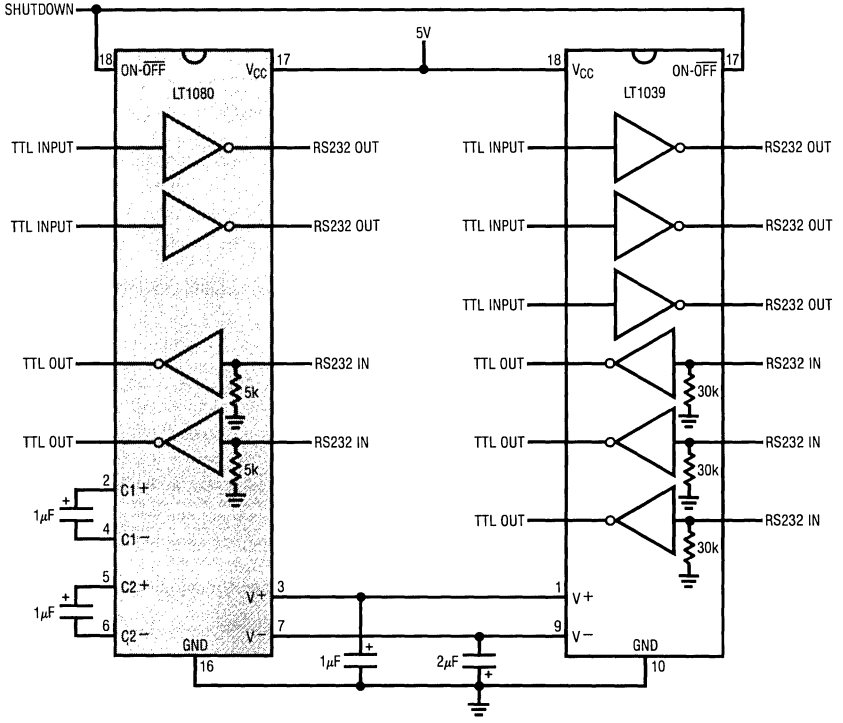


Shutdown to Receiver Output



TYPICAL APPLICATION

Supporting an LT1039 (Triple Driver/Receiver)



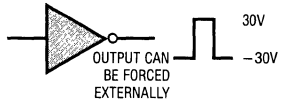
APPLICATION HINTS

The driver output stage of the LT1080 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to ±30V with no damage or excessive current flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

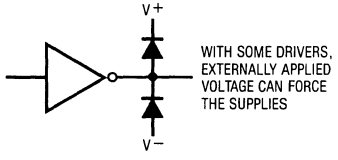
Placing the LT1080 in the SHUTDOWN mode (Pin 18 low) puts both the driver and receiver outputs in a high impedance state. This allows data line sharing and transceiver applications.

The SHUTDOWN mode also drops input supply current (V_{CC}; Pin 17) to zero for power-conscious systems.

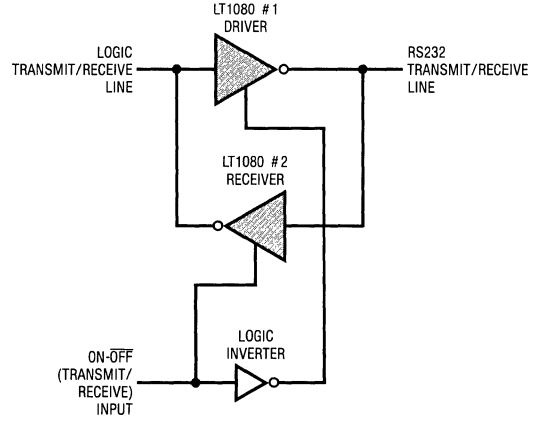
LT1080/LT1081 Driver



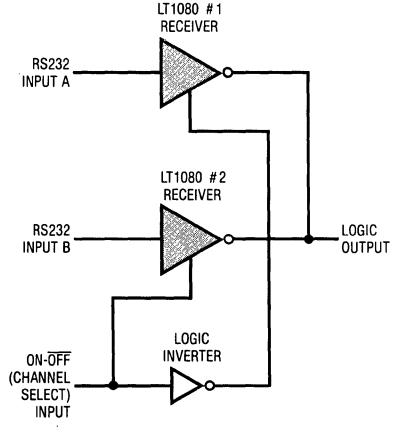
Older RS232 Drivers and CMOS Drivers



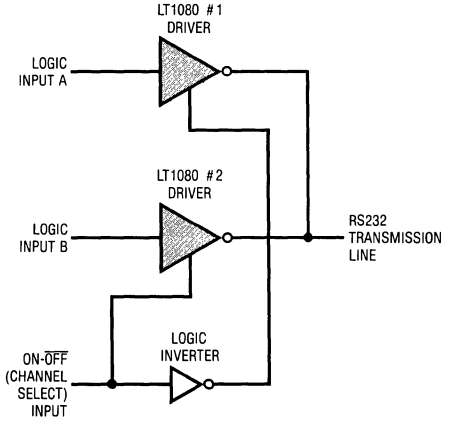
Transceiver



Sharing a Receiver Line

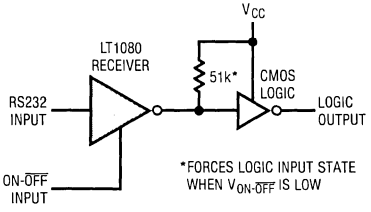


Sharing a Transmitter Line

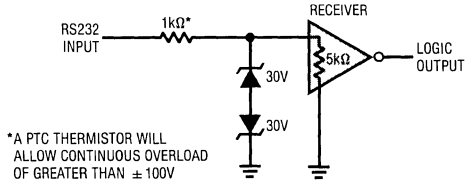


APPLICATION HINTS

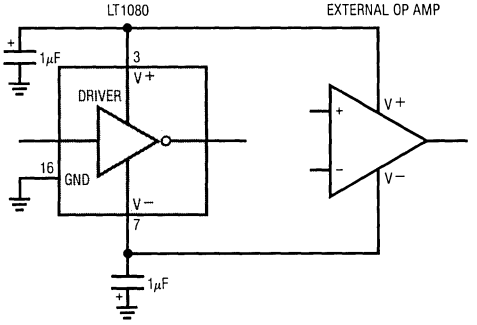
When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.



To protect against receiver input overloads in excess of ±30V, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.

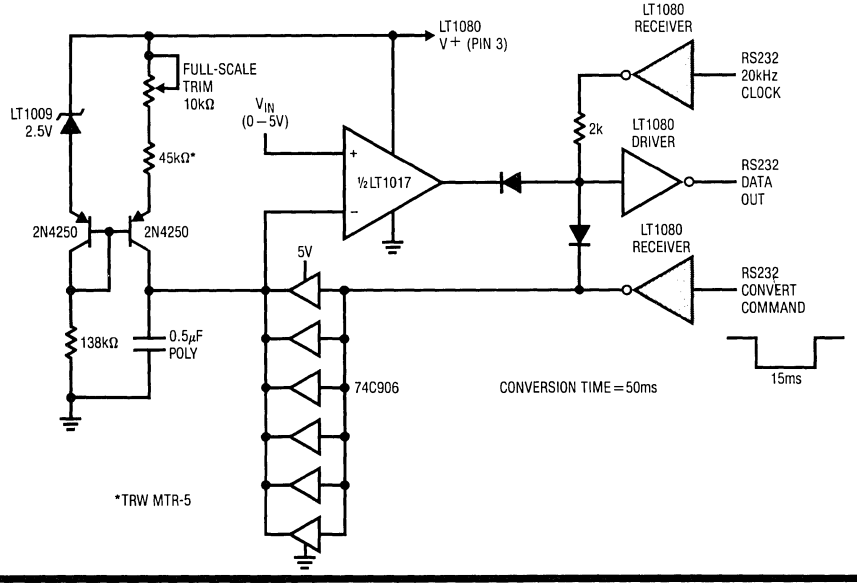


The generated driver supplies (V+ and V−) may be used to power external circuitry such as other RS232 drivers or op amps. They should be loaded with care, since excessive loading can cause the generated supply voltages to drop causing the RS232 driver output voltages to fall below RS232 requirements. See the graph "Supply Generator Outputs" for a comparison of generated supply voltage versus supply current.



TYPICAL APPLICATION

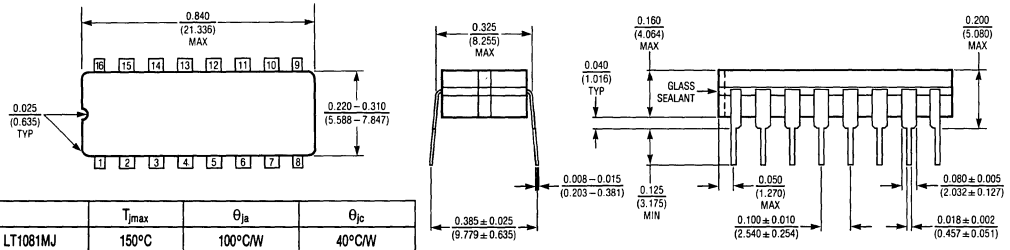
RS232 Compatible 10-Bit A-D Converter



PACKAGE DESCRIPTION

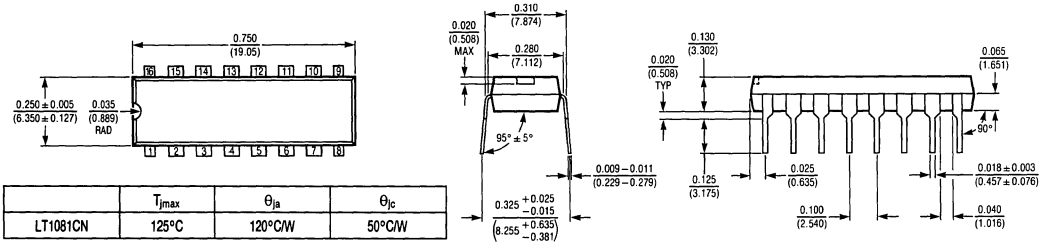
Dimensions in inches (millimeters) unless otherwise noted.

J16 Package Ceramic DIP



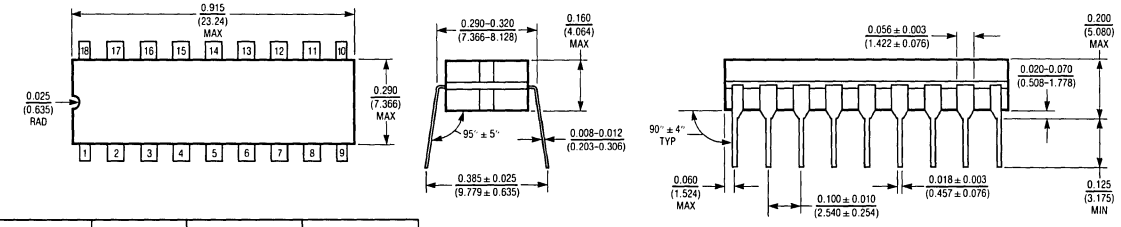
	T_{jmax}	θ_{ja}	θ_{jc}
LT1081MJ	150°C	100°C/W	40°C/W
LT1081CJ	150°C	100°C/W	40°C/W

N16 Package Plastic DIP



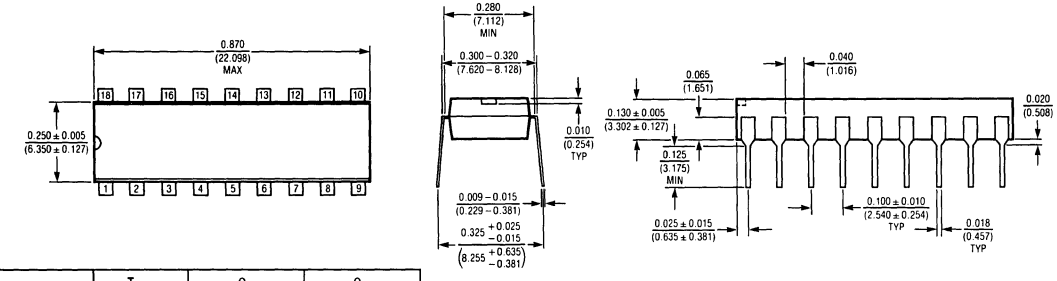
	T_{jmax}	θ_{ja}	θ_{jc}
LT1081CN	125°C	120°C/W	50°C/W

J18 Package Ceramic DIP



	T_{jmax}	θ_{ja}	θ_{jc}
LT1080MJ	150°C	100°C/W	40°C/W
LT1080CJ	150°C	100°C/W	40°C/W

N18 Package Plastic DIP



	T_{jmax}	θ_{ja}	θ_{jc}
LT1080CN	125°C	120°C/W	50°C/W

Wideband RMS-DC Converter Building Block

FEATURES

- 300MHz 3dB Bandwidth
- 1% Accuracy DC-50MHz
- 2% to 100MHz
- Bandwidth Flat Over Input Voltage Range
- 50:1 Crest Factor
- 20:1 Dynamic Range
- 35V Peak Input
- Thermally Based Operation
- Fully Specified Thermal and Electrical Parameters
- Standard IC Package
- Resistive Inputs

APPLICATIONS

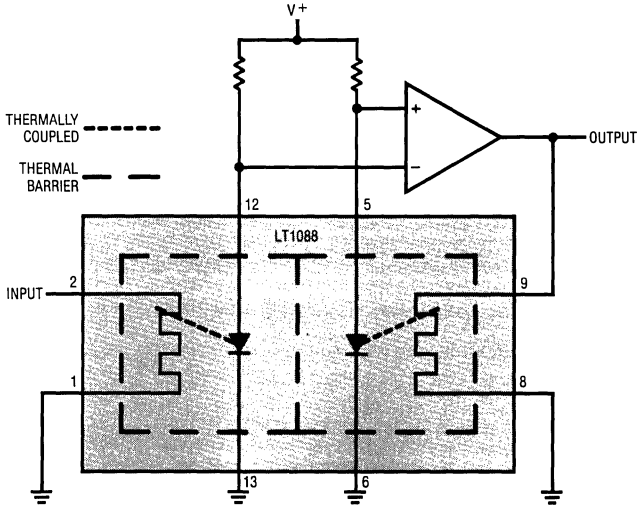
- Wideband RMS Voltmeters
- RF Leveling Loops
- Wideband AGC
- High Crest Factor Measurements
- SCR Power Monitoring

DESCRIPTION

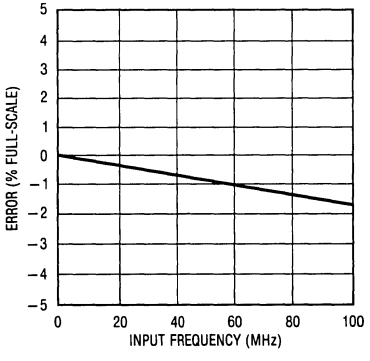
The LT1088 is a thermally based RMS-DC converter building block. It converts the input waveform to heat. Using external circuitry, the thermal signal is expressed as a DC output voltage.

LTC's proprietary thermal packaging process permits accurate thermal signal processing in a standard IC package. The thermal method provides far greater bandwidth than RMS converters based on logarithmic computing techniques. The LT1088's high voltage breakdown allows crest factor measurements of 50:1 and operation over a 20:1 input dynamic range. Resistive inputs of 50Ω or 250Ω accommodate drive from a wide variety of sources.

Simplified RMS-DC Converter



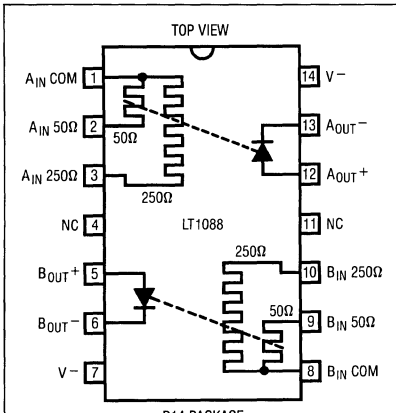
Accuracy vs Frequency (50Ω Input)



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin ..... V⁻ + 40V to V⁻
Voltage from Channel A to Channel B 100V
Reverse Diode Voltage..... 3.5V
Forward Diode Current 15mA
Input Power (25°C)..... 0.375W
Peak Input Power (30 sec) 0.435W
Derate Power at – 3mW/°C above 25°C
Maximum Die Temperature..... 150°C
Peak Die Temperature (30 sec)..... 175°C
Functional Temperature Range..... – 55°C to 125°C
Operating Temperature Range..... – 40°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1088CD

ELECTRICAL CHARACTERISTICS T_A = 25°C, unless otherwise noted (See Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Heaters						
50Ω Input			40	50	60	Ω
250Ω Input			200	250	300	Ω
50Ω Temperature Coefficient		●		2000		ppm/°C
250Ω Temperature Coefficient		●		2000		ppm/°C
50Ω Temperature Coefficient Match	Input A to Input B	●		30	500	ppm
250Ω Temperature Coefficient Match	Input A to Input B	●		30	500	ppm
Resistance Matching	50Ω Inputs 250Ω Inputs			2 2	10 10	% %
250Ω to 50Ω Ratio Match			– 15	0	5	%
250Ω to 50Ω Ratio Match Temperature Coefficient		●		50		ppm/°C
Output Diodes						
Forward Voltage	I = 5mA		0.6	0.7	0.8	V
Forward Voltage Match	Out A to Out B; I = 5mA	●		5		mV
Voltage Temperature Coefficient	I = 5mA	●	– 1.6	– 1.75	– 1.9	mV/°C
Thermal Characteristics						
Thermal Resistance	Either Die to Ambient	●	200	300	400	°C/W
Thermal Matching	Channel A to Channel B	●		30		°C/W
Thermal Cross Talk	Channel A to Channel B	●		2500		°C/W

The ● denotes specifications which apply over full operating temperature range.

Note 1: All electrical testing conducted at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4's Response vs Frequency—50Ω Input

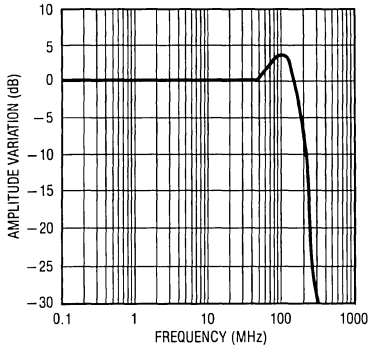
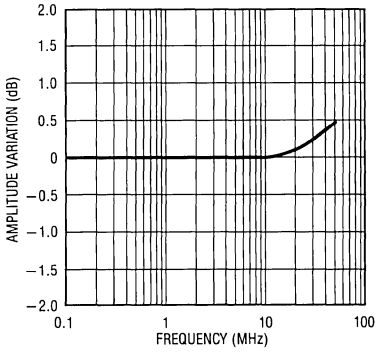
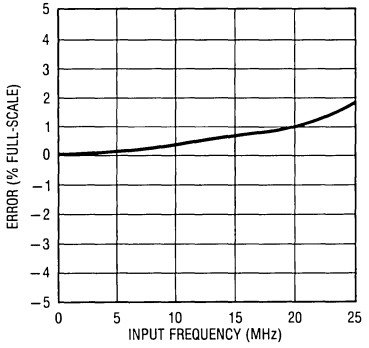


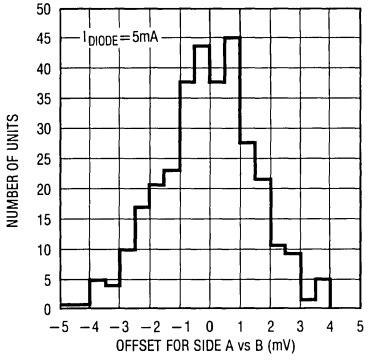
Figure 4's Response vs Frequency—250Ω Input



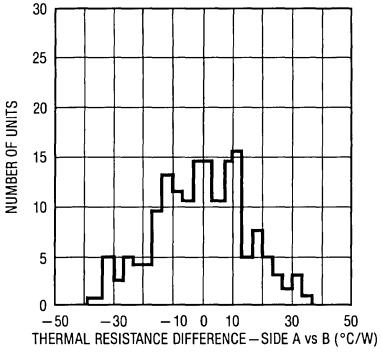
Accuracy vs Frequency for Figure 4—250Ω Input



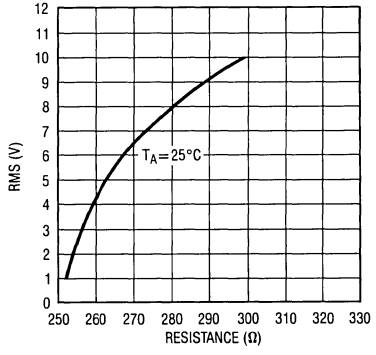
Distribution of Diode Offset Voltage



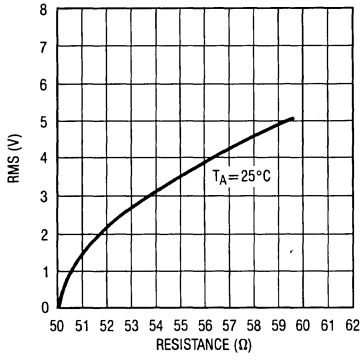
Distribution of Thermal Resistance



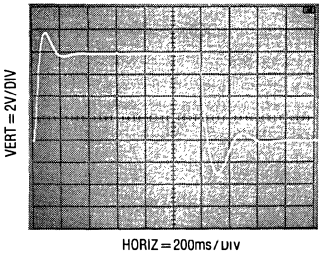
Heater Resistance vs RMS Volts—250Ω Heater



Heater Resistance vs RMS Volts—50Ω Heater



Figures 4's Settling Time



APPLICATIONS INFORMATION

Pin Functions

A_{IN} 50Ω, B_{IN} 50Ω, A_{IN} 250Ω, B_{IN} 250Ω (Pins 2, 9, 3, 10): Heater input pins. Input and servo amplifier are connected to these pins. Since the LT1088 is symmetrical, either channel A or B may be used as the input. For higher input impedance, the 50Ω and 250Ω heaters may be series connected. No heater pin may be below V^- or more than 40V above V^-. Maximum heater dissipation must not exceed the absolute maximum ratings.

A_{IN} COM, B_{IN} COM (Pins 1, 8): Common point for the 50Ω and 250Ω input heaters, usually tied to ground.

A_{OUT}^+, B_{OUT}^+ (Pins 12, 5): High side of the temperature sensing diodes. Normally they are driven at 5mA from the positive supply. No diode pin may be below V^- or more than 40V above V^-.

A_{OUT}^-, B_{OUT}^- (Pins 13, 6): Low side of the temperature sensing diodes. These pins are normally tied to ground. No diode pin may be below V^- or more than 40V above V^-.

V^- (Pins 7, 14): These pins must be the most negative potential of the circuit, usually tied to ground.

Parasitic Diodes

As with all bipolar ICs the LT1088 contains parasitic diodes which must not be forward biased. The parasitic diodes, marked with asterisks, appear in Figure 1. The dashed lines indicate that all points of the heaters are parasitically diode connected to V^-.

Thermal Considerations

Because the LT1088's operation depends on thermal symmetry, it is sensitive to external temperature gradients. This is particularly the case for small inputs, which cause the device to run very close to ambient temperature. The device should be mounted in an area which is isothermal and free of drafts. Power generating components should be kept away from the LT1088 and particular caution taken in fan cooled equipment. Under normal conditions no thermal baffle or enclosure is required. Under no circumstances should a heat sink be used.

Heater Protection

Most LT1088 failures will be caused by excessive heater drive. Input power (25°C) is specified at 375mW with 30 second excursions to 435mW permitted. These figures are derated by –3mW/°C above 25°C. Figure 2 plots safe operating limits for input duty cycle vs input voltage. Accidental heater overdrives can damage or destroy the LT1088. In situations where overdrive may occur, some form of heater protection should be employed. Suggested circuits appear in the applications section.

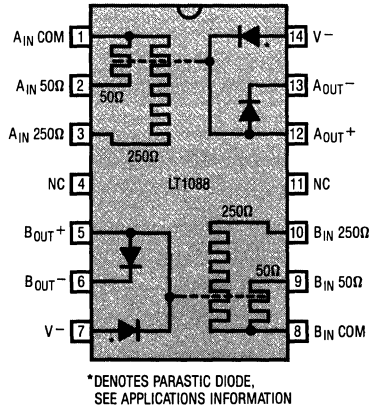


Figure 1

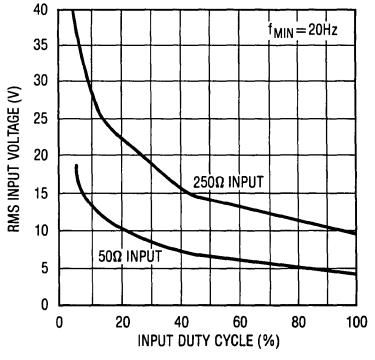


Figure 2. Safe Operating Limits

APPLICATIONS INFORMATION

Filtering

The LT1088's thermal time constant provides effective low pass filtering. Low frequency cut-off is set by servo loop time constants. For the 3300pF value given in the basic RMS-DC application, the circuit begins to follow the input below about 50Hz. Normally, this is not a problem, because the LT1088's primary application will be at high frequency. Lower frequency operation is obtainable by increasing the 3300pF value, although settling time will increase proportionally.

Crest Factor

Crest factor is defined as the ratio of peak input voltage to RMS value. Crest factor performance is set by IC breakdown limits and the usable low input power range. Breakdown limits are a function of processing. The usable low input power range is a basic signal-to-noise conflict. Low input power produces small amounts of signal. This makes accurate, stable discrimination between desired inputs and ambient thermal phenomena uncertain and noisy. These constraints set crest factor at 50:1 for the 50Ω input and 40:1 for the 250Ω input.

Layout

At frequencies above 10MHz, input connections require care. Parasitic inductance builds quickly in wire runs, so the LT1088's input heater lead should be *directly* connected to the source to be measured. It is also wise to shield the input line from the rest of the circuit. The heater common should be returned directly to a ground plane. An additional precaution is to mount the 0.01μF bypass capacitors right at the LT1088 package. These units minimize the effects of RF pick-up by the temperature sensing diodes.

Accuracy

Amplitude measurement at high frequency to significant accuracy is difficult because of parasitic effects. At frequencies much above 5MHz, small parasitic capacitive and inductive terms become important. The accuracy figures quoted for the applications circuits were taken against certified standards utilizing direct and transfer techniques. Thermal transfer standards (Fluke Model 540B with A-55 converters) certified to 50MHz were used as references. The data above 50MHz was also taken with these references, although the individual units used had not been certified at these frequencies. The accuracy of units of this type which have been certified is normally inside the tolerances listed, so there is good probability the data is valid.

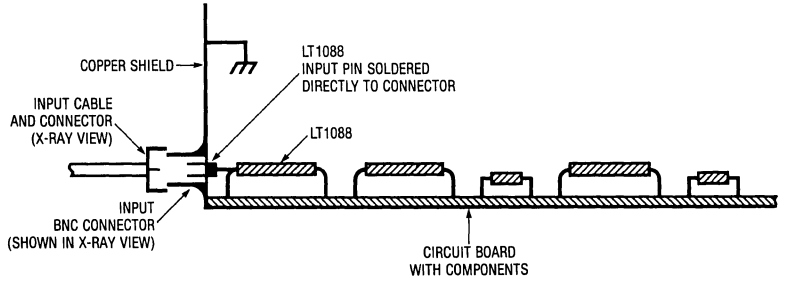


Figure 3. Typical Evaluation Layout

APPLICATIONS INFORMATION

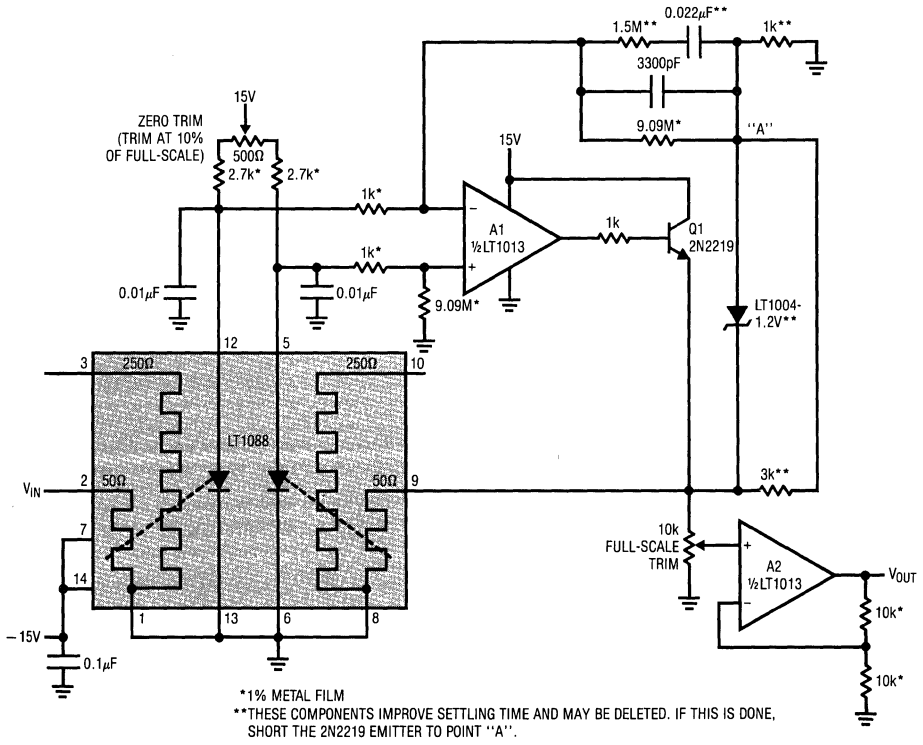


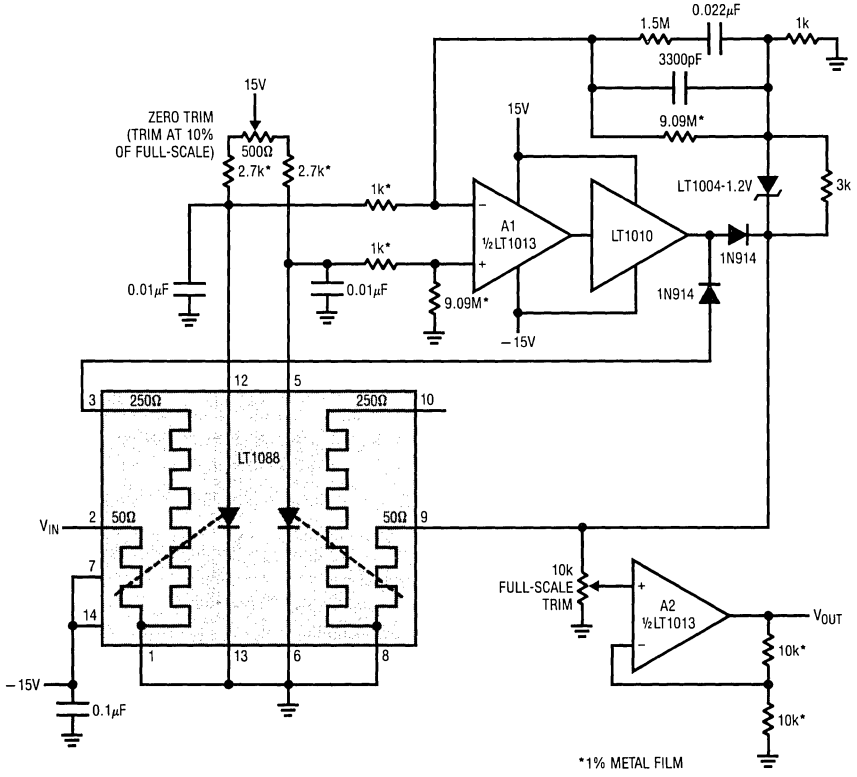
Figure 4. Basic RMS-DC Converter

Figure 4's Typical Specifications

Accuracy:	
50Ω Input	
DC to 50MHz	1% FS
DC to 100MHz	2% FS
250Ω Input	
DC to 20MHz	1% FS
Temperature Effect on Accuracy	100ppm/°C
Dynamic Range	20:1
Crest Factor:	
50Ω Input	50:1
250Ω Input	40:1
3dB Bandwidth	300MHz
Full-Scale Settling Time (1%)	500ms
Input Voltage Range (25°C)	
50Ω Input	4.25V
250Ω Input	9.5V

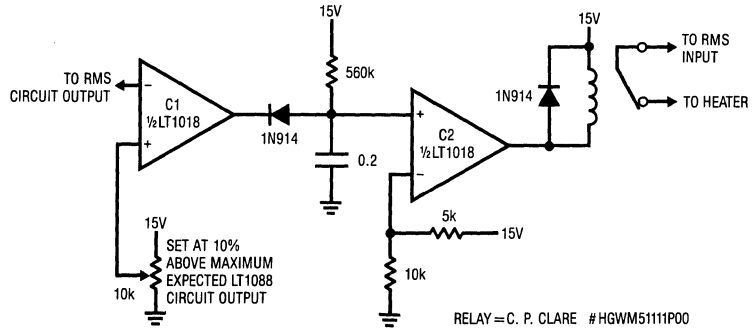
APPLICATIONS

Fast Settling RMS-DC Converter

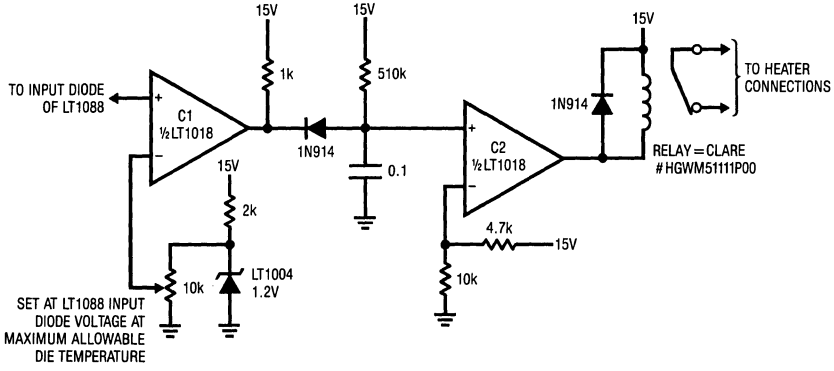


APPLICATIONS

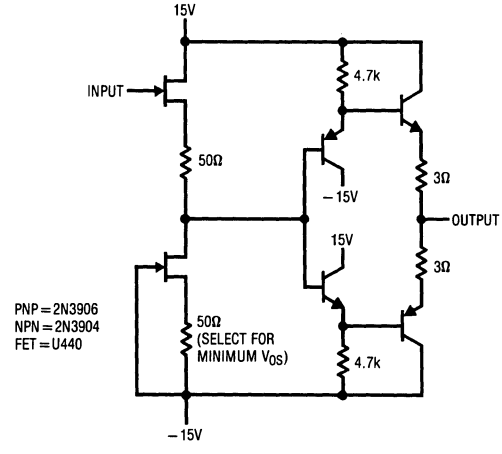
Servo-Sensed Heater Protection Circuit (≈50ms Response)



Diode Sensed Heater Protection Circuit (≈15ms Response)

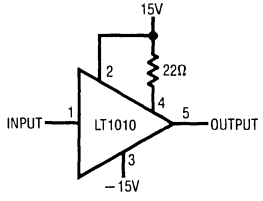


Discrete Input Buffer for the LT1088

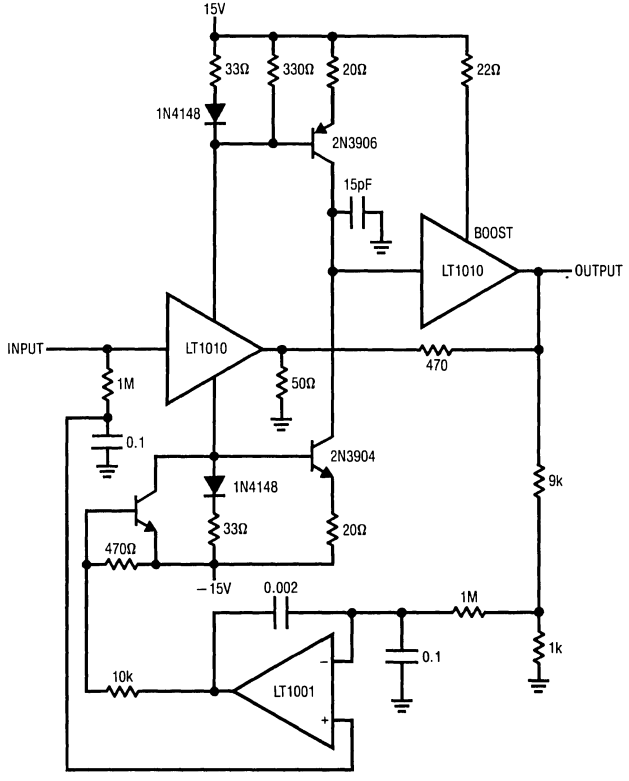


APPLICATIONS

LT1010 Buffer†



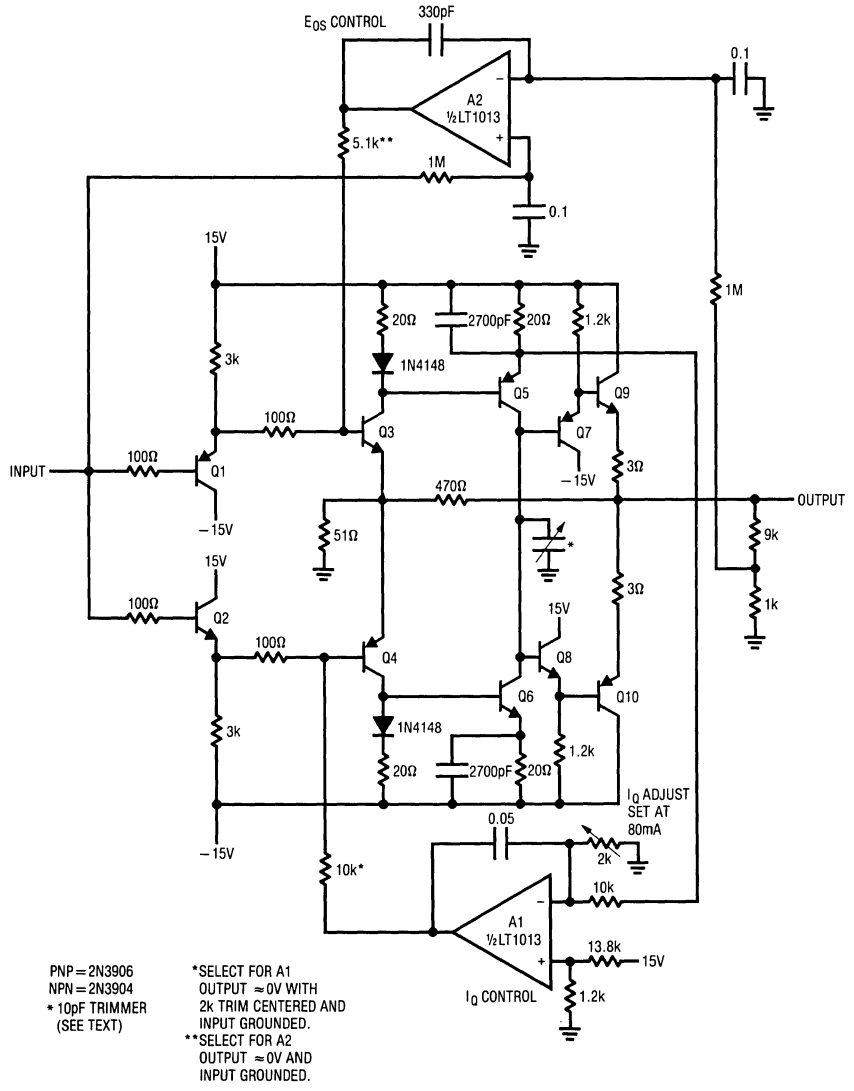
LT1010 Buffer with Gain of 10†



† See Summary of Buffer Characteristics table for buffer speed.

APPLICATIONS

Wideband Discrete Buffer with Gain = 10†



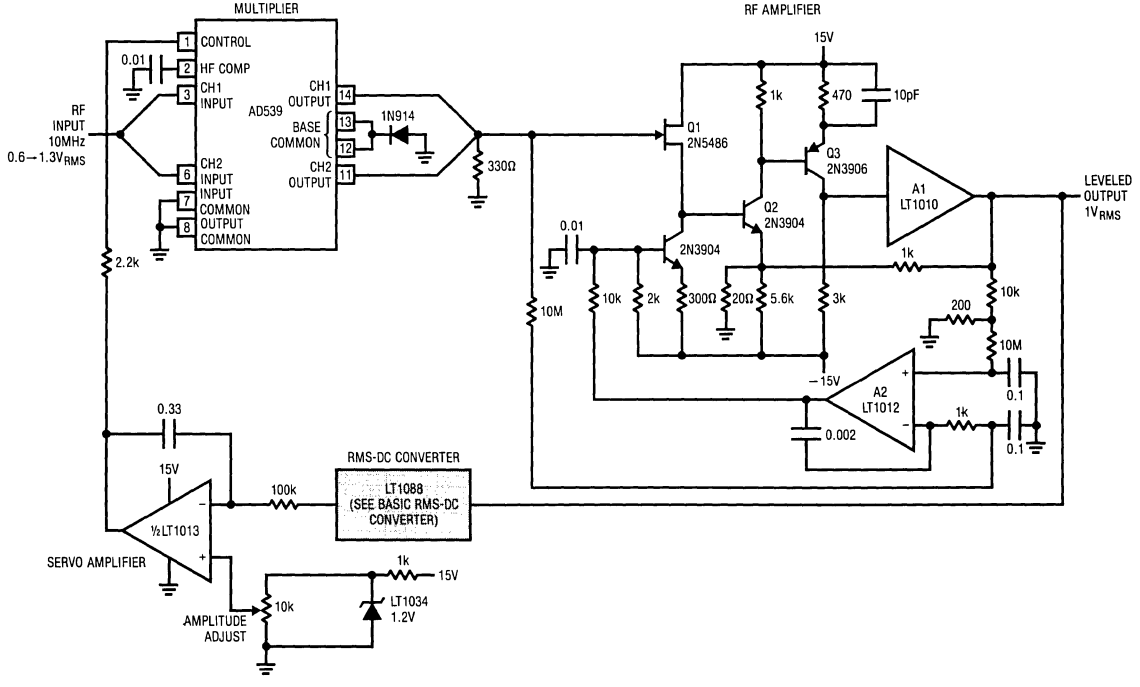
† See Summary of Buffer Characteristics table for buffer speed.

APPLICATIONS

Summary of Buffer Characteristics

Type of Buffer	Slew Rate	1% Error Bandwidth	
		250Ω Load ($\pm 10V_{OUT}$)	50Ω Load ($\pm 5V_{OUT}$)
Discrete—A = 10	3000V/μs	25MHz	32MHz
LT1010 Based—A = 10	100V/μs	0.75MHz	2MHz
Discrete—A = 1	2000V/μs	15MHz	25MHz
LT1010 Based—A = 1	100V/μs	0.75MHz	2MHz

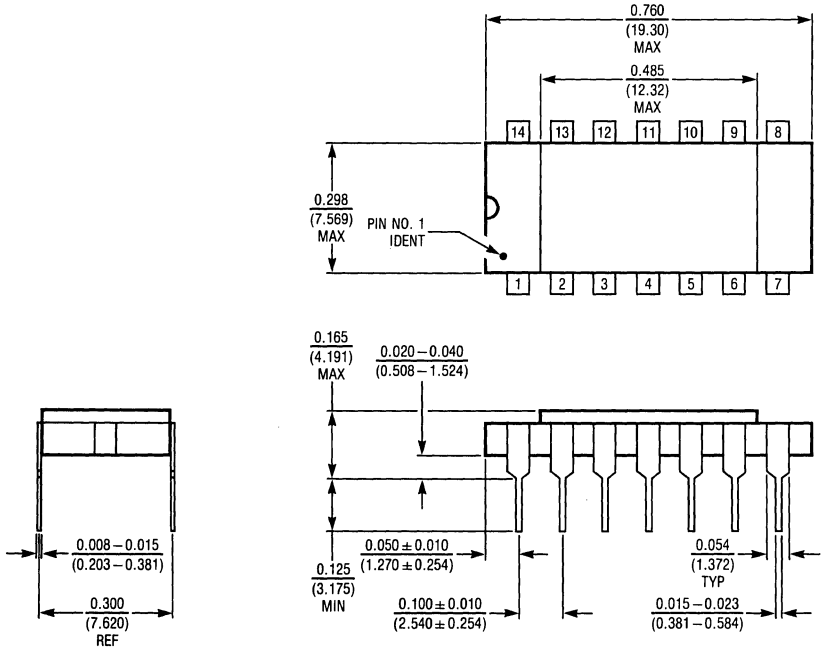
RF Leveling Loop



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

D14 Package
Hermetic DIP (Sidebrazed)



Single Chip 10-Bit Data Acquisition System

FEATURES

- Software Programmable Features:
  - Unipolar/Bipolar Conversions
  - 4 Differential/8 Single Ended Inputs
  - MSB or LSB First Data Sequence
  - Variable Data Word Length
- Built-In Sample and Hold
- Single Supply 5V, 10V or ±5V Operation
- Direct 4 Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 30kHz Maximum Throughput Rate

KEY SPECIFICATIONS

■ Resolution	10 Bits
■ Total Unadjusted Error (LTC1090A)	±1/2LSB Max
■ Conversion Time	22μs
■ Supply Current	2.5mA Max, 1.0mA Typ

DESCRIPTION

The LTC1090 is a data acquisition component which contains a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform either 10-bit unipolar, or 9-bit plus sign bipolar A/D conversions. The 8-channel input multiplexer can be configured for either single ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single ended input channels.

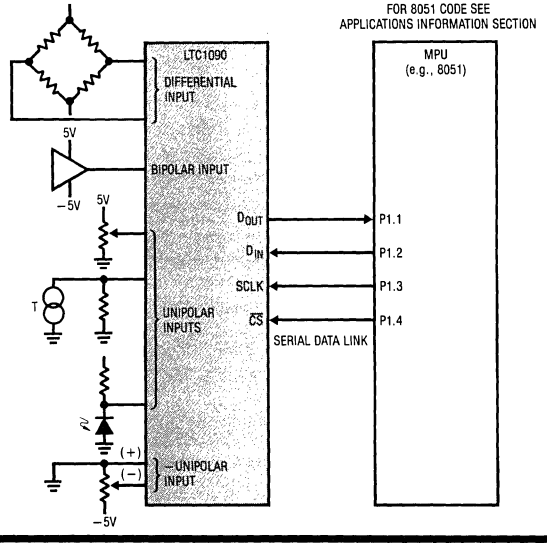
The serial I/O is designed to be compatible with industry standard full duplex serial interfaces. It allows either MSB or LSB first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8, 10, 12 or 16 bits. This allows easy interface to shift registers and a variety of processors.

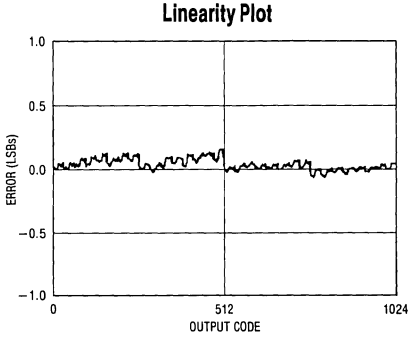
The LTC1090A is specified with total unadjusted error (including the effects of offset, linearity and gain errors) less than ±0.5LSB.

The LTC1090 is specified with offset and linearity less than ±0.5LSB but with a gain error limit of ±2LSB for applications where gain is adjustable or less critical.

LTCMOS is a trademark of Linear Technology Corp.

TYPICAL APPLICATION



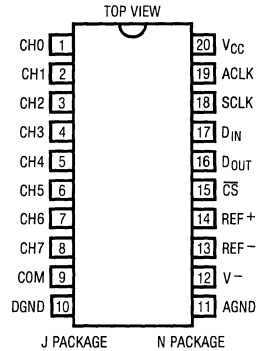


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
Negative Supply Voltage (V^-) ..... – 6V to GND
Voltage
  Analog and Reference
  Inputs ..... (V^-) – 0.3V to V_{CC} + 0.3V
  Digital Inputs ..... – 0.3V to 12V
  Digital Outputs ..... – 0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1090AC, LTC1090C ..... – 40°C to 85°C
  LTC1090AM, LTC1090M ..... – 55°C to 125°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1090AMJ
LTC1090MJ
LTC1090ACJ
LTC1090CJ
LTC1090ACN
LTC1090CN

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1090/LTC1090A MIN	MAX	UNITS
V_{CC}	Positive Supply Voltage	V^- = 0V	4.5	10	V
V^-	Negative Supply Voltage	V_{CC} = 5V	– 5.5	0	V
f_{SCLK}	Shift Clock Frequency	V_{CC} = 5V	0	1.0	MHz
f_{ACLK}	A/D Clock Frequency	V_{CC} = 5V	f_{SCLK}	2.0	MHz
t_{CYC}	Total Cycle Time	See Operating Sequence	10 SCLK + 48 ACLK		Cycles
$t_{h\overline{CS}}$	Hold Time, $\overline{CS}$ Low After Last SCLK↓	V_{CC} = 5V	0		ns
t_{hDI}	Hold Time, D_{IN} After SCLK↑	V_{CC} = 5V	150		ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before Clocking in First Address Bit (Note 9)	V_{CC} = 5V	2 ACLK Cycles + 1μs		
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK↑	V_{CC} = 5V	400		ns
t_{WHACLK}	ACLK High Time	V_{CC} = 5V	127		ns
t_{WLACLK}	ACLK Low Time	V_{CC} = 5V	200		ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	V_{CC} = 5V	44		ACLK Cycles

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1090A MIN	TYP	MAX	LTC1090 MIN	TYP	MAX	UNITS
Offset Error	(Note 4)	●			±0.5			±0.5	LSB
Linearity Error	(Notes 4 and 5)	●			±0.5			±0.5	LSB
Gain Error	(Note 4)	●			±0.5			±2.0	LSB
Total Unadjusted Error	V_{REF} = 5.000V (Notes 4 and 6)	●			±0.5				LSB

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1090A MIN	LTC1090A TYP	LTC1090A MAX	LTC1090 MIN	LTC1090 TYP	LTC1090 MAX	UNITS
Reference Input Resistance				10			10		kΩ
Analog and REF Input Range	(Note 7)			$(V^-) - 0.05V$ to $V_{CC} + 0.05V$					V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			1			1	μA
	On Channel = 0V Off Channel = 5V	●			−1			−1	μA
Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			−1			−1	μA
	On Channel = 0V Off Channel = 5V	●			1			1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1090/LTC1090A MIN	LTC1090/LTC1090A TYP	LTC1090/LTC1090A MAX	UNITS
t_{ACC}	Delay Time From $\overline{CS}$↓ to D_{OUT} Data Valid	(Note 9)			2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			5		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			44		ACLK Cycles
t_{dDO}	Delay Time, SCLK↓ to D_{OUT} Data Valid	See Test Circuits	●		250	450	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		140	300	ns
t_{en}	Delay Time, 2nd CLK↓ to D_{OUT} Enabled	See Test Circuits	●		150	400	ns
t_{hDO}	Time Output Data Remains Valid After SCLK↓				50		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		90	300	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		60	300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Off Channel Digital Inputs			65 5 5		pF pF pF

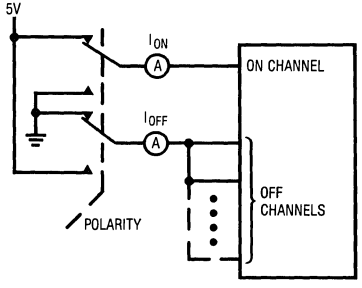
DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1090/LTC1090A MIN	LTC1090/LTC1090A TYP	LTC1090/LTC1090A MAX	UNITS
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25V$	●	2.0			V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	●			−2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V$, $I_O = 10\mu A$ $I_O = 360\mu A$	 ●	 2.4	4.7 4.0		V V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V$, $I_O = 1.6mA$	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High $V_{OUT} = 0V$, $\overline{CS}$ High	● ●			3 −3	μA μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			10		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High, REF^+ Open	●		1.0	2.5	mA
I_{REF}	Reference Current	$V_{REF} = 5V$	●		0.5	1.0	mA
I^-	Negative Supply Current	$\overline{CS}$ High, $V^- = -5V$	●		1	50	μA

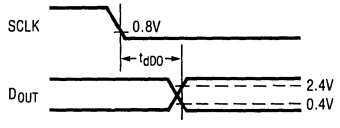
Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.
Note 2: All voltage values are with respect to ground with DGND, AGND and REF^- wired together (unless otherwise noted).
Note 3: $V_{CC} = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, $V^- = 0V$ for unipolar mode and $-5V$ for bipolar mode, ACLK = 2.0 MHz, SCLK = 0.5MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25°C$.
Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 1024. For example, when $V_{REF} = 5V$, 1LSB (bipolar) = 2(5V)/1024 = 9.77mV.
Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.
Note 6: Total unadjusted error includes offset, gain, linearity, multiplexer and hold step errors.
Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.
Note 8: Channel leakage current is measured after the channel selection.
Note 9: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edges after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select setup time has elapsed.

TEST CIRCUITS

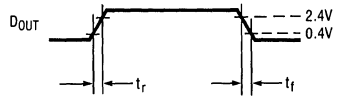
On and Off Channel Leakage Current



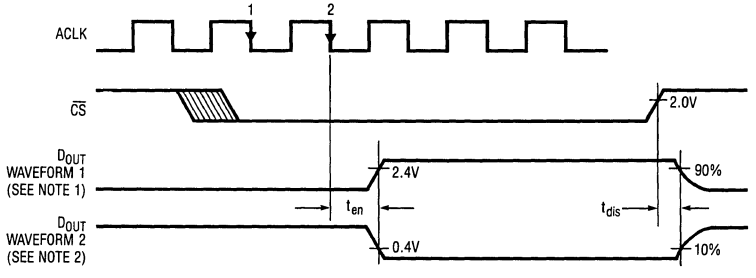
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for t_{en} and t_{dis}

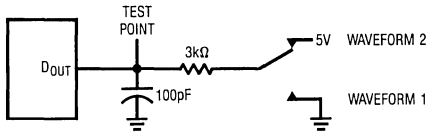


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

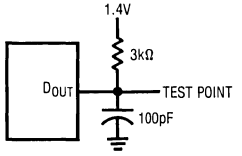
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS

Load Circuit for t_{dis} and t_{en}



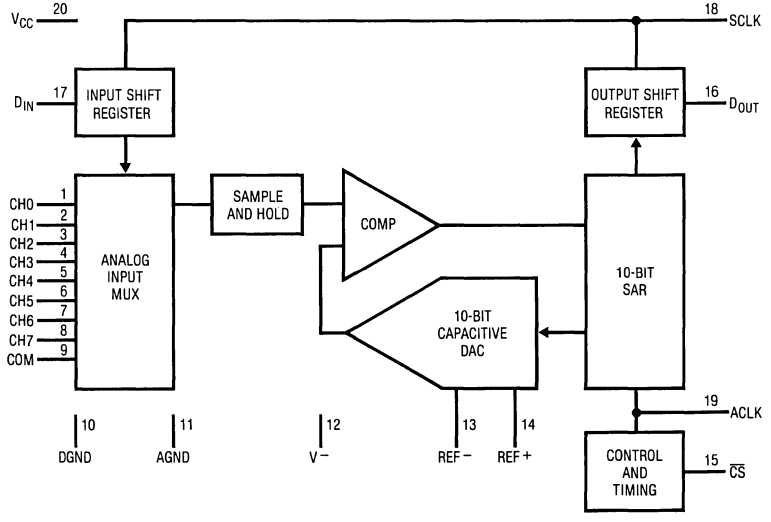
Load Circuit for t_{dDO}, t_r, and t_f



PIN FUNCTIONS

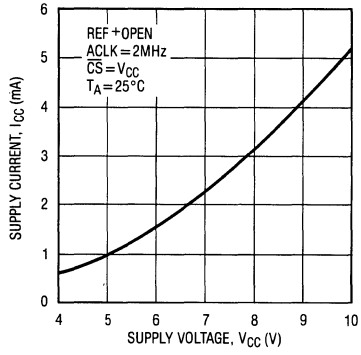
#	PIN	FUNCTION	DESCRIPTION
1-8	CH0-CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
12	V^-	Negative Supply	Tie V^- to most negative potential in the circuit. (Ground in single supply applications.)
13, 14	$\overline{REF}^-$, REF^+	Reference Inputs	The reference inputs must be kept free of noise with respect to AGND
15	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
18	SCLK	Shift Clock	This clock synchronizes the serial data transfer.
19	ACLK	A/D Conversion Clock	This clock controls the A/D conversion process.
20	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

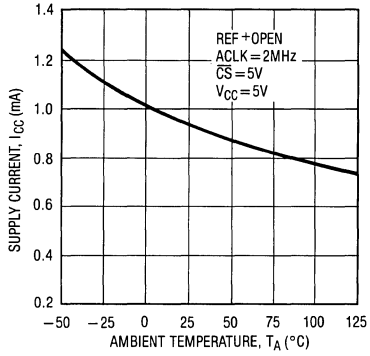


TYPICAL PERFORMANCE CHARACTERISTICS

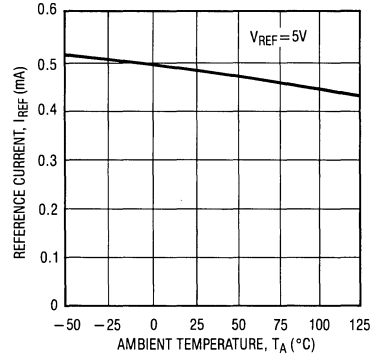
Supply Current vs Supply Voltage



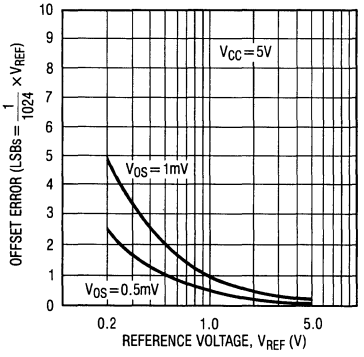
Supply Current vs Temperature



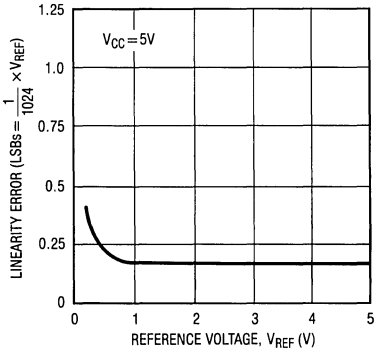
Reference Current vs Temperature



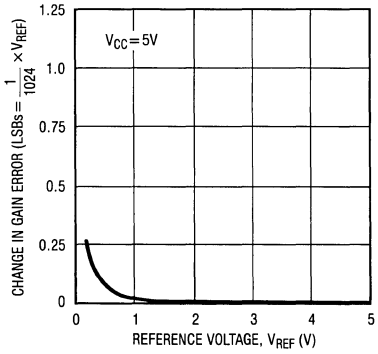
Unadjusted Offset Error vs Reference Voltage



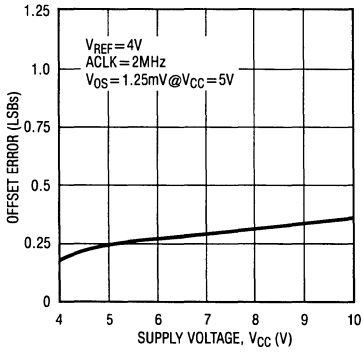
Linearity Error vs Reference Voltage



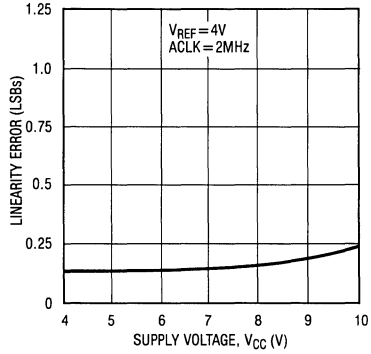
Change in Gain Error vs Reference Voltage



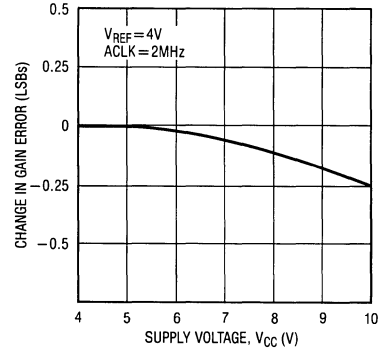
Offset Error vs Supply Voltage



Linearity Error vs Supply Voltage

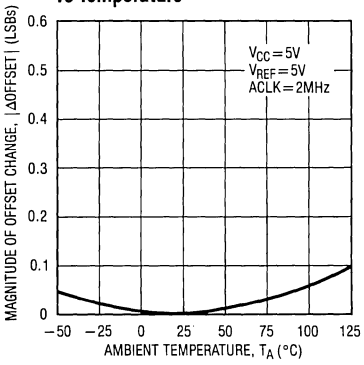


Change in Gain Error vs Supply Voltage

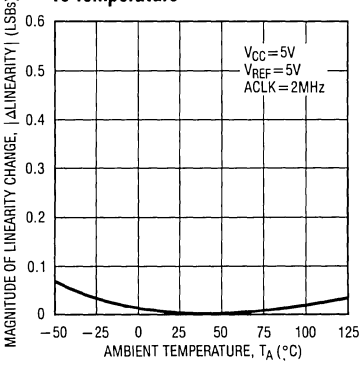


TYPICAL PERFORMANCE CHARACTERISTICS

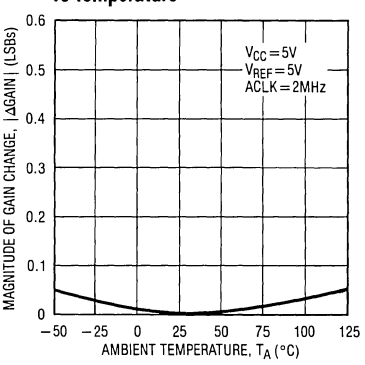
Change in Offset Error vs Temperature



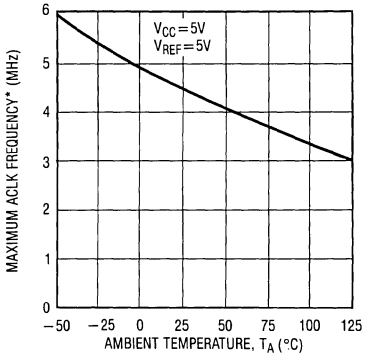
Change in Linearity Error vs Temperature



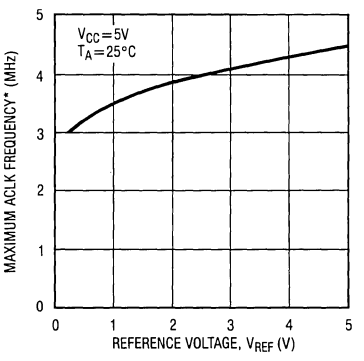
Change in Gain Error vs Temperature



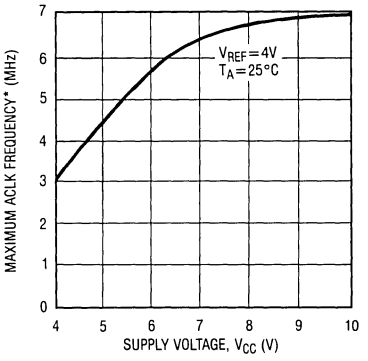
Maximum Conversion Clock Rate vs Temperature



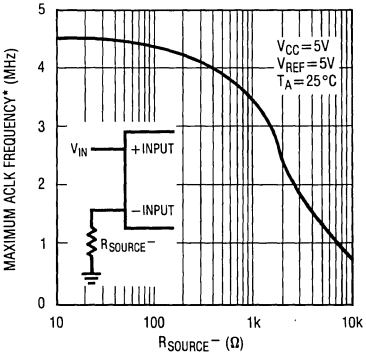
Maximum Conversion Clock Rate vs Reference Voltage



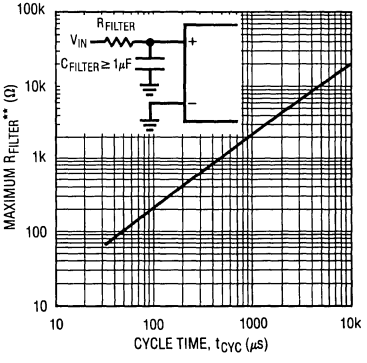
Maximum Conversion Clock Rate vs Supply Voltage



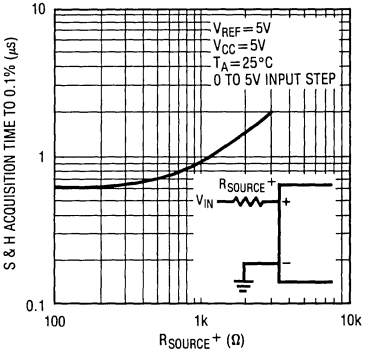
Maximum Conversion Clock Rate vs Source Resistance



Maximum Filter Resistor vs Cycle Time



Sample and Hold Acquisition Time vs Source Resistance

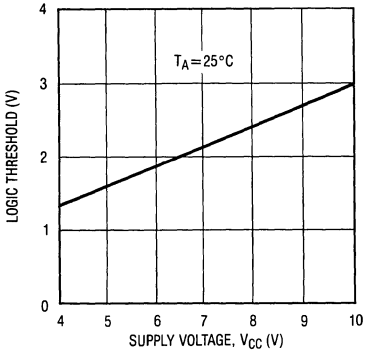


*MAXIMUM ACLK FREQUENCY REPRESENTS THE ACLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 2MHz VALUE IS FIRST DETECTED.

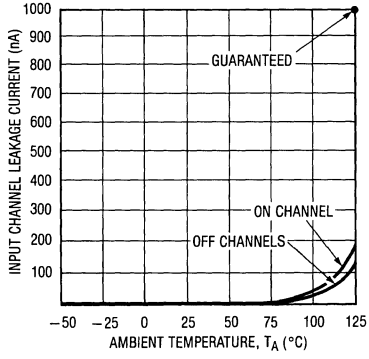
**MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0 IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

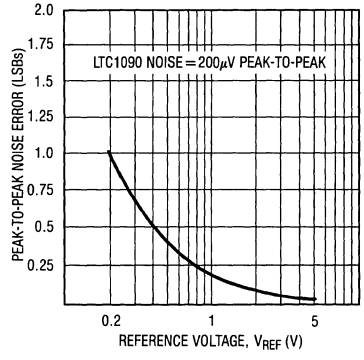
Digital Input Logic Threshold vs Supply Voltage



Input Channel Leakage Current vs Temperature



Noise Error vs Reference Voltage



APPLICATIONS INFORMATION

The LTC1090 is a data acquisition component which contains the following functional blocks:

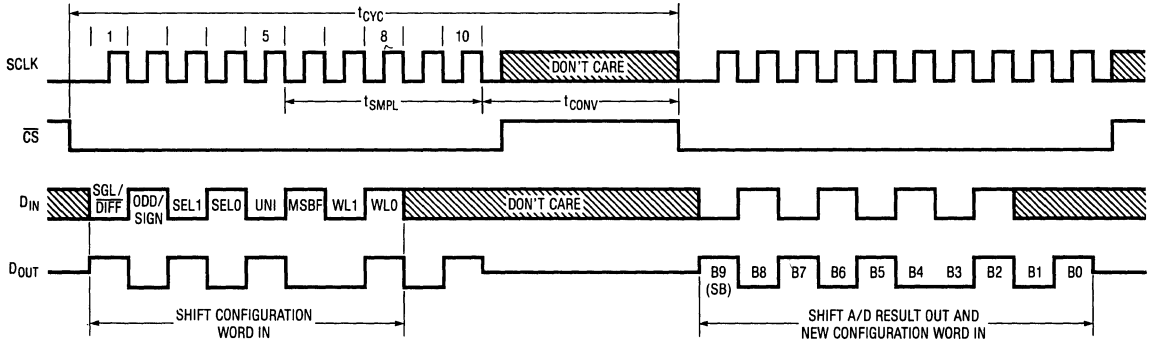
1. 10-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

1. Serial Interface

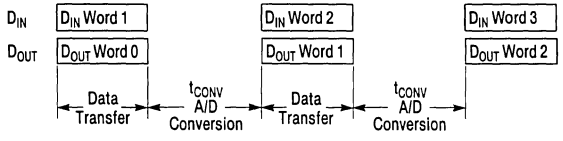
The LTC1090 communicates with microprocessors and other external circuitry via a synchronous, full duplex, four wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB First and 10-Bit Word Length)



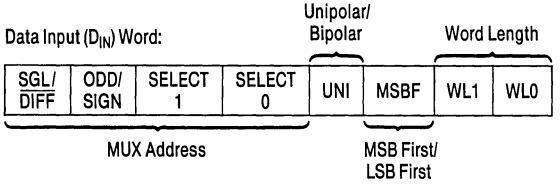
APPLICATIONS INFORMATION

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After the falling $\overline{CS}$ is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1090 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and $\overline{CS}$ should be brought high. After t_{CONV}, the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one $\overline{CS}$ cycle from the input word requesting it.



2. Input Data Word

The LTC1090 8-bit input data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The eight bits of the input word are defined as follows:



Multiplexer (MUX) Address

The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of Table 1. Note that in differential mode (SGL/$\overline{DIFF}$ = 0) measurements are limited to four adjacent input pairs with either polarity. In single ended mode, all input channels are measured with respect to COM. Figure 1 shows some examples of multiplexer assignments.

Table 1. Multiplexer Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION							
SGL/ DIFF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7
0	0	0	0	+	–						
0	0	0	1			+	–				
0	0	1	0					+	–		
0	0	1	1							+	–
0	1	0	0	–	+						
0	1	0	1			–	+				
0	1	1	0					–	+		
0	1	1	1							–	+

MUX ADDRESS				SINGLE ENDED CHANNEL SELECTION								
SGL/ DIFF	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								–
1	0	0	1			+						–
1	0	1	0					+				–
1	0	1	1							+		–
1	1	0	0		+							–
1	1	0	1				+					–
1	1	1	0						+			–
1	1	1	1								+	–

APPLICATIONS INFORMATION

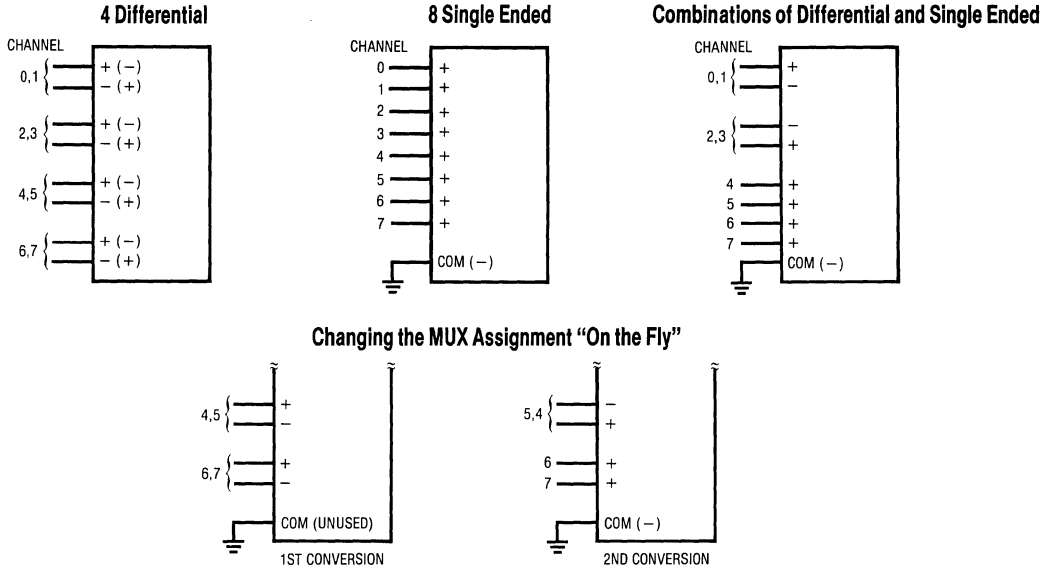
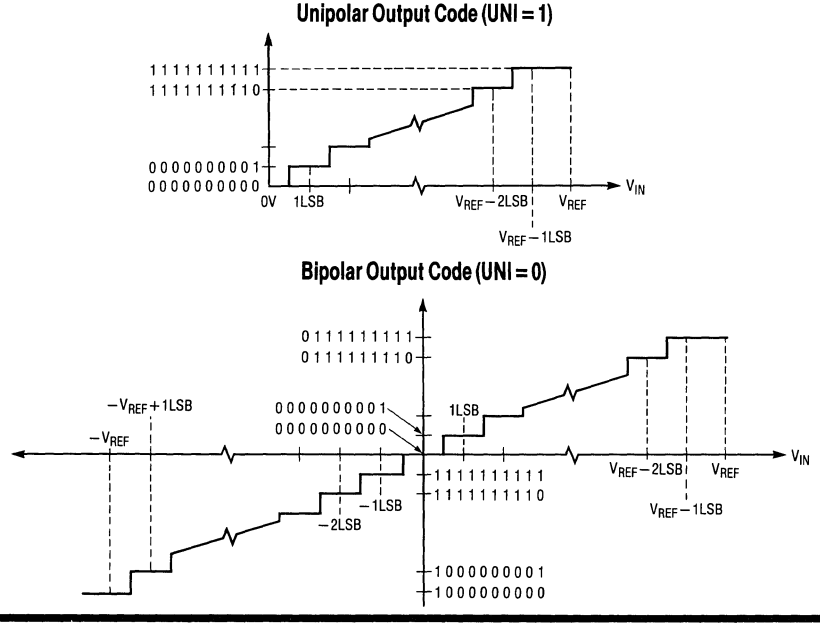


Figure 1. Examples of Multiplexer Options on the LTC1090

Unipolar/Bipolar (UNI)

The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.



APPLICATIONS INFORMATION

Unipolar Transfer Curve (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
1111111111	V_{REF} – 1LSB	4.9951V
1111111110	V_{REF} – 2LSB	4.9902V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0049V
0000000000	0V	0V

Bipolar Transfer Curve (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
0111111111	V_{REF} – 1LSB	4.9902V
0111111110	V_{REF} – 2LSB	4.9805V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0098V
0000000000	0V	0V
1111111111	– 1LSB	– 0.0098V
1111111110	– 2LSB	– 0.0195V
•	•	•
•	•	•
•	•	•
1000000001	– (V_{REF}) + 1LSB	– 4.9902V
1000000000	– (V_{REF})	– 5.000V

MSB First/LSB First Format (MSBF)

The output data of the LTC1090 is programmed for MSB first or LSB first sequence using the MSBF bit. For MSB first output data the input word clocked to the LTC1090 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB first output data, the input word clocked to the LTC1090 should always contain a zero in the MSBF bit location. The MSBF bit in a given D_{IN} word will control the order of the next D_{OUT} word. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB First
1	MSB First

Word Length (WL1, WL0)

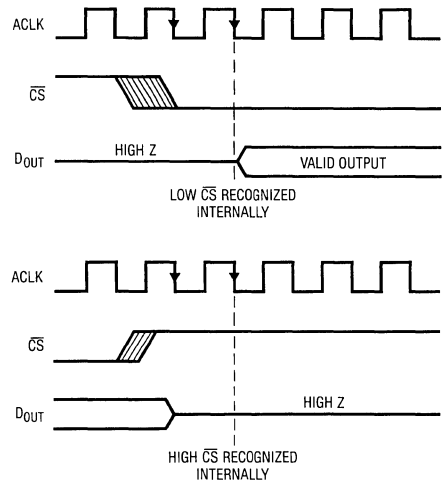
The last two bits of the input word (WL1 and WL0) program the output data word length of the LTC1090. Word lengths of 8, 10, 12 or 16 bits can be selected according to the following table. The WL1 and WL0 bits in a given D_{IN} word control the length of the present, not the next, D_{OUT} word. **WL1 and WL0 are never "don't cares"** and must be set for the correct D_{OUT} word length even when a "dummy" D_{IN} word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU.

WL1	WL0	OUTPUT WORD LENGTH
0	0	8 Bits
0	1	10 Bits
1	0	12 Bits
1	1	16 Bits

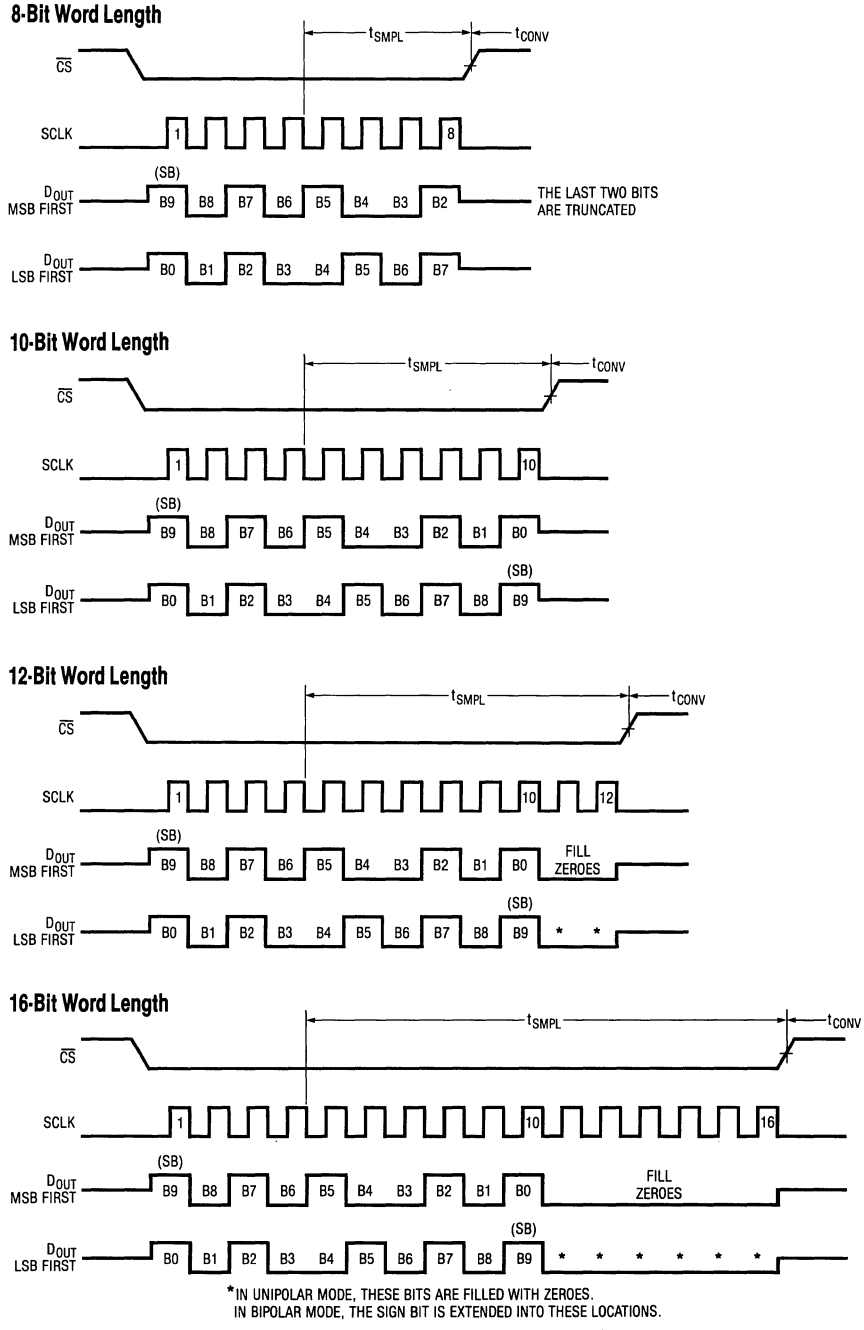
Figure 2 shows how the data output (D_{OUT}) timing can be controlled with word length selection and MSB/LSB first format selection.

3. Deglitcher

A deglitching circuit has been added to the Chip Select input of the LTC1090 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the $\overline{CS}$ input that are shorter in duration than 1 ACLK cycle. After a change of state on the $\overline{CS}$ input, the LTC1090 waits for two falling edges of the ACLK before recognizing a valid chip select. One indication of $\overline{CS}$ low recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling $\overline{CS}$ edges.



APPLICATIONS INFORMATION



*IN UNIPOLAR MODE, THESE BITS ARE FILLED WITH ZEROES.
IN BIPOLAR MODE, THE SIGN BIT IS EXTENDED INTO THESE LOCATIONS.

Figure 2. Data Output (D_{OUT}) Timing with Different Word Lengths

APPLICATIONS INFORMATION

4. $\overline{CS}$ Low During Conversion

In the normal mode of operation, $\overline{CS}$ is brought high during the conversion time (see Figure 3). The serial port ignores any SCLK activity while $\overline{CS}$ is high. The LTC1090 will also operate with $\overline{CS}$ low during the conversion. In this mode, SCLK must remain low during the conversion as shown in Figure 4. After the conversion is complete, the D_{OUT} line will become active with the first output bit. Then the data transfer can begin as normal.

5. Microprocessor Interfaces

The LTC1090 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous

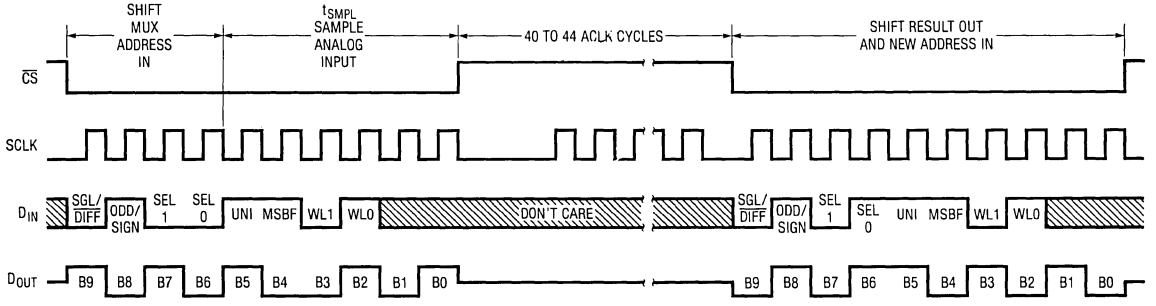


Figure 3. $\overline{CS}$ High During Conversion

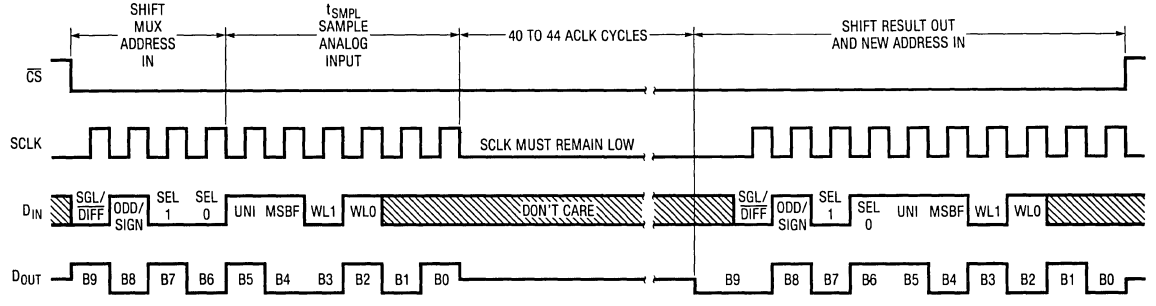


Figure 4. $\overline{CS}$ Low During Conversion

APPLICATIONS INFORMATION

serial formats (see Table 2). If an MPU without a serial interface is used, then 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1090. Included here are three serial interface examples and one example showing a parallel port programmed to form the serial interface.

Table 2. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1090**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port

*Requires external hardware

**Contact factory for interface information for processors not on this list

†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

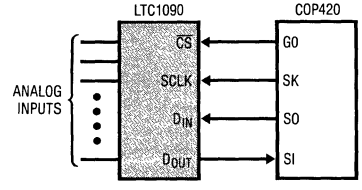
Serial Port Microprocessors

Most synchronous serial formats contain a shift clock (SCLK) and two data lines, one for transmitting and one for receiving. In most cases data bits are transmitted on the falling edge of the clock (SCLK) and captured on the rising edge. However, serial port formats vary among MPU manufacturers as to the smallest number of bits that can be sent in one group (e.g., 4-bit, 8-bit or 16-bit transfers). They also vary as to the order in which the bits are transmitted (LSB or MSB first). The following examples show how the LTC1090 accommodates these differences.

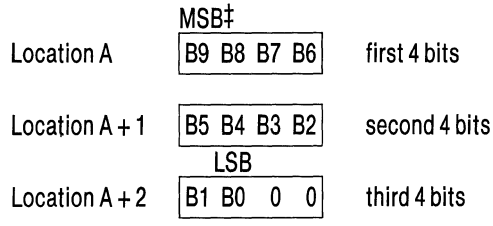
National MICROWIRE (COP420)

The COP420 transfers data MSB first and in 4-bit increments (nibbles). This is easily accommodated by setting the LTC1090 to MSB first format and 12-bit word length. The data output word is then received by the COP420 in three 4-bit blocks with the final two unused bits filled with zeroes by the LTC1090.

Hardware and Software Interface to National Semiconductor COP420 Processor



D_{OUT} from LTC1090 stored in COP420 RAM



‡B9 is MSB in unipolar or sign bit in bipolar

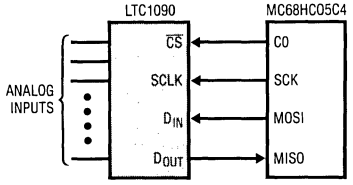
MNEMONIC	DESCRIPTION
LEI	Enable SIO
SC	Set Carry flag
OGI	G0 is set to 0 ($\overline{CS}$ goes low)
LDD	Load first 4 bits of D_{IN} to ACC
XAS	Swap ACC with SIO reg. Starts SK Clk
LDD	Load 2nd 4 bits of D_{IN} to ACC
NOP	Timing
XAS	Swap first 4 bits from A/D with ACC. SK continues.
XIS	Put first 4 bits in RAM (location A)
NOP	Timing
XAS	Swap 2nd 4 bits from A/D with ACC. SK continues.
XIS	Put 2nd 4 bits in RAM (location A + 1)
RC	Clear Carry
NOP	Timing
XAS	Swap 3rd 4 bits from A/D with ACC. SK off
XIS	Put 3rd 4 bits in RAM (location A + 2)
OGI	G0 is set to 1 ($\overline{CS}$ goes high)
LEI	Disable SIO

APPLICATIONS INFORMATION

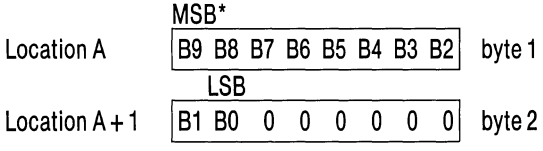
Motorola SPI (MC68HC05C4)

The MC68HC05C4 transfers data MSB first and in 8-bit increments. Programming the LTC1090 for MSB first format and 16-bit word length allows the 10-bit data output to be received by the MPU as two 8-bit bytes with the final 6 unused bits filled with zeroes by the LTC1090.

Hardware and Software Interface to Motorola MC68HC05C4 Processor



D_{OUT} from LTC1090 stored in MC68HC05C4 RAM



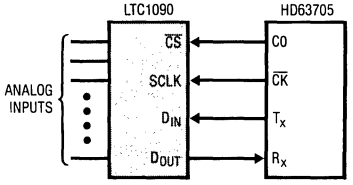
*B9 is MSB in unipolar or sign bit in bipolar

MNEMONIC	DESCRIPTION
BCLR n	C0 is cleared ($\overline{CS}$ goes low)
LDA	Load D_{IN} for LTC1090 into ACC
STA	Load D_{IN} from ACC to SPI data reg. Start SCK
↑	
NOP	8 NOPs for timing
↓	
LDA	Load contents of SPI status reg. into ACC
LDA	Load LTC1090 D_{OUT} from SPI data reg. into ACC (byte 1)
STA	Load LTC1090 D_{OUT} into RAM (location A)
STA	Start next SPI cycle
↑	
NOP	6 NOPs for timing
↓	
BSET n	C0 is set ($\overline{CS}$ goes high)
LDA	Load contents of SPI status reg. into ACC
LDA	Load LTC1090 D_{OUT} from SPI data reg. into ACC (byte 2)
STA	Load LTC1090 D_{OUT} into RAM (location A + 1)

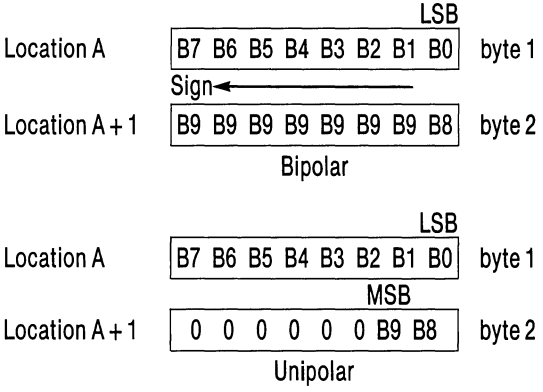
Hitachi Synchronous SCI (HD63705)

The HD63705 transfers serial data in 8-bit increments, LSB first. To accommodate this, the LTC1090 is programmed for 16-bit word length and LSB first format. The 10-bit output data is received by the processor as two 8-bit bytes, LSB first. The LTC1090 fills the final 6 unused bits (after the MSB) with zeroes in unipolar mode and with the sign bit in bipolar mode.

Hardware and Software Interface to Hitachi HD63705 Processor



D_{OUT} from LTC1090 stored in HD63705 RAM



MNEMONIC	DESCRIPTION
LDA	Load D_{IN} word for LTC1090 into ACC from RAM
BCLR n	C0 cleared ($\overline{CS}$ goes low)
STA	Load D_{IN} word for LTC1090 into SCI data reg from ACC and start clocking data (LSB first)
↑	
NOP	6 NOPs for timing
↓	
LDA	Load contents of SCI data reg into ACC (byte 1) Start next SCI cycle
STA	Load LTC1090 D_{OUT} word into RAM (Location A)
NOP	Timing
BSET n	C0 set ($\overline{CS}$ goes high).
LDA	Load contents of SCI data reg into ACC (byte 2)
STA	Load LTC1090 D_{OUT} word into RAM (Location A + 1)

APPLICATIONS INFORMATION

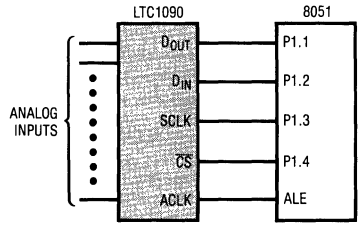
Parallel Port Microprocessors

When interfacing the LTC1090 to an MPU which has a parallel port, the serial signals are created on the port with software. Three MPU port lines are programmed to create the $\overline{CS}$, SCLK and D_{IN} signals for the LTC1090. A fourth port line reads the D_{OUT} line. An example is made of the Intel 8051/8052/80C252 family.

Intel 8051

To interface to the 8051, the LTC1090 is programmed for MSB first format and 10-bit word length. The 8051 generates $\overline{CS}$, SCLK and D_{IN} on three port lines and reads D_{OUT} on the fourth.

Hardware and Software Interface to Intel 8051 Processor



D_{OUT} from LTC1090 stored in 8051 RAM

	MSB*							LSB
R2	B9	B8	B7	B6	B5	B4	B3	B2
R3	B1	B0	0	0	0	0	0	0

*B9 is MSB in unipolar or sign bit in bipolar

8051 Code

MNEMONIC		DESCRIPTION
	MOV P1,#02H	Initialize port 1 (bit 1 is made an input)
	CLR P1.3	SCLK goes low
	SETB P1.4	$\overline{CS}$ goes high
CONTINUE:	MOV A,#0DH	D_{IN} word for the LTC1090 is placed in ACC.
	CLR P1.4	$\overline{CS}$ goes low
	MOV R4,#08	Load counter
	NOP	Delay for deglitcher
LOOP:	MOV C, P1.1	Read data bit into carry
	RLC A	Rotate data bit into ACC
	MOV P1.2, C	Output D_{IN} bit to LTC1090
	SETB P1.3	SCLK goes high
	CLR P1.3	SCLK goes low
	DJNZ R4, LOOP	Next bit
	MOV R2, A	Store MSBs in R2
	MOV C, P1.1	Read data bit into carry
	CLR A	Clear ACC
	RLC A	Rotate data bit into ACC
	SETB P1.3	SCLK goes high
	CLR P1.3	SCLK goes low
	MOV C, P1.1	Read data bit into carry
	RRC A	Rotate right into ACC
	RRC A	Rotate right into ACC
	MOV R3, A	Store LSBs in R3
	SETB P1.3	SCLK goes high
	CLR P1.3	SCLK goes low
	SETB P1.4	$\overline{CS}$ goes high
	MOV R5,#07H	Load counter
DELAY:	DJNZ R5, DELAY	Delay for LTC1090 to perform conversion
	AJMP CONTINUE	Repeat program

6. Sharing the Serial Interface

The LTC1090 can share the same 3 wire serial interface with other peripheral components or other LTC1090s (see Figure 5). In this case, the $\overline{CS}$ signals decide which LTC1090 is being addressed by the MPU.

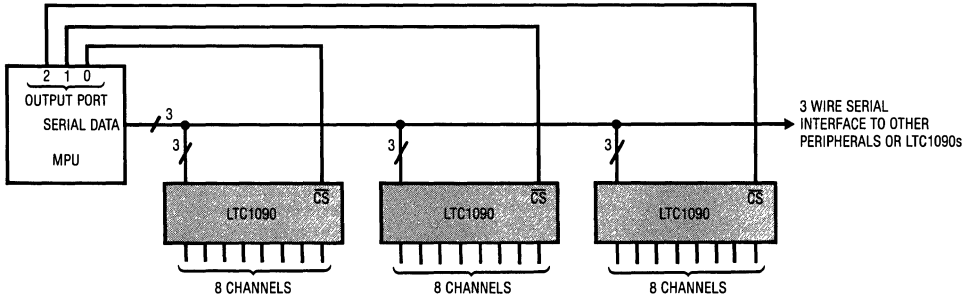


Figure 5. Several LTC1090s Sharing One 3 Wire Serial Interface

APPLICATIONS INFORMATION

ANALOG CONSIDERATIONS

1. Grounding

The LTC1090 should be used with an analog ground plane and single point grounding techniques.

Pin 11 (AGND) should be tied directly to this ground plane.

Pin 10 (DGND) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

Pin 20 (V_{CC}) should be bypassed to the ground plane with a 4.7μF tantalum with leads as short as possible. Pin 12 (V^-) should be bypassed with a 0.1μF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that pin 13 (REF^-) and pin 9 (COM) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 6 shows an example of an ideal ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

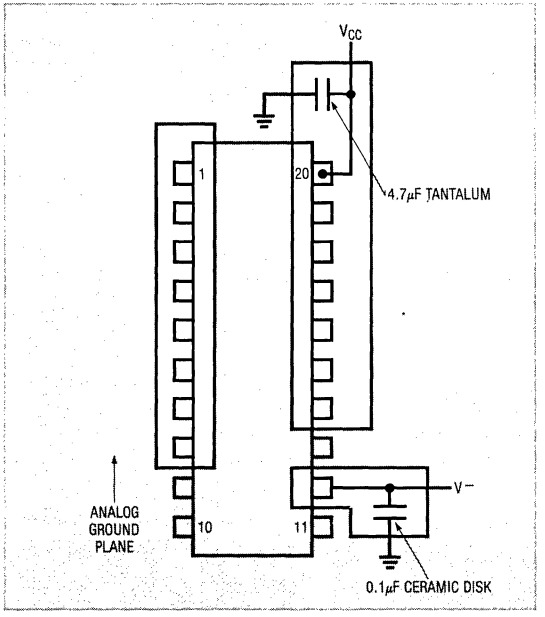


Figure 6. Example Ground Plane for the LTC1090

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a 4.7μF tantalum with leads as short as possible. Figures 7 and 8 show the effects of good and poor V_{CC} bypassing.

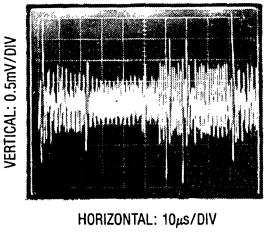


Figure 7. Poor V_{CC} Bypassing. Noise and Ripple can Cause A/D Errors

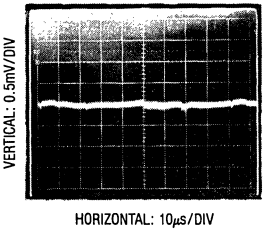


Figure 8. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1090 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem.

APPLICATIONS INFORMATION

However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1090 look like a 60pF capacitor (C_{IN}) is series with a 500Ω resistor (R_{ON}) as shown in Figure 9. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

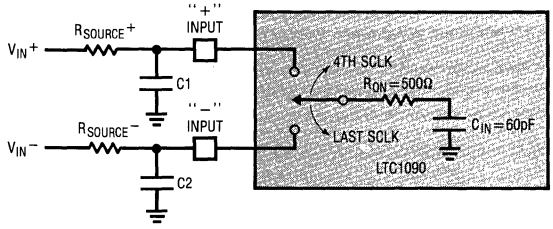


Figure 9. Analog Input Equivalent Circuit

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 10th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of 4μs, **R_{SOURCE}^+ < 2k and C1 < 20pF will provide adequate settling.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 10). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the "–" input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 2MHz, **R_{SOURCE}^- < 1kΩ and C2 < 20pF will provide adequate settling.**

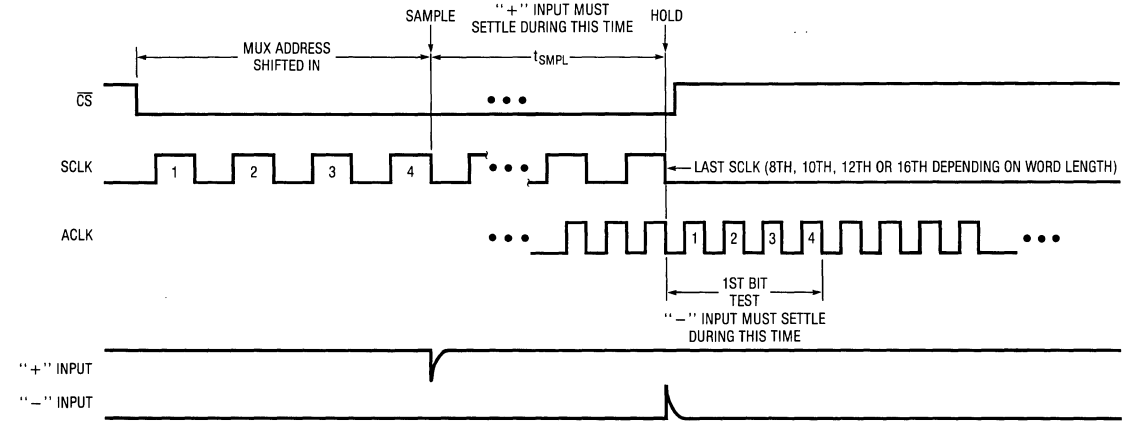


Figure 10. "+" and "–" Input Settling Windows

APPLICATIONS INFORMATION

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 4μs ("+" input) and 2μs ("–" input) which occur at the maximum clock rates (ACLK = 2MHz and SCLK = 1MHz). Figures 11 and 12 show examples of adequate and poor op amp settling.

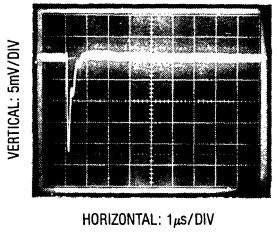


Figure 11. Adequate Settling of Op Amp Driving Analog Input

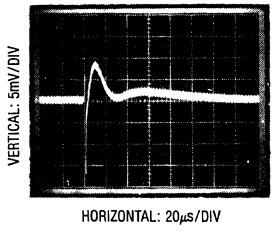


Figure 12. Poor Op Amp Settling can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of C_F (e.g., 1μF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 60pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 33μs, the input current equals 9μA at $V_{IN} = 5V$. In this case, a filter resistor of 50Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

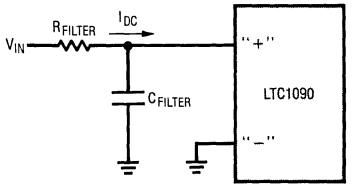


Figure 13. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

Noise Coupling into Inputs

High source resistance input signals (>500Ω) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2-CH7) for signals which have the highest output resistance because they are essentially shielded by the pins on the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

4. Sample and Hold

Single Ended Inputs

The LTC1090 provides a built-in sample and hold (S&H) function for all signals acquired in the single ended mode (COM pin grounded). This sample and hold allows the LTC1090 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the

APPLICATIONS INFORMATION

final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 10th, 12th or 16th falling edge of the SCLK depending on the word length selected.

Differential Inputs

With differential inputs or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 44 ACLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR(MAX)} = V_{PEAK} \times 2 \times \pi \times f("-") \times 44/f_{ACLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{ACLK} is the frequency of the ACLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (1.25mV) with the converter running at ACLK = 2MHz, its peak value would have to be 150mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1090 defines the voltage span of the A/D converter. The reference inputs look primarily like a 10kΩ resistor but will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

When driving the reference inputs, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference inputs should be low (less than 1Ω) to prevent DC drops caused by the 1mA maximum reference current (I_{REF}).
2. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 2MHz most references and op amps can be made to settle within the 2μs bit time.
3. It is recommended that the REF^- input be tied directly to the analog ground plane. If REF^- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

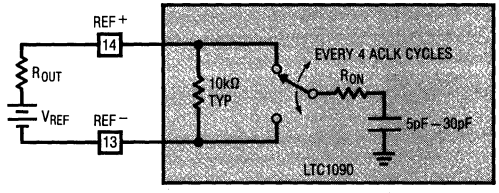


Figure 14. Reference Input Equivalent Circuit

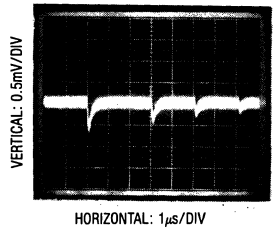


Figure 15. Adequate Reference Settling

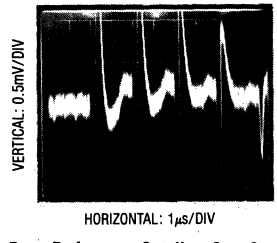


Figure 16. Poor Reference Settling Can Cause A/D Errors

APPLICATIONS INFORMATION

6. Reduced Reference Operation

The effective resolution of the LTC1090 can be increased by reducing the input span of the converter. The LTC1090 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Conversion speed (ACLK frequency)
2. Offset
3. Noise

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1090 internal comparator overdrive is reduced. With less overdrive, more time is required to perform a conversion. Therefore, the maximum ACLK frequency should be reduced when low values of V_{REF} are used. This is shown in the typical curve of Maximum Conversion Clock Rate vs Reference Voltage.

Offset with Reduced V_{REF}

The offset of the LTC1090 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 0.5mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1090.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1090 can be reduced to approximately 200μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200μV of noise.

For operation with a 5V reference, the 200μV noise is only 0.04LSB peak-to-peak. In this case, the LTC1090 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200μV noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.2LSB. If the reference is further reduced to 200mV, the 200μV noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

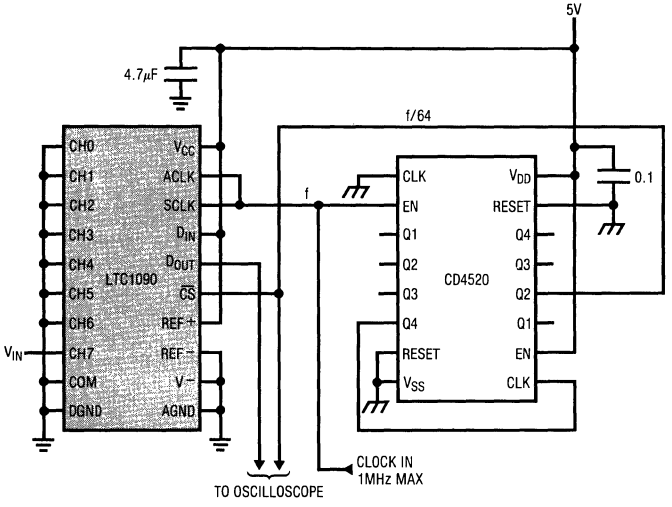
TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1090

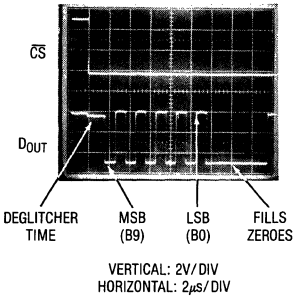
Users can get a quick look at the function and timing of the LTC1090 by using the following simple circuit. REF^+ and D_{IN} are tied to V_{CC} selecting a 5V input span, CH7 as a single ended input, unipolar mode, MSB first format and 16-bit word length. ACLK and SCLK are tied together and driven by an external clock. $\overline{CS}$ is driven at 1/64 the clock rate by the CD4520 and D_{OUT} outputs the data. All other pins are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of $\overline{CS}$.

TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1090



Scope Trace of LTC1090 "Quick Look" Circuit Showing A/D Output of 0101010101 (155_{HEX})

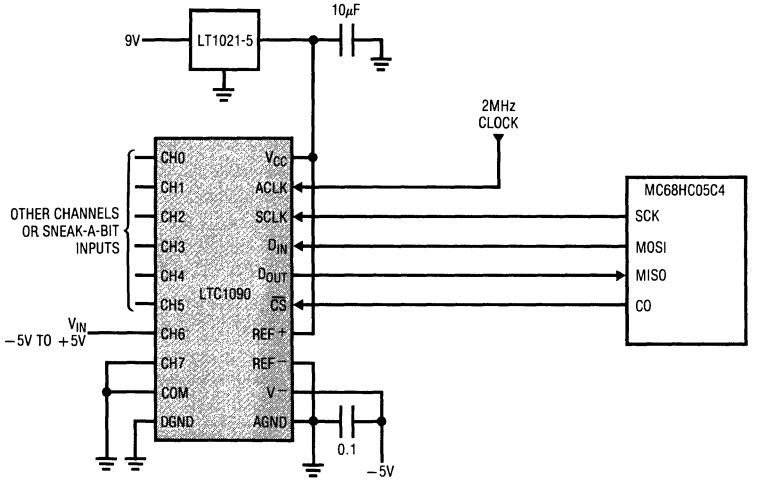


SNEAK-A-BIT™

The LTC1090's unique ability to software select the polarity of the differential inputs and the output word length is used to achieve one more bit of resolution. Using the circuit below with two conversions and some software, a 2's complement 10-bit + sign word is returned to memory inside the MPU. The MC68HC05C4 was chosen as an example; however, any processor could be used.

Two 10-bit unipolar conversions are performed: the first over a 0 to 5V span and the second over a 0 to –5V span (by reversing the polarity of the inputs). The sign of the input is determined by which of the two spans contained it. Then the resulting number (ranging from –1023 to +1023 decimal) is converted to 2's complement notation and stored in RAM.

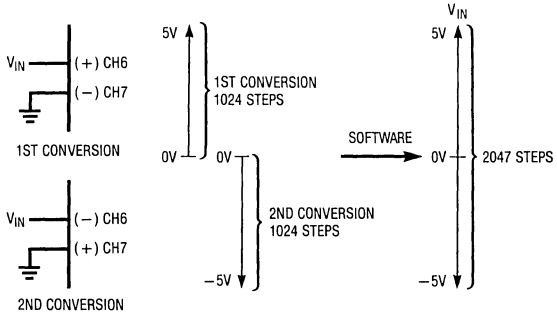
SNEAK-A-BIT Circuit



SNEAK-A-BIT is a trademark of Linear Technology Corp.

TYPICAL APPLICATIONS

SNEAK-A-BIT



SNEAK-A-BIT Code

D_{OUT} from LTC1090 in MC68HC05C4 RAM

	Sign							
Location $77	B10	B9	B8	B7	B6	B5	B4	B3
	LSB							
Location $87	B2	B1	B0	filled with 0s				

D_{IN} words for LTC1090

	MUX Addr. (ODD/SIGN)				UNI	MSBF	Word Length	
D_{IN} 1	0	0	1	1	1	1	1	1
D_{IN} 2	0	1	1	1	1	1	1	1
D_{IN} 3	0	0	1	1	1	1	1	1

Sneak-A-Bit Code for the LTC1090 Using the MC68HC05C4

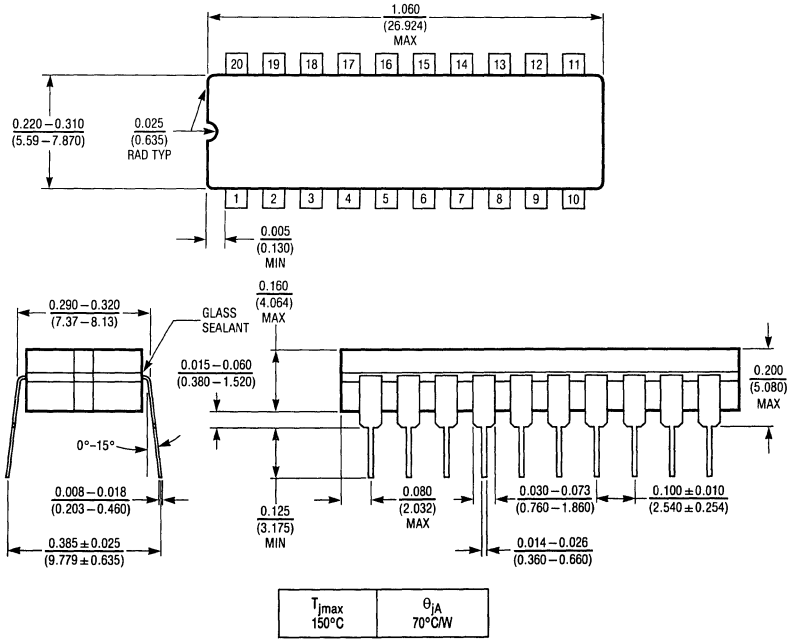
MNEMONIC		DESCRIPTION
LDA	#$50	Configuration data for SPCR
STA	$0A	Load configuration data into $0A
LDA	#$FF	Configuration data for port C DDR
STA	$06	Load configuration data into port C DDR
BSET	0, $02	Make sure $\overline{CS}$ is high
JSR	READ – / +	Dummy read configures LTC1090 for next read
JSR	READ + / –	Read CH6 with respect to CH7
JSR	READ – / +	Read CH7 with respect to CH6
JSR	CHK SIGN	Determines which reading has valid data, converts to 2's complement and stores in RAM

Sneak-A-Bit Code for the LTC1090 Using the MC68HC05C4

MNEMONIC			DESCRIPTION
READ – / + :	LDA	#$3F	Load D_{IN} word for LTC1090 into ACC
	JSR	TRANSFER	Read LTC1090 routine
	LDA	$60	Load MSBs from LTC1090 into ACC
	STA	$71	Store MSBs in $71
	LDA	$61	Load LSBs from LTC1090 into ACC
	STA	$72	Store LSBs in $72
	RTS		Return
READ + / – :	LDA	#$7F	Load D_{IN} word for LTC1090 into ACC
	JSR	TRANSFER	Read LTC1090 routine
	LDA	$60	Load MSBs from LTC1090 into ACC
	STA	$73	Store MSBs in $73
	LDA	$61	Load LSBs from LTC1090 into ACC
	STA	$74	Store LSBs in $74
	RTS		Return
TRANSFER:	BCLR	0, $02	$\overline{CS}$ goes low
	STA	$0C	Load D_{IN} into SPI. Start transfer
LOOP 1:	TST	$0B	Test status of SPIF
	BPL	LOOP 1	Loop to previous instruction if not done
	LDA	$0C	Load contents of SPI data reg into ACC
	STA	$0C	Start next cycle
	STA	$60	Store MSBs in $60
LOOP 2:	TST	$0B	Test status of SPIF
	BPL	LOOP 2	Loop to previous instruction if not done
	BSET	0, $02	$\overline{CS}$ goes high
	LDA	$0C	Load contents of SPI data reg into ACC
	STA	$61	Store LSBs in $61
	RTS		Return
CHK SIGN:	LDA	$73	Load MSBs of + / – read into ACC
	ORA	$74	Or ACC (MSBs) with LSBs of + / – read
	BEQ	MINUS	If result is 0 goto minus
	CLC		Clear carry
	ROR	$73	Rotate right $73 through carry
	ROR	$74	Rotate right $74 through carry
	LDA	$73	Load MSBs of + / – read into ACC
	STA	$77	Store MSBs in RAM location $77
	LDA	$74	Load LSBs of + / – read into ACC
	STA	$87	Store LSBs in RAM location $87
	BRA	END	Goto end of routine
MINUS:	CLC		Clear carry
	ROR	$71	Shift MSBs of – / + read right
	ROR	$72	Shift LSBs of – / + read right
	COM	$71	1's complement of MSBs
	COM	$72	1's complement of LSBs
	LDA	$72	Load LSBs into ACC
	ADD	#$01	Add 1 to LSBs
	STA	$72	Store ACC in $72
	CLRA		Clear ACC
	ADC	$71	Add with carry to MSBs. Result in ACC
	STA	$71	Store ACC in $71
	STA	$77	Store MSBs in RAM location $77
	LDA	$72	Loac LSBs in ACC
	STA	$87	Store LSBs in RAM location $87
END:	RTS		Return

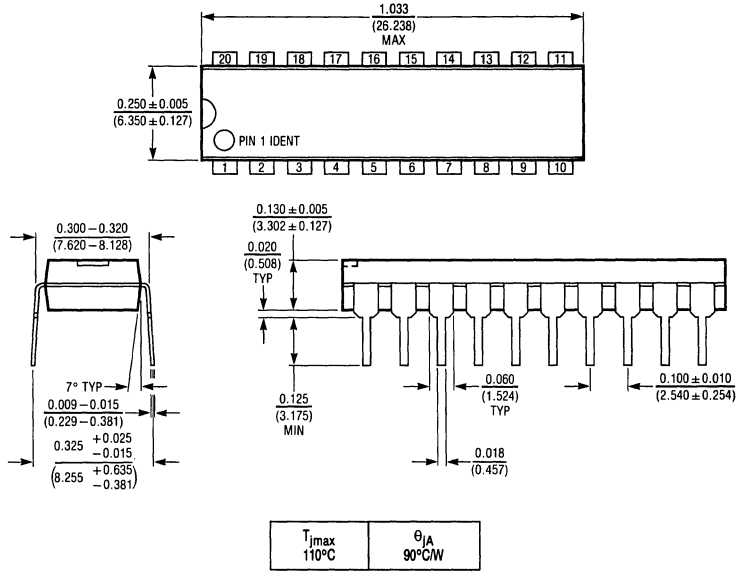
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J20 Package Ceramic DIP



T_{jmax}	θ_{JA}
150°C	70°C/W

N20 Package Molded DIP



T_{jmax}	θ_{JA}
110°C	90°C/W

2 Channel, 10-Bit Serial A-to-D Converter

FEATURES

- 10-Bit Resolution
- Software Controlled 2-Channel Multiplexer
- Differential and Single Ended Input Capability
- Built-In Sample and Hold
- Analog Inputs Common-Mode to V_{CC} and GND
- Single Supply Operation
- Direct 3 or 4 Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 8 Pin DIP Package

KEY SPECIFICATIONS

■ Resolution	10 Bits
■ Total Unadjusted Error (LTC1091A)	±1/2LSB
■ Fast Conversion Time	20μs
■ Low Supply Current	3.5mA Max, 1.5mA Typ

LTCMOS is a trademark of Linear Technology Corp.

DESCRIPTION

The LTC1091 is a serial data acquisition component which contains a successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform 10-bit A/D conversions. A 2-channel input multiplexer can be configured for either single ended or differential inputs. An on-chip sample and hold is included for single ended input channels.

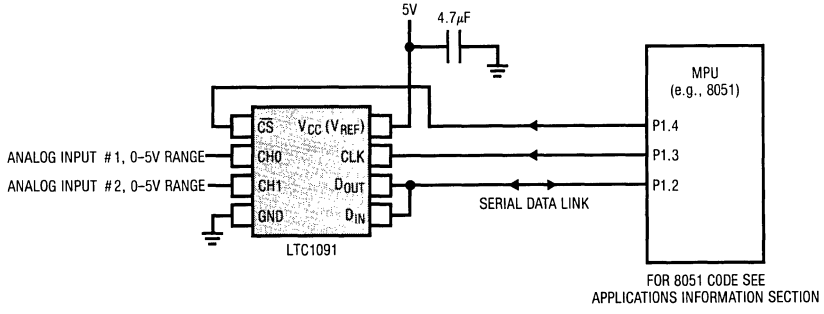
The reference input for the A/D converter is internally connected to the power supply pin making ratiometric operation easy. If absolute reference operation is desired, the LTC1091's low supply current allows it to be powered directly from most popular references (e.g., LT1021).

The serial I/O is designed to be compatible with industry standard half duplex serial interfaces. It allows either MSB or LSB first data. It can provide output data word lengths of 10 to 16 bits. This allows easy interface to shift registers and a variety of processors.

The LTC1091A is specified with total unadjusted error (including the effects of offset, linearity and gain errors) less than ±0.5LSB.

The LTC1091 is specified with offset and linearity less than ±0.5LSB but with a gain error limit of ±2LSB for applications where gain is adjustable or less critical.

TYPICAL APPLICATION

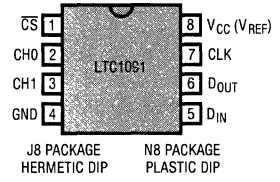


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) 12V
Voltage
  Analog and Digital Inputs ..... – 0.3V to V_{CC} + 0.3V
  Digital Outputs ..... – 0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1091AC, LTC1091C ..... – 40°C to 85°C
  LTC1091AM, LTC1091M ..... – 55°C to 125°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
HERMETIC DIP

N8 PACKAGE
PLASTIC DIP

ORDER PART NUMBER
LTC1091AMJ8
LTC1091MJ8
LTC1091ACJ8
LTC1091CJ8
LTC1091ACN8
LTC1091CN8

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1091/LTC1091A MIN	MAX	UNITS
V_{CC} (V_{REF})	Supply and Reference Voltage		4.5	10	V
f_{CLK}	Clock Frequency	V_{CC} = 5V	0.01	0.5	MHz
t_{CYC}	Total Cycle Time	See Operating Sequence	15 CLK Cycles + 2μs		
t_{hDI}	Hold Time, D_{IN} After SCLK↑	V_{CC} = 5V	150		ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before Clocking in First Address Bit	V_{CC} = 5V	1		μs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V	400		ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V	0.8		μs
t_{WLCLK}	CLK Low Time	V_{CC} = 5V	1		μs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V	2		μs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer		15		CLK Cycles

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1091A MIN	TYP	MAX	LTC1091 MIN	TYP	MAX	UNITS
Offset Error		●			±0.5			±0.5	LSB
Linearity Error	(Note 4)	●			±0.5			±0.5	LSB
Gain Error		●			±0.5			±2.0	LSB
Total Unadjusted Error	V_{CC} = 5.000V (Note 5)	●			±0.5				LSB
Analog Input Range	(Note 6)				– 0.05V to V_{CC} + 0.05V				V
On Channel Leakage Current (Note 7)	On Channel = 5V Off Channel = 0V	●			1			1	μA
	On Channel = 0V Off Channel = 5V	●			– 1			– 1	μA
Off Channel Leakage Current (Note 7)	On Channel = 5V Off Channel = 0V	●			– 1			– 1	μA
	On Channel = 0V Off Channel = 5V	●			1			1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1091/LTC1091A MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			10		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		400	850	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		180	450	ns
t_{en}	Delay Time, 4th CLK↓ to D_{OUT} Enabled	See Test Circuits	●		160	450	ns
t_{hDO}	Time Output Data Remains Valid After SCLK↓				150		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		90	300	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		60	300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Off Channel Digital Inputs			65 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1091/LTC1091A MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	μA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	μA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10μA I_O = 360μA	 ●	 2.4	4.7 4.0		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 –3	μA μA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			10		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High	●		1.5	3.5	mA

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 5V, CLK = 0.5MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 4: Linearity error is specified between the actual end points of the A/D transfer curve.

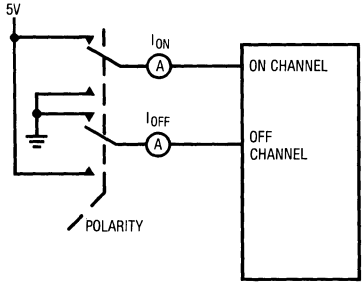
Note 5: Total unadjusted error includes offset, gain, linearity, multiplexer and hold step errors.

Note 6: Two on-chip diodes are tied to each analog input which will conduct for analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

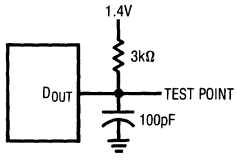
Note 7: Channel leakage current is measured after the channel selection.

TEST CIRCUITS

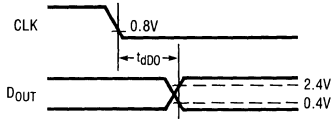
On and Off Channel Leakage Current



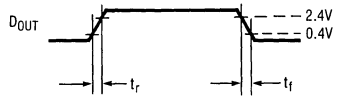
Load Circuit for t_{dDO}, t_r, and t_f



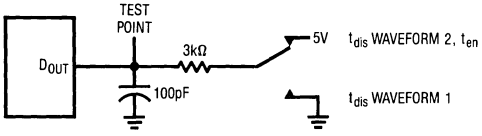
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



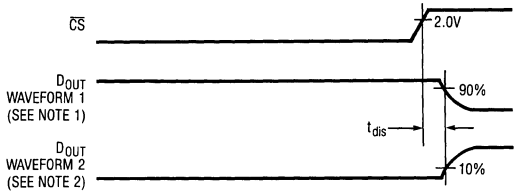
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f



Load Circuit for t_{dis} and t_{en}



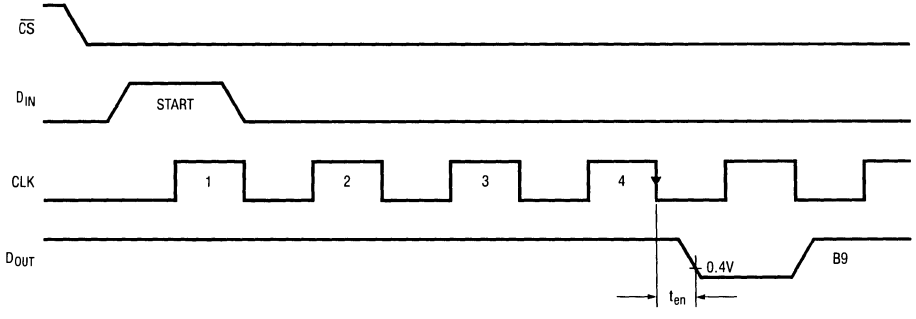
Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

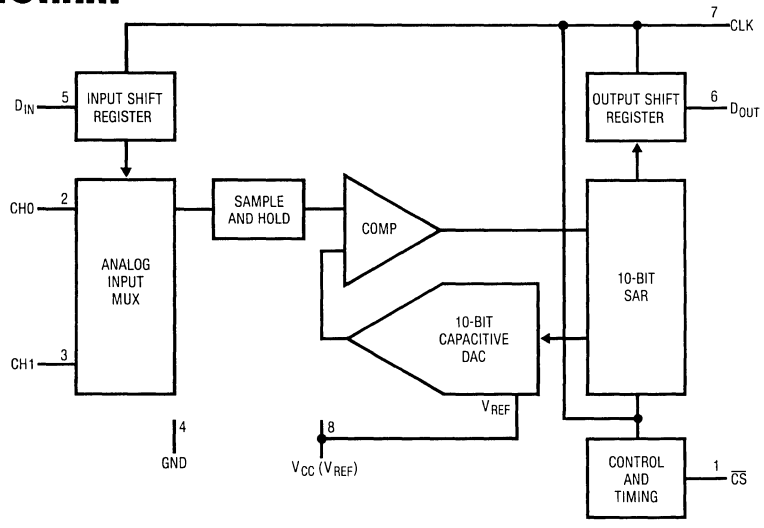
Voltage Waveforms for t_{en}



PIN FUNCTIONS

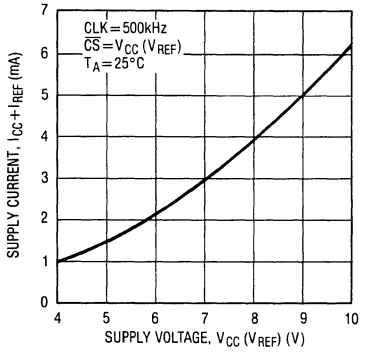
#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1091.
2, 3	CH0, CH1	Analog Inputs	These inputs must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	D_{IN}	Digital Data Input	The multiplexer address is shifted into this input.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	V_{CC} (V_{REF})	Positive Supply and Reference Voltage	This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

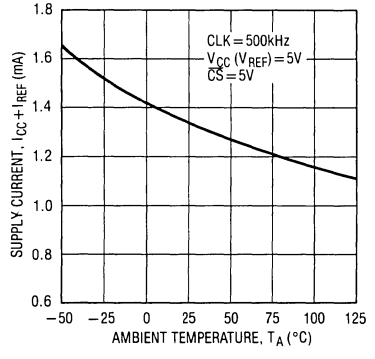


TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage

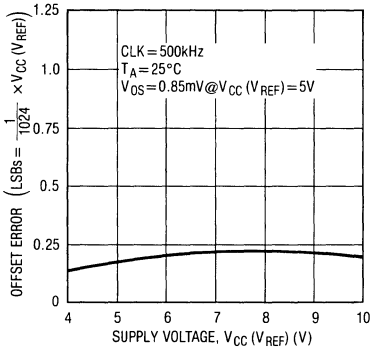


Supply Current vs Temperature

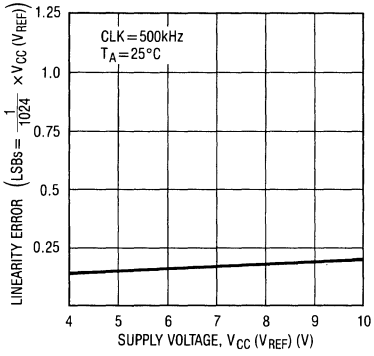


TYPICAL PERFORMANCE CHARACTERISTICS

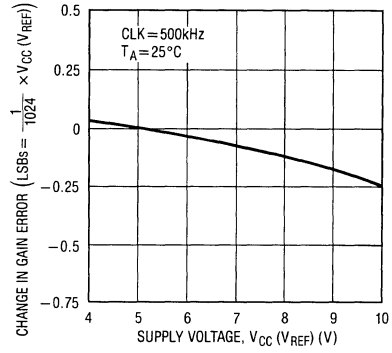
Offset Error vs Supply Voltage



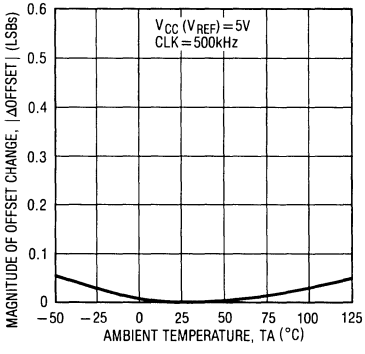
Linearity Error vs Supply Voltage



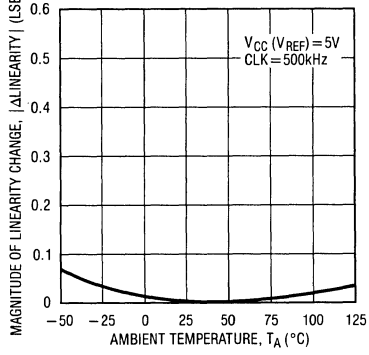
Change in Gain Error vs Supply Voltage



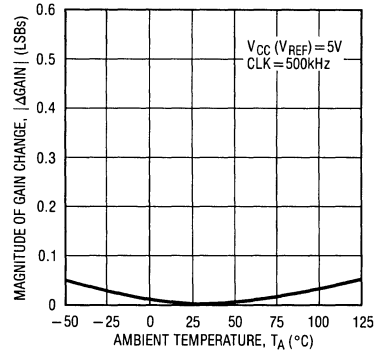
Change in Offset Error vs Temperature



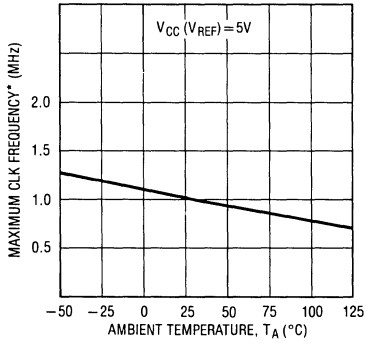
Change in Linearity Error vs Temperature



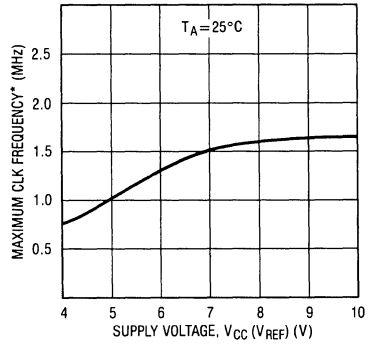
Change in Gain Error vs Temperature



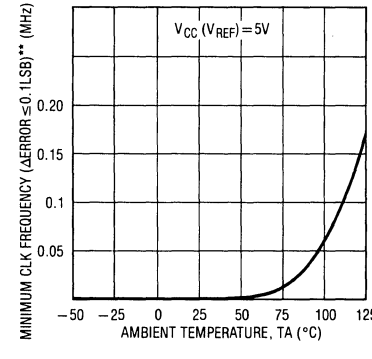
Maximum Clock Rate vs Temperature



Maximum Clock Rate vs Supply Voltage



Minimum Clock Rate vs Temperature

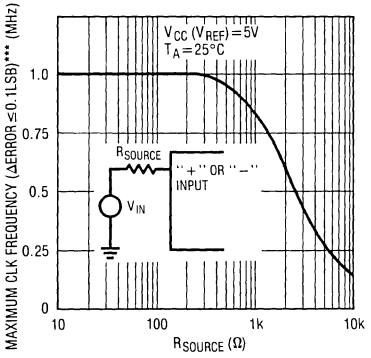


*MAXIMUM CLK FREQUENCY REPRESENTS THE HIGHEST FREQUENCY AT WHICH CLK CAN BE OPERATED (WITH 50% DUTY CYCLE) WHILE STILL PROVIDING 100ns SETUP TIME FOR THE DEVICE RECEIVING THE D_{OUT} DATA.

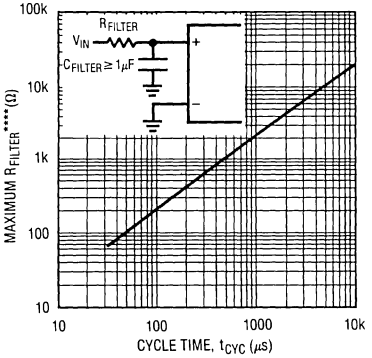
**AS THE CLK FREQUENCY IS DECREASED FROM 500kHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

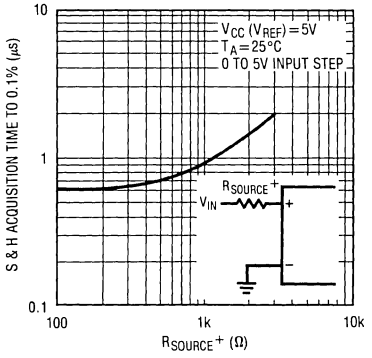
Maximum Clock Rate vs Source Resistance



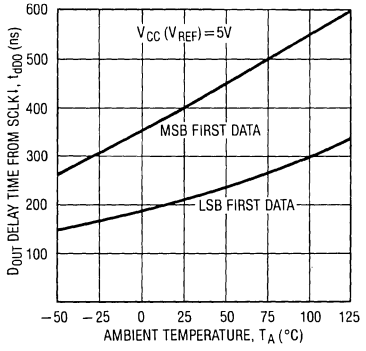
Maximum Filter Resistor vs Cycle Time



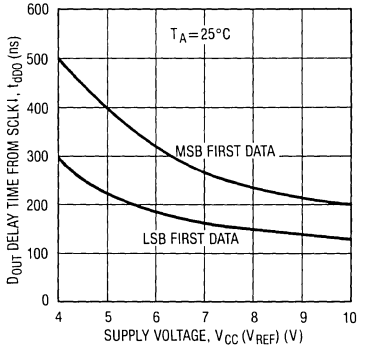
Sample and Hold Acquisition Time vs Source Resistance



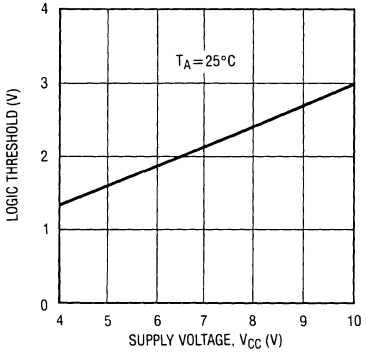
DOUT Delay Time vs Temperature



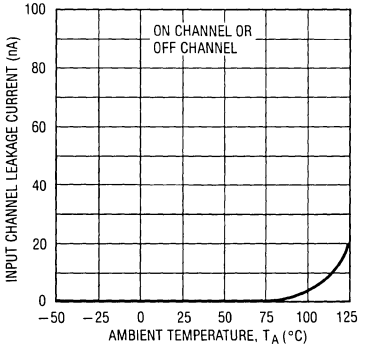
DOUT Delay Time vs Supply Voltage



Digital Input Logic Threshold vs Supply Voltage



Input Channel Leakage Current vs Temperature



***AS THE CLK FREQUENCY AND SOURCE RESISTANCE ARE INCREASED, MAXIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz, 0Ω VALUE IS FIRST DETECTED.

****MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0 IS FIRST DETECTED.

APPLICATIONS INFORMATION

The LTC1091 is a data acquisition component which contains the following functional blocks:

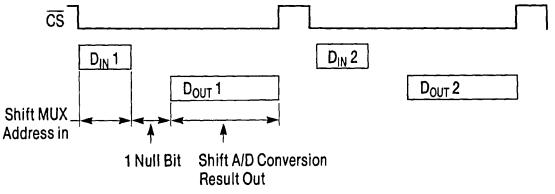
1. 10-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, half duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

1. Serial Interface

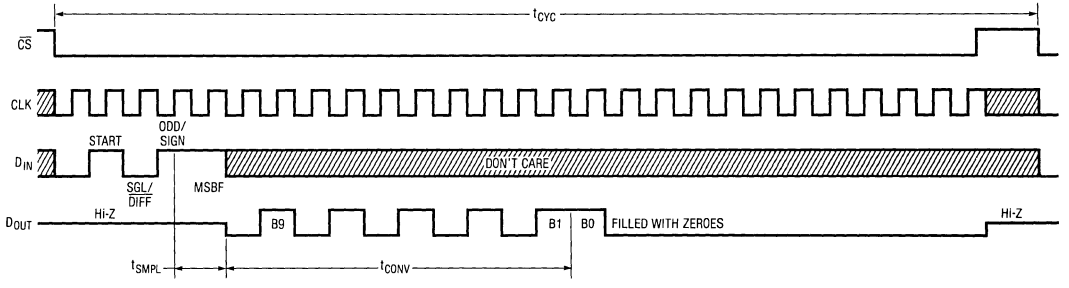
The LTC1091 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1091 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1091 looks for a start bit. After the start bit is received, a 3-bit input word is shifted into the D_{IN} input which configures the LTC1091 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1091 in preparation for the next data exchange.

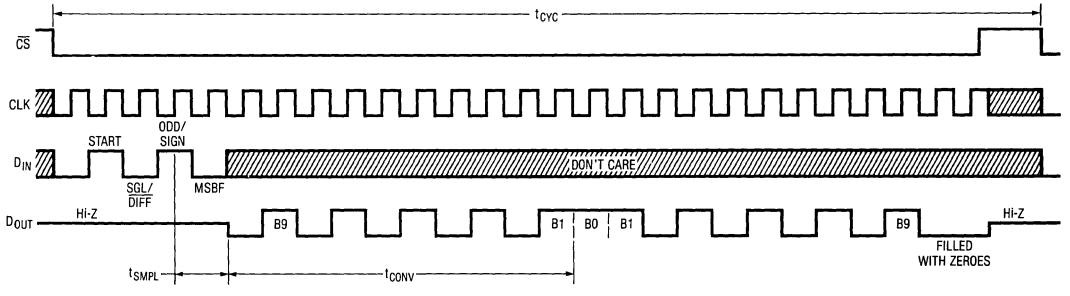


Operating Sequence
Example: Differential Inputs (CH1 + , CHO –)

MSB First Data (MSBF = 1)



LSB First Data (MSBF = 0)



APPLICATIONS INFORMATION

2. Input Data Word

The LTC1091 clocks data into the D_{IN} input on the rising edge of the clock. The four bit input data word is defined as follows:

Start	SGL/$\overline{\text{DIFF}}$	ODD/SIGN	MSBF
	MUX Address		MSB First/ LSB First

Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1091 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining 3 bits of the input word will be clocked in. Further inputs on the DIN pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The two bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of of the following table. In single ended mode, all input channels are measured with respect to GND.

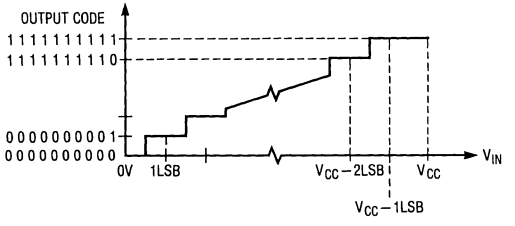
	MUX ADDRESS		CHANNEL #		GND
	SGL/$\overline{\text{DIFF}}$	ODD/SIGN	0	1	
Single-ended MUX mode	1	0	+		–
	1	1		+	–
Differential MUX mode	0	0	+	–	
	0	1	–	+	

MSB First/LSB First (MSBF)

The output data of the LTC1091 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the DOUT line. (See operating sequence).

Transfer Curve

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{CC} = 5V)
1111111111	V_{CC} – 1LSB	4.9951V
1111111110	V_{CC} – 2LSB	4.9902V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0049V
0000000000	0V	0V



APPLICATIONS INFORMATION

3. Accommodating Microprocessors with Different Word Lengths

The LTC1091 will fill zeroes indefinitely after the transmitted data until $\overline{CS}$ is brought high. At that time the D_{OUT} line is disabled. This makes interfacing easy to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS). Any word length can be accommodated by the correct positioning of the start bit in the LTC1091 input word.

Figure 1 shows examples of input and output words for 4-bit and 8-bit processors. A complete data exchange can be implemented with two 4-bit MPU outputs and three inputs in 4-bit systems and one 8-bit output and two inputs in 8-bit systems. The resulting data winds up left justified in the MPU with zeroes automatically filled in the unused low order bits by the LTC1091. In section 5 another example is given using the MC68HC05C4 in which one 8-bit transfer is saved and data is positioned right justified inside the MPU.

4. Operation with D_{IN} and D_{OUT} Tied Together

The LTC1091 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the MPU. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1091 will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 2). Therefore the processor port line must be switched to an input before this happens, to avoid a conflict.

In section 5, an example is made of interfacing the LTC1091 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

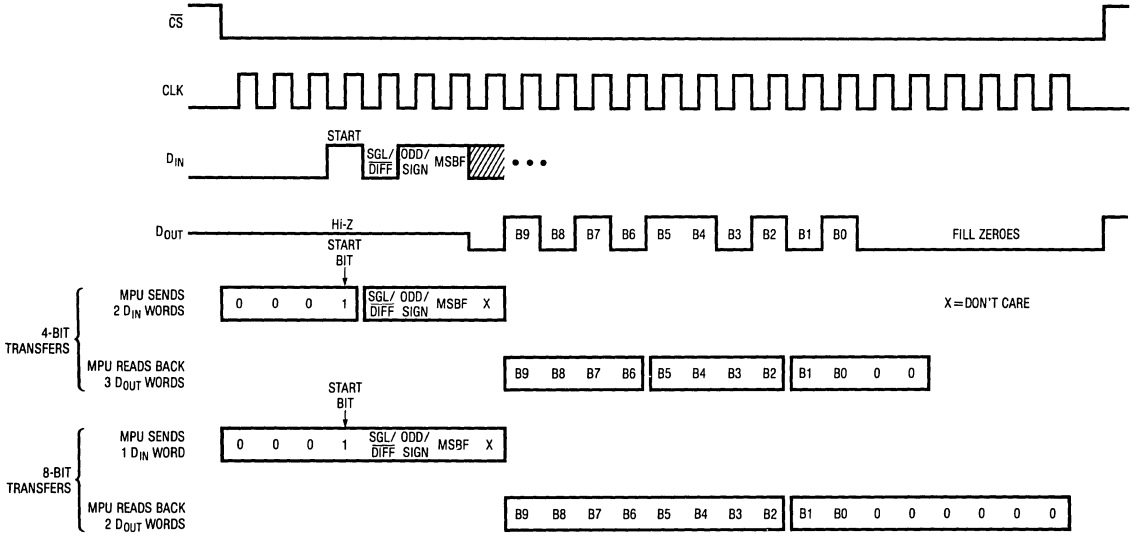


Figure 1. Example Input and Output Word Arrangements for 4-Bit and 8-Bit Serial Port Microprocessors

APPLICATIONS INFORMATION

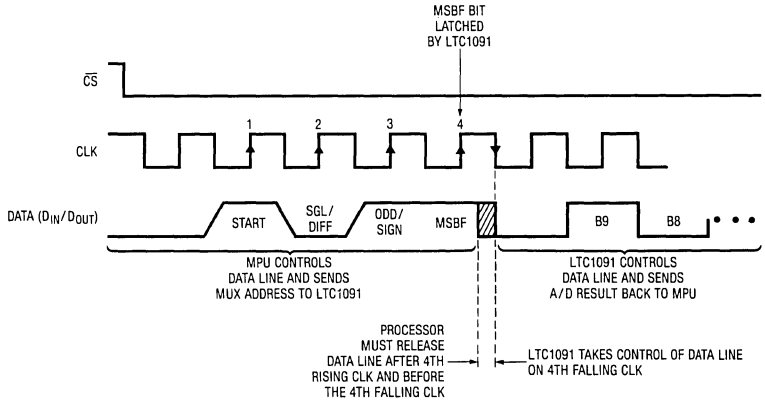


Figure 2. Operation with D_{IN} and D_{OUT} Tied Together

5. Microprocessor Interfaces

The LTC1091 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 2). If an MPU without a dedicated serial port is used, then 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1091. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Table 2. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1090

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port

*Requires external hardware
†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

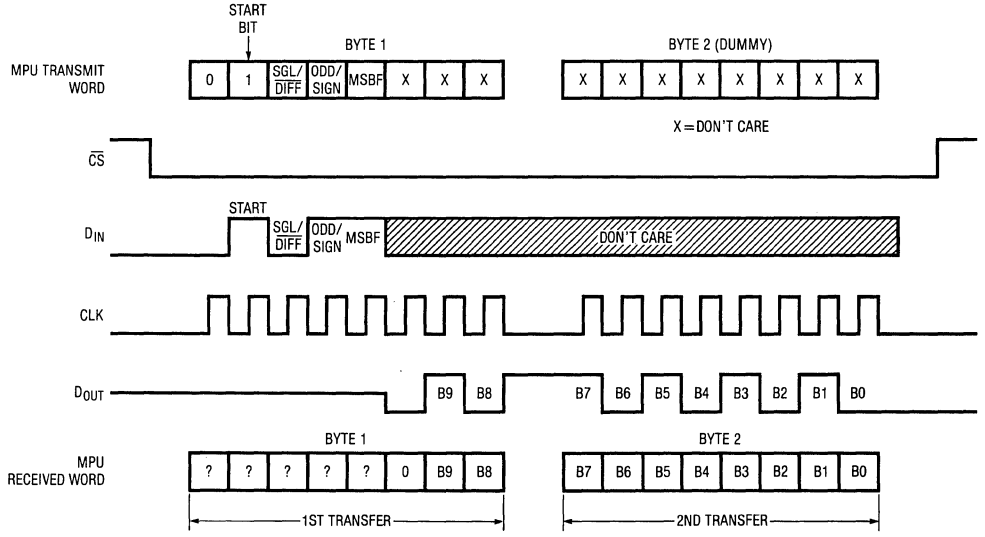
APPLICATIONS INFORMATION

Motorola SPI (MC68HC05C4, MC68HC11)

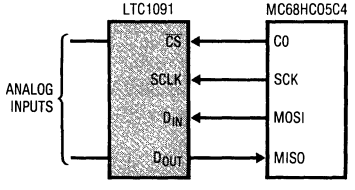
The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the D_{IN} word to the LTC1091 and clocks B9 and B8 of the A/D conversion result into the processor. The second 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU.

ANDing the first MPU received byte with 03 Hex clears the 6 most significant bits. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right justified in two memory locations.

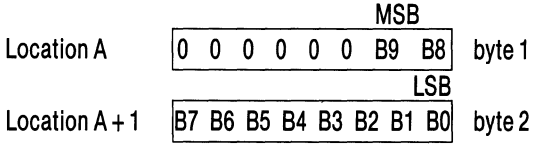
Data Exchange Between LTC1091 and MC68HC05C4



Hardware and Software Interface to Motorola MC68HC05C4 Microcontroller



D_{OUT} from LTC1091 stored in MC68HC05C4 RAM



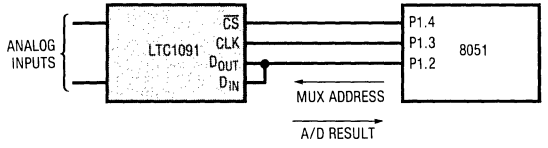
LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C goes low ($\overline{CS}$ goes low)
	LDA	Load LTC1090 D_{IN} word into Acc.
	STA	Load LTC1090 D_{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load contents of SPI data register into Acc. (D_{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear 6 MSBs of first D_{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C ($\overline{CS}$ goes high)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

APPLICATIONS INFORMATION

Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1091 and parallel port microprocessors. Normally the $\overline{CS}$, SCLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1091 tied together as described in section 4. This saves one wire.

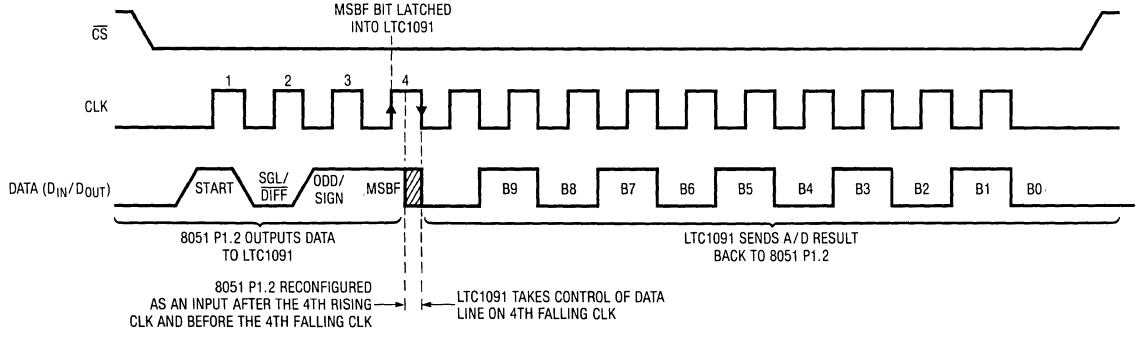
The 8051 first sends the start bit and MUX address to the LTC1091 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 10-bit A/D result over the same data line.



LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} word for LTC1091
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
	MOV	R4, #04	Load counter
LOOP 1	RLC	A	Rotate D_{IN} bit into Carry
	CLR	P1.3	SCLK goes low
	MOV	P1.2, C	Output D_{IN} bit to LTC1091
	SETB	P1.3	SCLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	SCLK goes low
	MOV	R4, #09	Load counter
LOOP	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP	Next bit
	MOV	R2, A	Store MSBs in R2
	MOV	C, P1.2	Read data bit into Carry
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	CLR	A	Clear Acc.
	RLC	A	Rotate data bit from Carry to Acc.
	MOV	C, P1.2	Read data bit into Carry
	RRC	A	Rotate right into Acc.
	RRC	A	Rotate right into Acc.
	MOV	R3, A	Store LSBs in R3
	SETB	P1.4	$\overline{CS}$ goes high

D_{OUT} from LTC1091 stored in 8051 RAM

	MSB							LSB
R2	B9	B8	B7	B6	B5	B4	B3	B2
R3	B1	B0	0	0	0	0	0	0



APPLICATIONS INFORMATION

Sharing the Serial Interface

The LTC1091 can share the same 3 wire serial interface with other peripheral components or other LTC1091s (see Figure 3). In this case, the $\overline{CS}$ signals decide which LTC1091 is being addressed by the MPU.

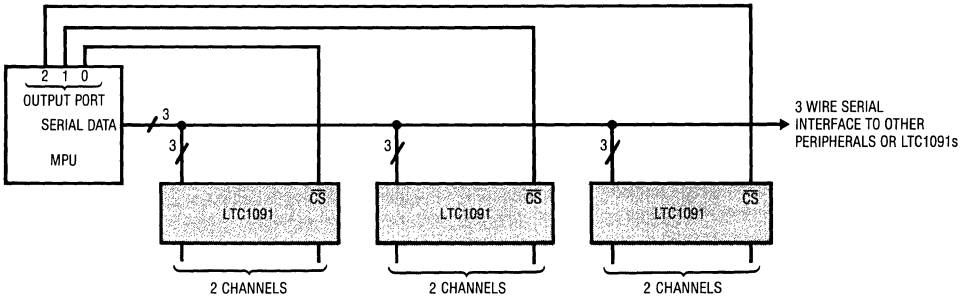


Figure 3. Several LTC1091s Sharing One 3 Wire Serial Interface

ANALOG CONSIDERATIONS

1. Grounding

The LTC1091 should be used with an analog ground plane and single point grounding techniques.

Pin 4 (GND) should be tied directly to this ground plane.

Pin 8 (V_{CC} (V_{REF})) should be bypassed to the ground plane with a 4.7μF tantalum with leads as short as possible.

All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the analog circuitry.

Figure 4 shows an example of an ideal ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

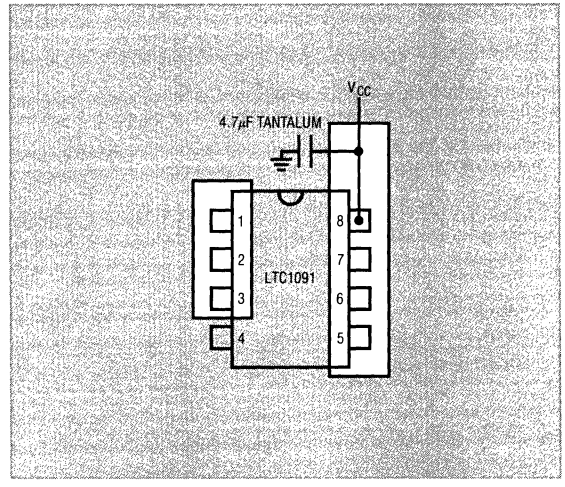


Figure 4. Example Ground Plane for the LTC1091

APPLICATIONS INFORMATION

2. Bypassing of the V_{CC} (V_{REF}) Pin

The V_{CC} (V_{REF}) pin of the LTC1091 defines the voltage span of the A/D converter and provides power to the internal circuitry and logic.

For good performance, V_{CC} (V_{REF}) must be free of noise and ripple. Any changes in the V_{CC} (V_{REF}) voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} (V_{REF}) noise and ripple can be kept below 1mV by driving V_{CC} (V_{REF}) from a clean supply and bypassing the V_{CC} (V_{REF}) pin directly to the analog ground plane with a 4.7μF tantalum with leads as short as possible. Figures 5 and 6 show the effects of good and poor V_{CC} (V_{REF}) bypassing.

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1091 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1091 look like a 60pF capacitor (C_{IN}) is series with a 500Ω resistor (R_{ON}) as shown in Figure 7. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

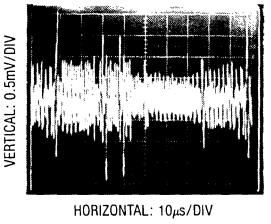


Figure 5. Poor V_{CC} (V_{REF}) Bypassing. Noise and Ripple can Cause A/D Errors

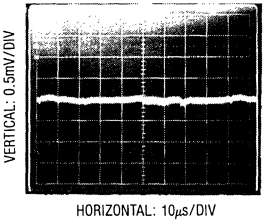


Figure 6. Good V_{CC} (V_{REF}) Bypassing Keeps Noise and Ripple on V_{CC} (V_{REF}) Below 1mV

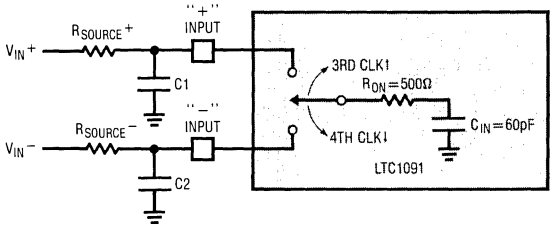


Figure 7. Analog Input Equivalent Circuit

APPLICATIONS INFORMATION

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 8). The sample phase starts at the 3rd CLK cycle and lasts until the falling edge of the 4th CLK. The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3μs, **$R_{SOURCE}^+ < 2k$ and C1 < 20pF will provide adequate settling.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 8). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the "–" input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency. At the maximum CLK rate of 500kHz, **$R_{SOURCE}^- < 1k\Omega$ and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 8). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT1006 and LT1013 single supply op amps, can be made to settle well even with the minimum settling windows of 3μs ("+" input) and 2μs ("–" input) which occur at the maximum clock rate of 500kHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

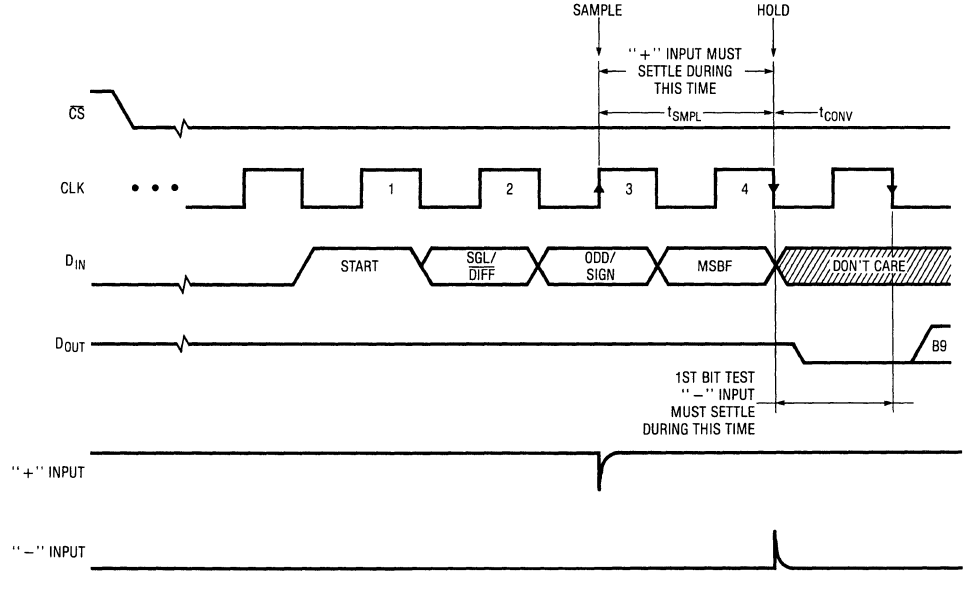


Figure 8. "+" and "–" Input Settling Windows

APPLICATIONS INFORMATION

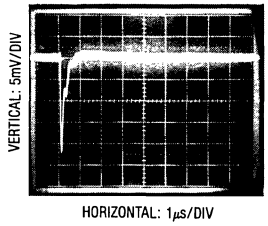


Figure 9. Adequate Settling of Op Amp Driving Analog Input

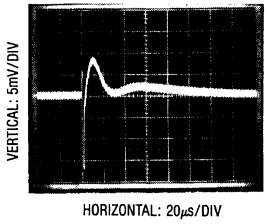


Figure 10. Poor Op Amp Settling can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1μF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 60pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 32μs, the input current equals 9μA at $V_{IN} = 5V$. In this case, a filter resistor of 50Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

4. Sample and Hold

Single Ended Inputs

The LTC1091 provides a built-in sample and hold (S&H) function for signals acquired in the single ended mode. This sample and hold allows the LTC1091 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins as the ODD/SIGN MUX address bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On the falling edge of the 4th CLK, the S&H goes into hold mode and the conversion begins.

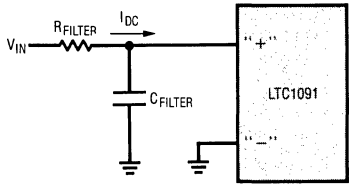


Figure 11. RC Input Filtering

APPLICATIONS INFORMATION

Differential Inputs

With differential inputs, the A/D no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 10 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR(MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{"}-\text{"}) \times 10/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (1.25mV) with the converter running at CLK = 500kHz, its peak value would have to be 150mV.

5. Other Data Acquisition Family Members

LTC1092: Reduced Span Operation

The minimum span of the LTC1091 is limited to about 4.5V because the reference input (V_{REF}) is internally tied to V_{CC}. If operation with a smaller span is desired, another member of Linear Technology's data conversion family should be considered: the LTC1092. This 8 pin device is similar to the LTC1091 except that a separate reference input (V_{REF}) is provided on pin 5. This allows the span to be reduced to 1V or below. The D_{IN} pin is eliminated and the LTC1092 is programmed for a single differential input.

LTC1090: More Input Channels and Bipolar Mode

For applications where more than two analog signals must be digitized, the LTC1090 should be considered. This 20 pin device provides 8 analog inputs, each of which can be configured for unipolar or bipolar conversions and for single ended or differential inputs. The LTC1090 also has a separate reference input to allow operation with reduced spans.

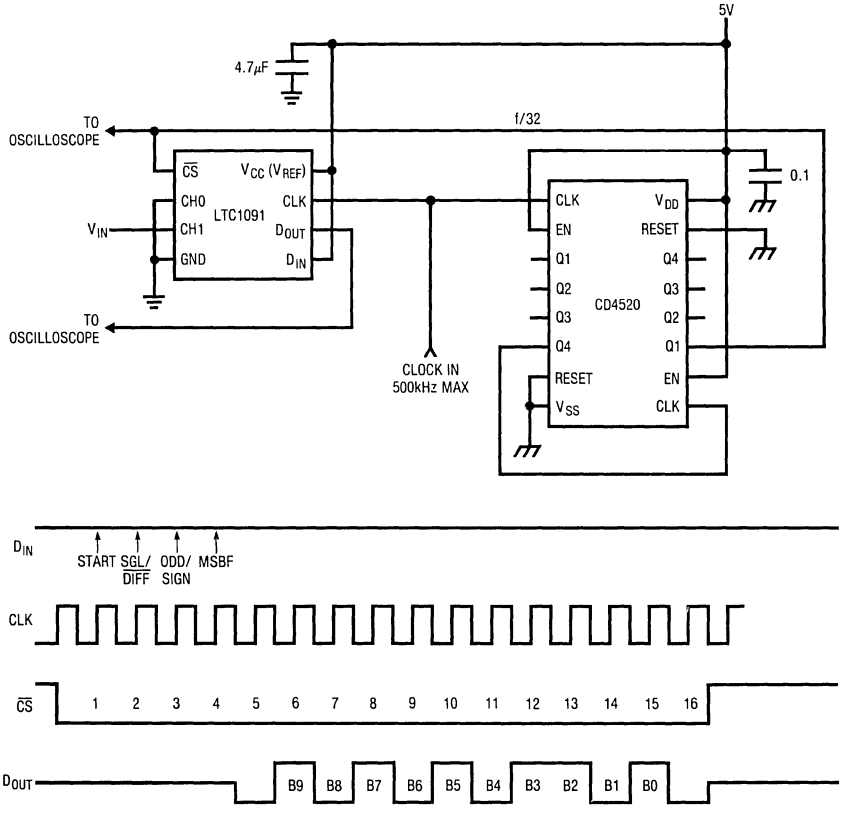
TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1091

Users can get a quick look at the function and timing of the LTC1091 by using the following simple circuit. D_{IN} and V_{CC} are tied to 5V selecting CH1 as a single ended input with a 5V span and MSB first output data. A 500kHz clock is applied to the CLK input and $\overline{CS}$ is driven at 1/32nd the clock rate by the CD4520. CH0 and GND are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of $\overline{CS}$.

TYPICAL APPLICATIONS

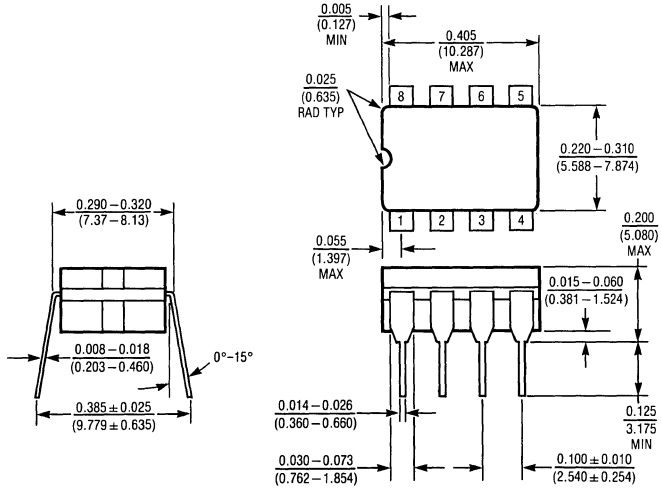
A "Quick Look" Circuit for the LTC1091



Scope Trace of LTC1091 "Quick Look" Circuit
Showing A/D Output of 1010101010 (682 Decimal)

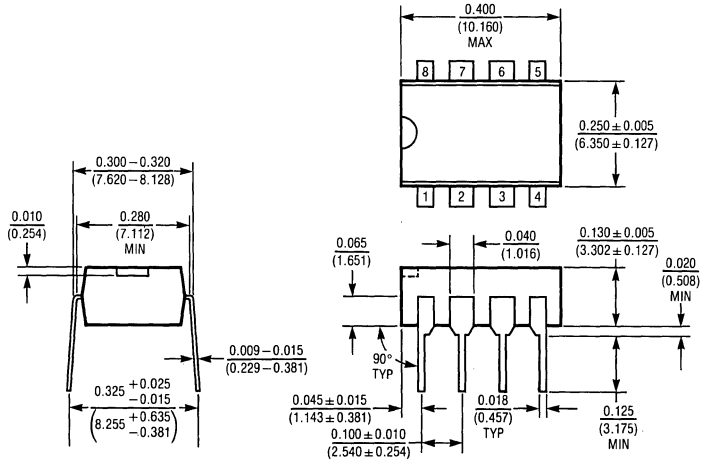
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8 Lead Hermetic DIP



T_{jmax}	θ_{JA}
150°C	100°C/W

N8 Package
8 Lead Plastic



T_{jmax}	θ_{JA}
110°C	150°C/W

SECTION 9—MILITARY PRODUCTS

SECTION 9—MILITARY PRODUCTS

NOTE

Material contained in this section has been substantially revised since first published in the 1986 Linear Databook. For the most current military information, consult these pages or contact the factory.

LINEAR TECHNOLOGY MIL/JAN PRODUCTS

Linear Technology Corporation offers a comprehensive selection of precision voltage references, operational amplifiers, voltage regulators, comparators, and CMOS circuits designed specifically to serve the rigorous requirements of the military marketplace.

The company's specification system and quality procedures and policies were set up from the beginning to meet the exacting demands of MIL-Q-9858 (Quality Program Requirements), MIL-I-45208 (Inspection System Requirements), MIL-M-38510 (General Specification For Microcircuits) and MIL-STD-883 (Test Methods and Procedures For Microelectronics).

Compliance to these specifications is a statutory requirement for all employees at Linear Technology. The programs now in place that serve the varied requirements for ground, sea, air, and space applications include:

- JAN
- Standard Military Drawings (SMD)
- Hi-Rel (SCD)
- 883

Linear Technology JAN

At the end of 1969, the Solid State Applications Branch of the Rome Air Development Center (RADC) issued the first copy of MIL-M-38510. This general specification for microcircuits established the procedures that a manufacturer must follow to have his products listed on the Qualified Parts List (QPL).

One major problem faced by defense contractors using semiconductor devices was the inability to interchange devices caused by a proliferation of non-standard electrical specifications. The 38510 (JAN) program addressed this problem by publishing detailed electrical specifications (slash sheets) for each component to be listed on the QPL.

JAN devices are completely processed in the United States or its territories and all wafer fabrication, wafer sort, assembly, testing, and conformance testing are performed onshore.

In early 1985, Linear Technology Corporation joined the ranks of the eighteen existing QPL suppliers. Of these eighteen, only a handful of suppliers participate in the linear military JAN market. Linear Technology believes its analog design experience and manufacturing strength can contribute significantly to this market.

In August 1984, Linear Technology Corporation was visited by a team of DESC (Defense Electronics and Supply Center) personnel. This team spent almost four days on their audit and at the end of the visit they awarded the company "line certification". *This was a first for any company to receive this distinction on a first audit!* A reaudit took place in 1986 and our record still stands.

Linear Technology's first QPL listing was achieved in February, 1985, one year after the company made JAN Class B a corporate goal. Other companies have typically taken 2 to 3 years to achieve this status. The line certification and QPL approvals were awarded to the *new MIL-38510 Rev. F* and *MIL-STD-883 Rev. C* specifications.

Linear Technology's policy of providing JAN Class B linear components supports the United States Government's position of standardization to decrease the number of active part types maintained by DESC. This number is currently in excess of 70,000 for all types of components (contrasted to approximately 5,000 industry standard components). Standardization will clearly decrease costs and assist in the maintenance of military weapon systems and equipment now in the field. Linear Technology Corporation has over 30 products listed on the Qualified Parts List (Part 1) and we have an active and aggressive program to further expand our offering of JAN products.

EXAMPLES OF LINEAR TECHNOLOGY MILITARY PROGRAM PARTICIPATION

AMRAAM	SPARROW	PERSHING II
PHOENIX	HARPOON	MINUTEMAN
PHALANX	HARM	B-1B
F-15	COPPERHEAD	B-52
F-16	GPS	TOW
F-18	HTTB	MAVERICK
DRAGON	SEAHAWK	ACTS
STD. MISSILE	FLEET SATCOM	M-1 TANK

Linear Technology Standard Military Drawings

DESC drawings were initiated in 1976 to standardize the electrical requirements for full temperature-tested military components. These DESC drawings (or minispecs) were initially issued for low power Schottky devices (54LS) used by defense subcontractors on the Air Force's F16. The program accomplished standardization of testing, without the delays associated with the qualification process for JAN components.

The DESC drawing was viewed as a preliminary specification prior to JAN approval, and it ranks second in the order of purchasing hierarchy to JAN. This order is defined in Requirement 64 of MIL-STD-454. If a JAN part is available, it is still preferred, however, there are many types of devices where the volume is such that the cost of a full JAN qualification may not be justified, but where a need exists for electrical standardization.

CMOS and analog circuits were added to the DESC Drawing Program in 1977, 1978 and 1979, but widespread acceptance of these parts was not achieved. Today with more emphasis being placed on standardization, the interest level in DESC drawings has accelerated. This category of product can be built offshore with 883-level processing and the electrical parameters are tested specifically to the DESC drawing.

To provide parts to a DESC drawing, a manufacturer has to have at least one part on the 38510 Qualified Parts List. He must also provide DESC with a certificate of compliance agreeing to the tests and conditions listed on the drawing.

In 1986 a new program named Standard Military Drawings (SMDs) was launched by DESC. This replaced the previous DESC Drawing Program. This new program is aimed directly at standardizing electrical requirements with the objective to decrease the time required to issue a military drawing. To achieve this, we have set up a computer link-up with the DESC Standardized Mil Drawing Group. A flowchart showing the preparation of Mil drawings is shown in Figure 1. Linear Technology is actively supporting this new Mil Drawing program and we are working closely with DESC and OEMs to participate in this government plan toward a greater level of standardization in military specifications.

Linear Technology has a number of devices listed on DESC and Mil drawings, and we are actively supporting these standardization programs by having parts available off the shelf from Linear Technology Corporation and from distribution outlets.

Linear Technology Hi-Rel

Linear Technology Corporation recognizes the need for source controlled drawings (SCD's) and the company's DESC-certified line is well equipped to handle these requirements for space and hi-rel applications. The company has a comprehensive review procedure and emphasis is placed on compliance to test methods and procedures. Over 2,800 specifications have been reviewed to date with fast feedback to our customers.

Linear Technology has serviced source controlled drawing orders including "S" level specifications with a variety of source inspection and conformance test requirements. Each source controlled drawing requires dedicated flows, software and hardware, and as a result, certain minimum requirements have to be fulfilled. Linear Technology's Product Marketing group can provide you with more details on a case-by-case basis.

Linear Technology MIL-STD-883 Product

The semiconductor industry 883 designation on military semiconductor components established a defacto standard in response to a significant demand from the military defense contractors. The Government recognized the existence of 883 components in the recent revisions of MIL-STD-883C and MIL-M-38510F, and the requirements for compliant 883 components are now defined very specifically in these documents.

MIL-STD-883 is a test procedures and methods document and the last major revision (Rev. C) became effective on June 1, 1984. This document is revised periodically and defines the conditions for two categories of product, Class B and Class S. Class B is intended for applications where maintenance is difficult or expensive and where reliability is vital. Class S is intended for space and critical applications where replacement is extremely difficult or impossible and where reliability is imperative. The Class B PDA (Percent Defective Allowable) was tightened from 10% to 5% following

burn-in and the Group A electrical sampling plans (LTPD levels) also were tightened. In addition, a critical paragraph was added to MIL-STD-883 to alleviate any misinterpretation; a factor that had previously created vastly different 883 programs throughout the semiconductor industry.

On December 31, 1984, another key clause was added to MIL-STD-883 Rev. C, "paragraph 1.2.1." This states that if a manufacturer advertises, certifies, or marks parts as compliant with MIL-STD-883 those parts must meet all of the provisions of MIL-STD-883, a practice consistent with "Truth in Advertising".

According to the Defense Electronics Supply Center (a branch of the Defense Department's Logistics Agency), the intent of paragraph 1.2.1 was to link MIL-STD-883 with the controls and details contained in MIL-M-38510.

Linear Technology Corporation can state unequivocally that all of its 883 products are in full compliance with the new MIL-STD-883 Rev. C requirements. We have over 275 versions of our 883 products listed in our current catalog, including operational amplifiers, voltage regulators, voltage references, comparators, and our advanced line of proprietary CMOS circuits.

All products manufactured by Linear Technology are designed to meet the full requirements of the military, from –55°C to 125°C.

Military Market Commitment

Linear Technology Corporation is a focused, dedicated company servicing the needs of the linear military marketplace. We are shipping to the top U.S. defense electronics contractors who have qualified and approved our products. Linear Technology Corporation is committed to being the best and most proficient high quality supplier of analog military components.

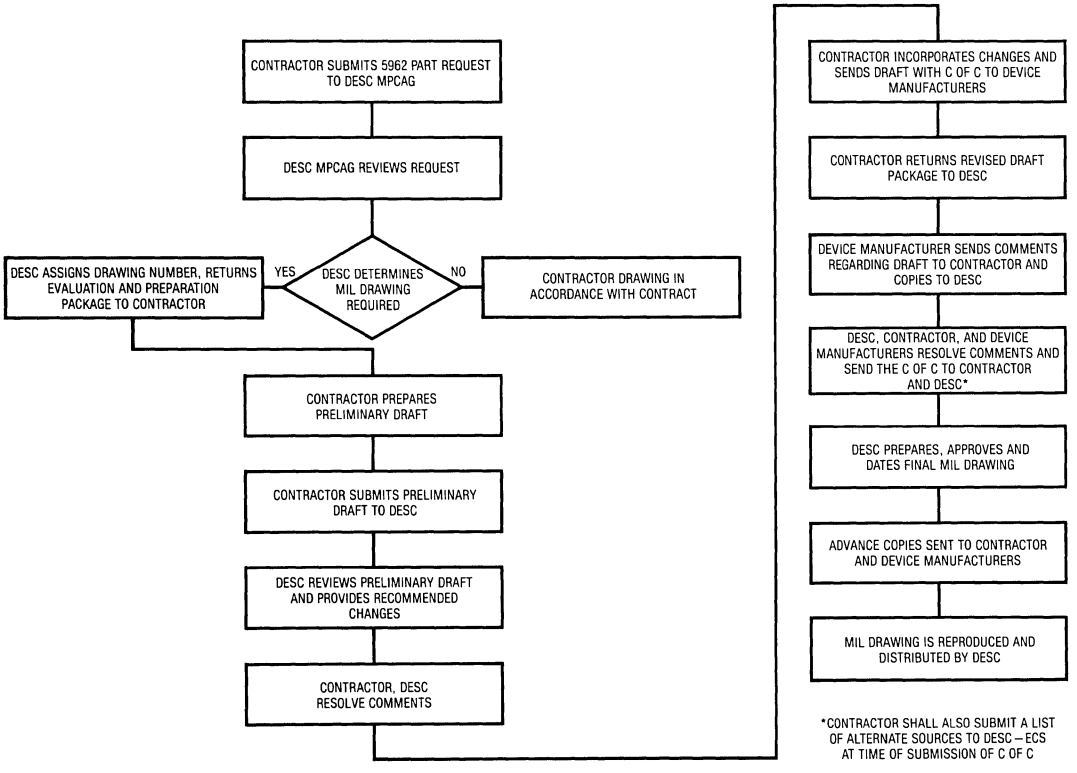
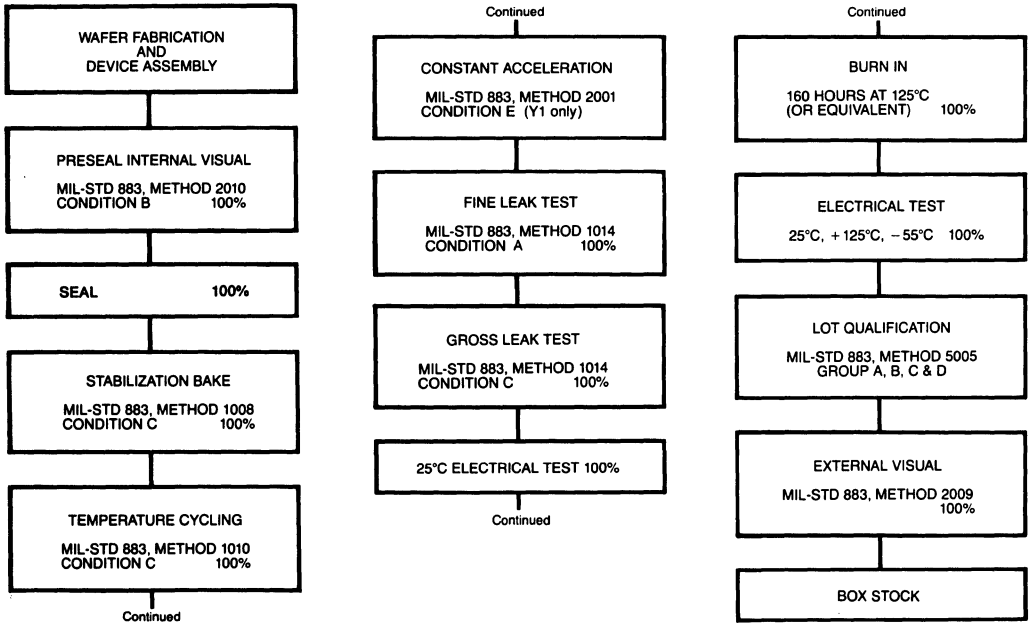


Figure 1. Mil Drawing Preparation Flowchart

883 PRODUCT FLOW — CLASS B



LINEAR TECHNOLOGY 883 GROUP A SAMPLING PLAN

TEST	CONDITION	883C (CLASS B)	
		SAMPLE SIZE	LTPD
DC Parametric	$T_A = 25°C$	116	2.0%
DC Parametric	$T_A = -55°C$ to $+125°C$	116	2.0%
AC Parametric	$T_A = 25°C$	116	2.0%

883 CERTIFICATE OF CONFORMANCE—LEVEL B

LTC Part Number _____

Lot Traceability No. _____

Purchase Order No. _____

QUALITY ASSURANCE INSPECTOR	
DATE	SIGNATURE

Customer Name _____ P/N _____ Qty _____

Date Code _____ Shipper # _____ Traveller Lot # _____

Group A = _____ Group B = _____ Group C = _____ Group D = _____

Group A Re-Inspection Data, If Applicable _____

LINEAR TECHNOLOGY CORPORATION HEREBY DECLARES THAT THE COMPONENTS SPECIFIED ON THE ABOVE PURCHASE ORDER COMPLY WITH YOUR SPECIFICATIONS AND REQUIREMENTS OF MIL-STD 883 REV C. ALL SUPPORTING DOCUMENTATION AND RECORDS ARE RETAINED ON FILE BY LTC AND ARE AVAILABLE FOR INSPECTION. THE MAJOR ELEMENTS OF THE 883C PROGRAM ARE SHOWN BELOW.

Operation	Screening Procedure MIL-STD-883C Method 5004
Internal Visual	Method 2010, Condition B
Stabilization Bake	Method 1008, Condition C
Temperature Cycling	Method 1010, Condition C, 10 cycles – 65°C to 150°C
Constant Acceleration	Method 2001, Condition E, 30K G's Y1 axis (TO-3 PKG at 20K G's)
Fine Leak	Method 1014, Condition A
Gross Leak	Method 1014, Condition C
Burn-in	Method 1015, 160 hrs at 125°C (or equivalent)
Final Electrical	+ 25°C DC (per LTC Data Sheet) PDA = 5% + 125°C or 150°C DC – 55°C DC + 25°C AC
QA Acceptance	Method 5005 Group A (sample/lot)
Quality Conformance	Group B (sample/lot) Group C (sample every 3 months/Generic Group) Group D (sample every 6 months/Package Type)
External Visual	Method 2009

NOTE: Each operation is performed on a 100% basis unless otherwise stated.

FORM. NO. 00-03-6072

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP A DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

	LTPD	ACC #	S/S	# FAILED	DATE TEST	OPER NUMBER
SUBGROUP 1 Static test at 25°C	2%					
SUBGROUP 2 Static tests at maximum rated operating temperature	2%					
SUBGROUP 3 Static tests at minimum rated operating temperature	2%					
SUBGROUP 4 Dynamic tests at 25°C	2%					
SUBGROUP 5 Dynamic tests at maximum rated operating temperature	2%					
SUBGROUP 6 Dynamic tests at minimum rated operating temperature	2%					
SUBGROUP 7 Functional tests at 25°C	SAME AS SUBGROUP #1					
SUBGROUP 8 Functional tests at maximum and minimum operating temperature	SAME AS SUBGROUPS 2 & 3					
SUBGROUP 9 Switching tests at 25°C	2%					
SUBGROUP 10 Switching tests at maximum rated operating temperature	2%					
SUBGROUP 11 Switching tests at minimum rated operating temperature	2%					

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6037

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Physical Dimensions	2016			0	2			
SUBGROUP 2 Resistance to Solvents	2015			0	4			
SUBGROUP 3 Solderability	2003	Soldering Temp. of 245 ± 5°C	10	0				
SUBGROUP 4 Internal Visual/Mechanical	2014	design and construction requirements		0	1			
SUBGROUP 5 Bond Strength	2011	C or D	15	0				
SUBGROUP 7 Fine Leak Gross Leak	1014		5	0				

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6006

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP C DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT # _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
CT. GROUP: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Steady State Life Test	1005	T_A = 125°C (1000 Hours or Equiv.)	5	0	45			
Electrical Endpoints		Test #						
SUBGROUP 2 Temperature Cycling	1010	C	15	0	15			
Constant Acceleration	2001	E Y1 only						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1010/ 1011							
Electrical Endpoints		Test #						

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6007

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP D DATA
Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1			15	0	15			
Physical Dimensions	2016							
SUBGROUP 2			15	0	15			
Lead Integrity	2004	B2 (lead fatigue)						
Fine Leak	1014							
Gross Leak	1014							
SUBGROUP 3			15	0	15			
Thermal Shock	1011	B 15 cycles						
Temperature Cycle	1010	C 100 cycles						
Moisture Resistance	1004							
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1004/ 1010							
Electrical Endpoints		Test #						
SUBGROUP 4			15	0	15			
Mechanical Shock	2002	B						
Vibration Variables-Frequency	2007	A						
Constant Acceleration	2001	E Y1 only						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1010/ 1011							
Electrical Endpoints		Test #						
SUBGROUP 5			15	0	15			
Salt Atmosphere	1009	A						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1009	Visual Criteria						
SUBGROUP 6				0	3			
Internal Water-Vapor	1018	5000ppm						
SUBGROUP 7			15	0	15			
Adhesion of Lead Finish	2025							
SUBGROUP 8				0	5			
Lid Torque	2024	Glass Frit Seal only						

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6008

MILITARY PARTS LIST

JAN QPL†

JM38510/10104BGA (LM108AH)	JM38510/11402BGC (LF156H)	JM38510/11804BYA (LM137K)
JM38510/10104BGC (LM108AH)	JM38510/11404BGA (LF155AH)	JM38510/13501BGA (OP07AH)
JM38510/10104BPA (LM108AJ8)	JM38510/11404BGC (LF155AH)	JM38510/13501BGC (OP07AH)
JM38510/10106BEA (LH2108AD)	JM38510/11405BGA (LF156AH)	JM38510/13501BPA (OP07AJ8)
JM38510/10107BGA (LM118H)	JM38510/11405BGC (LF156AH)	JM38510/13502BGA (OP07H)
JM38510/10107BGC (LM118H)	JM38510/11703BXA (LM117H)	JM38510/13502BGC (OP07H)
JM38510/10107BPA (LM118J8)	JM38510/11703BXC (LM117H)	JM38510/13502BPA (OP07J8)
JM38510/11401BGA (LF155H)	JM38510/11704BYA (LM117K)	JM38510/13503BGA (OP27AH)
JM38510/11401BGC (LF155H)	JM38510/11803BXA (LM137H)	JM38510/13503BGC (OP27AH)
JM38510/11402BGA (LF156H)	JM38510/11803BXC (LM137H)	JM38510/13503BPA (OP27AJ8)

DESC Drawings*

7703401XA (LM117H)	7703403YA (LM137K)	8601401CA (LM119H)
7703401XC (LM117H)	7703403YX (LM137K)	8601401CX (LM119H)
7703401YA (LM117K)	7703404XA (LM137HVH)	8601401IA (LM119J)
7703401YX (LM117K)	7703404XC (LM137HVH)	8601401IX (LM119J)
7703402XA (LM117HVH)	7703404YA (LM137HVK)	8601402CA (LT119AH)
7703402XC (LM117HVH)	7703404YX (LM137HVK)	8601402CX (LT119AH)
7703402YA (LM117HVK)	7802801EA (SG1524J)	8601402IA (LT119AJ)
7703402YX (LM117HVK)	7802801EX (SG1524J)	8601402IX (LT119AJ)
7703403XA (LM137H)	8418001XA (LM136AH-2.5)	
7703403XC (LM137H)	8418001XC (LM136AH-2.5)	

Standard Military Drawings (SMD)

5962-8680601EA (UC1846J)	5962-8688202XA (LH0070-1H)	5962-8688203XC (LH0070-2H)
5962-8688201XA (LH0070-0H)	5962-8688202XC (LH0070-1H)	5962-8688701EA (OP227AJ)
5962-8688201XC (LH0070-0H)	5962-8688203XA (LH0070-2H)	

883 Operational Amplifiers

LF155AH/883B	LT1001AMJ8/883B	LT1028AMJ8/883B	OP-07AJ8/883B
LF155H/883B	LT1001MH/883B	LT1028MH/883B	OP-07H/883B
LF156AH/883B	LT1001MJ8/883B	LT1028MJ8/883B	OP-07J8/883B
LF156H/883B	LT1002AMJ/883B	LT1037AMH/883B	OP-15AH/883B
LF412AM/883B	LT1002MJ/883B	LT1037AMJ8/883B	OP-15BH/883B
LF412MH/883B	LT1007AMH/883B	LT1037MH/883B	OP-15CH/883B
LH0070-0H/883B	LT1007AMJ8/883B	LT1037MJ8/883B	OP-16AH/883B
LH0070-1H/883B	LT1007MH/883B	LT1055AMH/883B	OP-16BH/883B
LH0070-2H/883B	LT1007MJ8/883B	LT1055MH/883B	OP-16CH/883B
LH2108AD/883B	LT1008MH/883B	LT1056AMH/883B	OP-27AH/883B
LH2108D/883B	LT1012MD/883B	LT1056MH/883B	OP-27AJ8/883B
LM10H/883B	LT1012MH/883B	LT1057AMH/883B	OP-27CH/883B
LM10J8/883B	LT1013AMH/883B	LT1057AMJ8/883B	OP-27CJ8/883B
LM101AH/883B	LT1013AMJ8/883B	LT1057MH/883B	OP-37AH/883B
LM101AJ8/883B	LT1013MH/883B	LT1057MJ8/883B	OP-37AJ8/883B
LM107H/883B	LT1013MJ8/883B	LT1058AMJ/883B	OP-37CH/883B
LM107J8/883B	LT1014AMJ/883B	LT1058MJ/883B	OP-37CJ8/883B
LM108AH/883B	LT1014MJ/883B	LTC1052MH/883B	OP-215AH/883B
LM108H/883B	LT1022AMH/883B	LTC1052MJ/883B	OP-215AJ8/883B
LM108AJ8/883B	LT1022MH/883B	LTC1052MJ8/883B	OP-215CH/883B
LM108J8/883B	LT1023MH/883B	OP-05AH/883B	OP-215CJ8/883B
LM118H/883B	LT1023MJ8/883B	OP-05AJ8/883B	OP-227AJ/883B
LM118J8/883B	LT1024AMD/883B	OP-05H/883B	OP-227CJ/883B
LT118AH/883B	LT1024MD/883B	OP-05J8/883B	OP-237AJ/883B
LT118AJ8/883B	LT1028AMH/883B	OP-07AH/883B	OP237CJ/883B
LT1001AMH/883B			

883 Regulators	LM117H/883B	LM137K/883B	LT137AH/883B	LT1005MK/883B
	LM117HVH/883B	LM138K/883B	LT137AHVH/883B	LT1020MJ/883B
	LM117HVK/883B	LM150K/883B	LT137AHVK/883B	LT1033MK/883B
	LM117K/883B	LT117AH/883B	LT137AK/883B	LT1035MK/883B
	LM123K/883B	LT117AHVH/883B	LT138AK/883B	LT1036MK/883B
	LM137H/883B	LT117AHVK/883B	LT150AK/883B	LT1038MK/883B
	LM137HVH/883B	LT117AK/883B	LT1003MK/883B	LT1054MJ8/883B
	LM137HVK/883B	LT123AK/883B		
883 References	AD580SH/883B	LM185H-2.5/883B	LT1021BMH-5/883B	LT1031DMH/883B
	AD580TH/883B	LM199AH/883B	LT1021CMH-5/883B	LT1034BMH/883B
	AD580UH/883B	LM199AH-20/883B	LT1021DMH-5/883B	LT1034MH/883B
	AD581SH/883B	LM199AH-50/883B	LT1021BMH-7/883B	REF-01AH/883B
	AD581TH/883B	LM199H/883B	LT1021DMH-7/883B	REF-01AJ8/883B
	LM129AH/883B	LT1004MH-1.2/883B	LT1021BMH-10/883B	REF-01H/883B
	LM129BH/883B	LT1004MH-2.5/883B	LT1021CMH-10/883B	REF-01J8/883B
	LM129CH/883B	LT1009MH/883B	LT1021DMH-10/883B	REF-02AH/883B
	LM134H/883B	LT1019MH-2.5/883B	LT1029AMH/883B	REF-02AJ8/883B
	LM136AH-2.5/883B	LT1019MH-5.0/883B	LT1029MH/883B	REF-02H/883B
	LM136H-2.5/883B	LT1019MH-6.2/883B	LT1031BMH/883B	REF-02J8/883B
	LM185H-1.2/883B	LT1019MH-10/883B	LT1031CMH/883B	
883 Comparators	LM111H/883B	LT111AJ8/883B	LT1011MH/883B	LT1017MJ8/883B
	LM111J8/883B	LT119AH/883B	LT1011MJ8/883B	LT1018MH/883B
	LM119H/883B	LT119AJ/883B	LT1016MH/883B	LT1018MJ8/883B
	LM119J/883B	LT1011AMH/883B	LT1016MJ8/883B	LTC1040MJ/883B
	LT111AH/883B	LT1011AMJ8/883B	LT1017MH/883B	LTC1042MJ/883B
883 Switched-Mode Control Circuits	LT1070MK/883B	LT1524J/883B	LT1527AJ/883B	SG1527AJ/883B
	LT1070HVMK/883B	LT1525AJ/883B	SG1524J/883B	UC1846J/883B
	LT1071MK/883B	LT1526J/883B	SG1525AJ/883B	UC1847J/883B
	LT1071HVMK/883B			
883 Interface	LT1032MJ/883B	LT1081MJ/883B		
	LT1039MJ/883B	LTC1045MJ/883B		
	LT1080MJ/883B			
Other 883	LF198AH/883B	LTC1041MJ8/883B	LTC1059AMJ/883B	LTC1061MJ/883B
	LF198H/883B	LTC1043MD/883B	LTC1059MJ/883B	LTC1062MJ8/883B
	LT1010MH/883B	LTC1044MH/883B	LTC1060AMJ/883B	
	LT1010MK/883B	LTC1044MJ8/883B	LTC1060MJ/883B	

†Parts may be ordered using an "X" lead finish suffix. These parts will be supplied with either gold plate or solder-dip finish at Linear Technology Corporation's discretion.

* Certain parts may be ordered with "C" lead finish suffix (gold plate). Consult factory for pricing and availability.

SECTION 10— NEW PRODUCTS

SECTION 10—NEW PRODUCTS

LT685

High Speed Comparator

FEATURES

- Ultra Fast (5.5ns typ)
- Complementary ECL Output
- 50Ω Line Driving Capability
- Low Offset Voltage
- Output Latch Capability
- External Hysteresis Control
- Pin Compatible with Am685

APPLICATIONS

- High Speed A to D Converters
- High Speed Sampling Circuits
- Oscillators

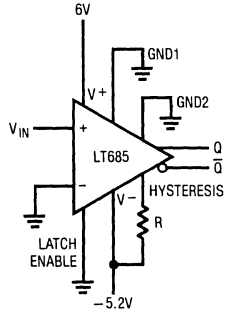
DESCRIPTION

The LT685 is an ultra-fast comparator with differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving transmission lines terminated in 50Ω. The low input offset and high resolution make this comparator ideally suited for anolog-to-digital signal processing applications.

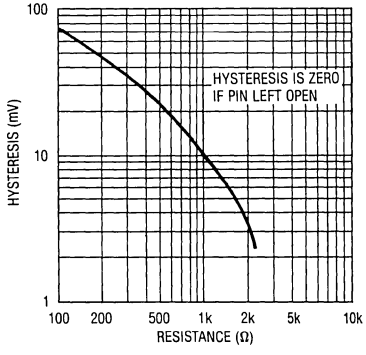
A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the comparator outputs are locked in their existing logical states. If the latch function is not used, the latch enable must be connected to ground or ECL high.

The device is pin-compatible with the Am685. Hysteresis has been added to improve switching time with slow input signals as well as to minimize oscillation. A single resistor between the hysteresis pin and V^- adds input hysteresis voltage as more current is drawn. If hysteresis is not required, the pin can be left unconnected.

Comparator with Hysteresis



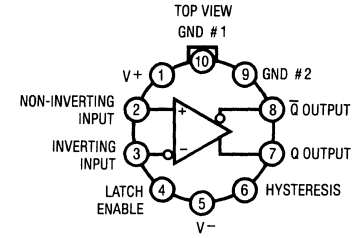
Hysteresis



ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage 7V
Negative Supply Voltage ..... −7V
Input Voltage ..... ±4V
Differential Input Voltage ..... ±6V
Latch Pin Voltage ..... 2V to V−
Hysteresis Pin Voltage ..... 0V toV−
Output Current 30mA
Operating Temperature
LT685C ..... $-30°C \le T_A \le 85°C$
LT685M ..... $-55°C \le T_A \le 125°C$

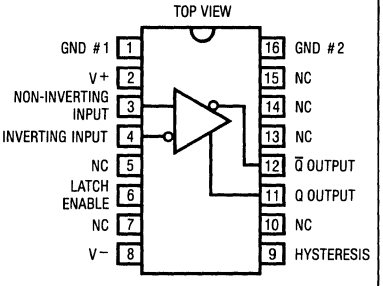
PACKAGE/ORDER INFORMATION



H PACKAGE
TO-5 METAL CAN

ORDER PART NUMBER

LT685CH
LT685MH



J PACKAGE
HERMETIC DIP

N PACKAGE
MOLDED DIP

LT685CJ
LT685CN
LT685MJ

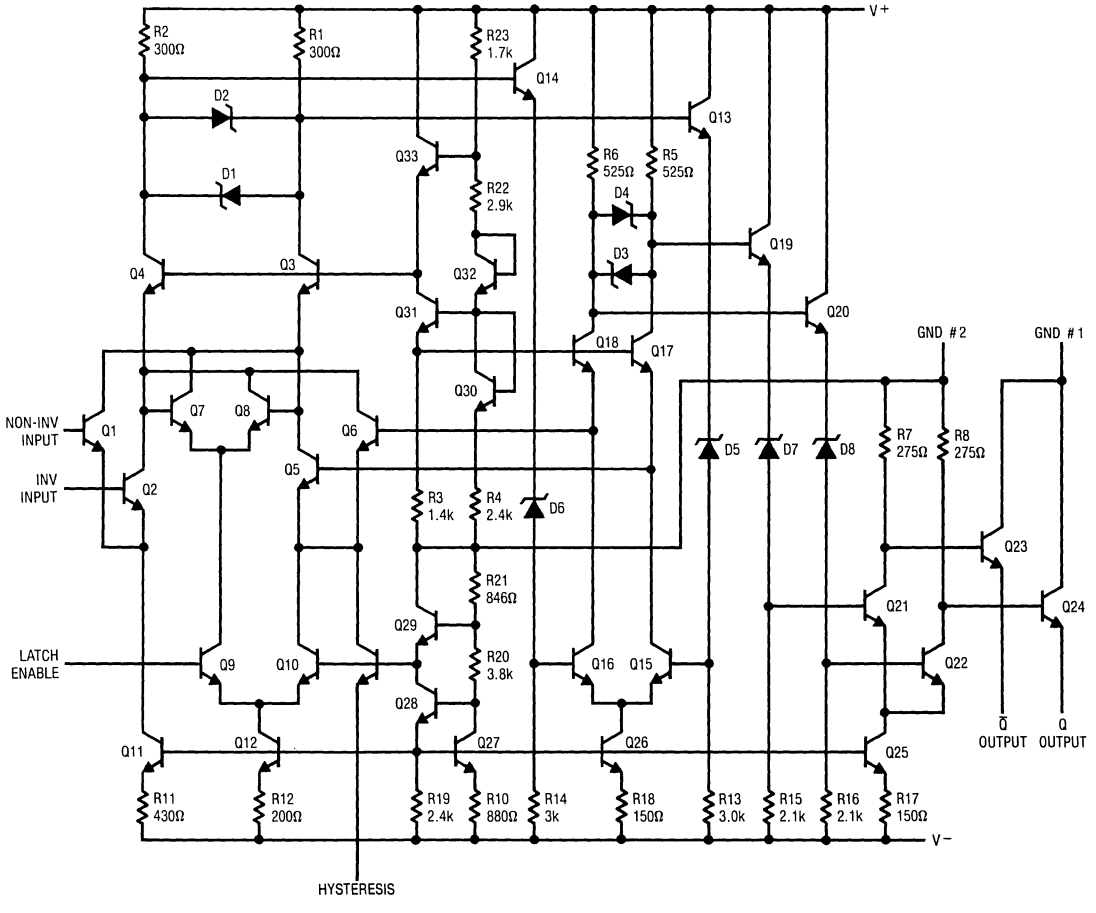
ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	LT685C MIN	LT685C TYP	LT685C MAX	LT685M MIN	LT685M TYP	LT685M MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25°C$		1.0	±2.0 ±2.5		1.0	±2.0 ±3.0	mV mV
dV_{OS}/dT	Input Offset Voltage Drift				±10			±10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$		0.3	±1.0 ±1.3		0.3	±1.0 ±1.6	µA µA
I_B	Input Bias Current	$T_A = 25°C$		5	10 13		5	10 16	µA µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0			6.0			kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$			3.0			3.0	pF
V_{CM}	Input Voltage Range				±3.3			±3.3	V
CMRR	Common-Mode Rejection		80			80			dB
SVRR	Supply Voltage Rejection		70			70			dB
V_{OH}	Output High Voltage	$T_A = 25°C$ $T_A = T_{MIN}$ $T_A = T_{MAX}$	−0.960 −1.060 −0.890		−0.810 −0.890 −0.700	−0.960 −1.100 −0.850		−0.810 −0.920 −0.620	V V V
V_{OL}	Output Low Voltage	$T_A = 25°C$ $T_A = T_{MIN}$ $T_A = T_{MAX}$	−1.850 −1.890 −1.825		−1.650 −1.675 −1.625	−1.850 −1.910 −1.810		−1.650 −1.690 −1.575	V V V
I+	Positive Supply Current				22			22	mA
I−	Negative Supply Current				26			26	mA
P_{DISS}	Power Dissipation				300			300	mW

SWITCHING CHARACTERISTICS (V_{IN} = 100mV step, 5mV overdrive)

SYMBOL	PARAMETER	CONDITIONS	LT685C MIN	LT685C TYP	LT685C MAX	LT685M MIN	LT685M TYP	LT685M MAX	UNITS
t_{PD}	Progagation Delay	$T_{MIN} < T_A < 25°C$	4.5	5.5	6.5	4.5	5.5	6.5	ns
		$T_A = T_{MAX}$	5.0		9.5	5.5		12	ns

SCHEMATIC DIAGRAM



LT1025

Micropower Thermocouple Cold Junction Compensator

FEATURES

- 80μA Supply Current
- 4V to 36V Operation
- 0.5°C Initial Accuracy (A Version)
- Compatible with Standard Thermocouples (E, J, K, R, S, T)
- Auxiliary 10mV/°C Output
- Bow Corrected

APPLICATIONS

- Thermocouple Cold Junction Compensator
- Centigrade Thermometer
- Temperature Compensation Network

DESCRIPTION

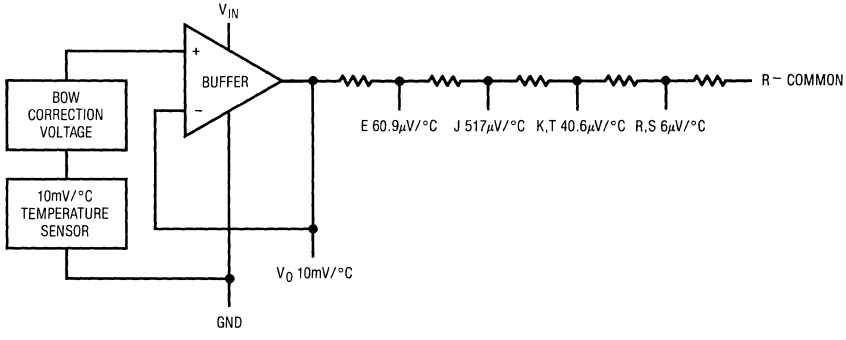
The LT1025 is a micropower thermocouple cold junction compensator for use with type E, J, K, R, S, and T thermocouples. It utilizes wafer level and post-package trimming to achieve 0.5°C initial accuracy. Special curvature correction circuitry is used to match the "bow" found in all thermocouples so that accurate cold junction compensation is maintained over a wider temperature range.

The LT1025 will operate with a supply voltage from 4V to 36V. Typical supply current is 80μA, resulting in less than 0.1°C internal temperature rise for supply voltages under 10V. A 10mV/°C output is available at low impedance, in addition to the direct thermocouple voltages of 60.9μV/°C (E), 51.7μV/°C (J), 40.3μV/°C (K, T) and 5.95μV/°C (R, S). All outputs are essentially independent of power supply voltage.

A special kit is available (LTK001) which contains an LT1025 and a custom tailored thermocouple amplifier. The amplifier and compensator are matched to allow a much tighter specification of temperature error than would be obtained by adding the compensator and amplifier errors on a worst-case basis. The amplifier from this kit is available separately as LTKA001.

The LT1025 is available in an 8 pin plastic miniDIP for temperatures between 0°C and 70°C. A ceramic miniDIP is also available for −55°C to +125°C operation.

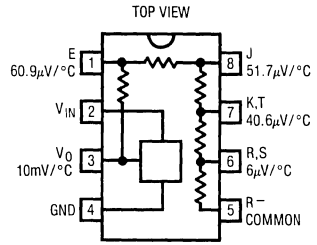
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage 36V
Output Voltage (Forced) 5V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
LT1025AC, LT1025C ..... 0°C to +70°C
LT1025AM, LT1025M ..... −55°C to +125°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1025AMJ8
LT1025MJ8
LT1025ACN8
LT1025CN8

ELECTRICAL CHARACTERISTICS

V_S = 5V, T_A = 25°C, Pin 5 tied to Pin 4, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Temperature Error at 10mV/°C Output (Note 3)	T_J = 25°C					
	LT1025A			0.3	0.5	°C
	LT1025			0.5	2.0	°C
	Full Temperature Span	●		See Curve		
Resistor Divider Accuracy (Notes 1, 3)	V_{OUT} = 10mV/°C					
	LT1025A E		60.6	60.9	61.3	μV/°C
	J		51.4	51.7	52.1	μV/°C
	K, T		40.3	40.6	41.0	μV/°C
	R, S		5.8	5.95	6.2	μV/°C
	LT1025 E		60.4	60.9	61.6	μV/°C
	J		51.2	51.7	52.3	μV/°C
	K, T		40.2	40.6	41.2	μV/°C
	R, S		5.75	5.95	6.3	μV/°C
Supply Current	4V ≤ V_{IN} ≤ 36V		50	80	100	μA
	LT1025AC, LT1025C	●	50		150	μA
	LT1025AM, LT1025M	●			200	μA
Line Regulation (Note 2)	4V ≤ V_{IN} ≤ 36V	●		0.003	0.02	°C/V
Load Regulation (Note 2)	0 ≤ I_O ≤ 1mA	●		0.04	0.2	°C
Divider Impedance	E			2.5		kΩ
	J			2.1		kΩ
	K, T			4.4		kΩ
	R, S			3.8		kΩ
Change in Supply Current	4V ≤ V_{IN} ≤ 36V			0.01	0.05	μA/V

The ● denotes the specifications which apply over the full operating temperature range.

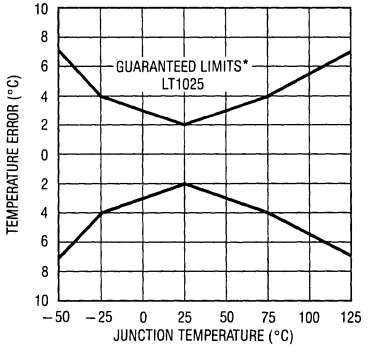
Note 1: Divider accuracy is measured by applying a 10.000V signal to the output divider and measuring the individual outputs.

Note 2: Regulation does not include the effects of self-heating. See "Internal Temperature Rise" in Application Guide.

Note 3: To calculate total temperature error at individual thermocouple outputs, add 10mV/°C output error to the resistor divider error. Total error for type K output at 25°C with an LT1025A is 0.5°C plus (0.4μV/°C) (25°C) / (40.6μV/°C) = 0.5°C + 0.25°C = 0.75°C.

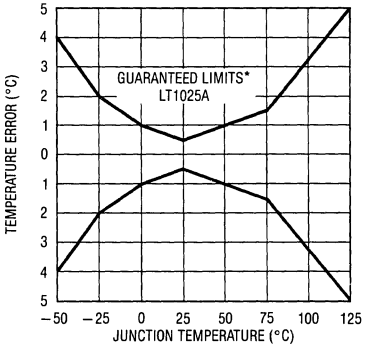
TYPICAL PERFORMANCE CHARACTERISTICS

10mV/°C Output Temperature Error LT1025



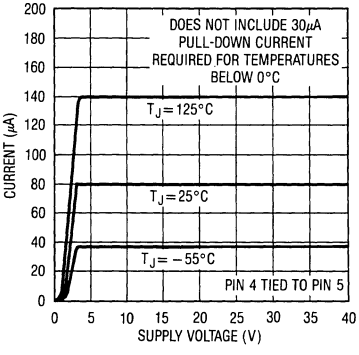
*ERROR CURVE FACTORS IN THE NONLINEARITY TERM BUILT IN TO THE LT1025. SEE THEORY OF OPERATION IN APPLICATION GUIDE SECTION.

10mV/°C Output Temperature Error LT1025A



*ERROR CURVE FACTORS IN THE NONLINEARITY TERM BUILT IN TO THE LT1025. SEE THEORY OF OPERATION IN APPLICATION GUIDE SECTION.

Supply Current



APPLICATION GUIDE

The LT1025 was designed to be extremely easy to use, but the following ideas and suggestions should be helpful in obtaining the best possible performance and versatility from this new cold junction compensator.

Theory of Operation

A thermocouple consists of two dissimilar metals joined together. A voltage (Seebeck EMF) will be generated if the two ends of the thermocouple are at different temperatures. In Figure 1, iron and constantan are joined at the temperature measuring point T1. Two additional thermocouple junctions are formed where the iron and constantan connect to ordinary copper wire. For the purposes of this discussion it is assumed that these two junctions are at the same temperature, T2. The Seebeck voltage, V_S, is the product of the Seebeck coefficient α, and the temperature difference, T1 – T2; $V_S = \alpha(T1 - T2)$. The junctions at T2 are commonly called the cold junction because a common practice is to immerse the T2 junction in 0°C ice/water slurry to make T2 independent of room temperature variations. Thermocouple tables are based on a cold-junction temperature of 0°C.

To date, IC manufacturers efforts to make microminiature thermos bottles have not been totally successful. Therefore, an electronically simulated cold-junction is required for most applications. The idea is basically to add a temperature dependent voltage to V_S such that the voltage sum is the same as if the T2 junction were at a constant 0°C instead of at room temperature. This voltage source is called a cold junction compensator. Its output is designed to be 0V at 0°C and have a slope equal to the Seebeck coefficient over the expected range of T2 temperatures.

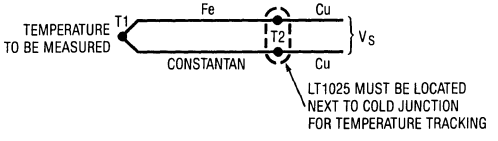


Figure 1

To operate properly, a cold junction compensator must be at exactly the same temperature as the cold junction of the thermocouple (T2). *Therefore, it is important to locate the LT1025 physically close to the cold junction with local temperature gradients minimized.* If this is not possible, an extender made of matching thermocouple wire can be used. This shifts the cold junction from the user termination to the end of the extender so that the LT1025 can be located remotely from the user termination as shown in Figure 2.

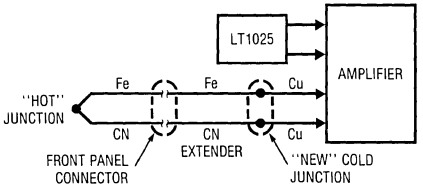


Figure 2

The four thermocouple outputs on the LT1025 are 60.9μV/°C (E), 51.7μV/°C (J), 40.6μV/°C (K and T), and 6μV/°C (R and S). These particular coefficients are chosen to match the room temperature (25°C) slope of the thermocouples. Over wide temperature ranges, however, the slope of thermocouples changes, yielding a quasi-parabolic error compared to a constant slope. The LT1025 outputs have a deliberate parabolic "bow" to help compensate for this effect. The outputs can be mathematically described as the sum of a linear term equal to room temperature slope plus a quadratic term proportional to temperature deviation from 25°C *squared.* The coefficient (β) of the quadratic term is a compromise value chosen to offer improvement in all the outputs.

$$V_{OUT} = \alpha T + \beta(T - 25°)^2$$
$$\beta \approx 5.5 \times 10^{-4}$$

The actual β term which would be required to best compensate each thermocouple type in the temperature range of 0°C to 50°C is: E, 6.6×10^{-4}; J, 4.8×10^{-4}; K, 4.3×10^{-4}; R, 1.9×10^{-3}; S, 1.9×10^{-3}; T, 1×10^{-3}.

The temperature error specification for the LT1025 (shown as a graph) assumes a β of 5.5×10^{-4}. For example, an LT1025 is considered "perfect" if its 10mV/°C output fits the equation $V_O = 10mV(T) + 0.55 \times 10^{-4}(T - 25)^2$.

Operating at Negative Temperatures

The LT1025 is designed to operate with a single positive supply. It therefore cannot deliver proper outputs for temperatures below zero unless an external pull-down resistor is added to the V_O output. This resistor can be connected to any convenient negative supply. It should be selected to sink at least 30μA of current. Suggested value for a −5V supply is 150kΩ, and for a −15V supply, 470kΩ. Smaller resistors must be used if an external load is connected to the 10mV/°C output. The LT1025 can source up to 1mA of current, but there is a trade-off with internal temperature rise.

Internal Temperature Rise

The LT1025 is specified for temperature accuracy assuming no internal temperature rise. At low supply voltages this rise is usually negligible (≃0.05°C@5V), but at higher supply voltages or with external loads or pull-down current, internal rise could become significant. This effect can be calculated from a simple thermal formula, $\Delta T = (\Theta_{JA})(V^+)(I_Q + I_L)$, where Θ_{JA} is thermal resistance from junction to ambient, (≃130°C/W), V^+ is the LT1025 supply voltage, I_Q is the LT1025 supply current (≃80μA), and I_L is the total load current including actual load to ground and any pull-down current needed to generate negative outputs. A sample calculation with a 15V supply and 50μA pull-down current would yield, (130°C/W) (15V) (80 + 50μA) = 0.32°C. This is a significant rise in some applications. It can be reduced by lowering supply voltage (a simple fix is to insert a 10V zener in the V_{IN} lead) or the system can be calibrated and specified after an initial warm-up period of several minutes.

Driving External Capacitance

The direct thermocouple drive pins on the LT1025 (J, K, etc.) can be loaded with as much capacitance as desired, but the 10mV/°C output should not be loaded with more than 50pF unless external pull-down current is added, or a compensation network is used.

Thermocouple Effects in Leads

Thermocouple voltages are generated whenever dissimilar materials are joined. **This includes the leads of IC packages,** which may be kovar in TO-5 cans, alloy 42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is "zero" if all are at exactly the same temperature, but temperature gradients exist within IC packages and across PC boards whenever power is dissipated. For this reason, extreme care must be used to ensure that no temperature gradients exist in the vicinity of the thermocouple terminations, the LT1025, or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be positioned isothermally, especially the LT1025 R^- and appropriate output pins, the amplifier input pins, and the gain setting resistor leads. An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire-bond/lead system of the IC package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification of the amplifier and can occur in amplifiers with measured "zero" drift. Warm-up drift is directly proportional to amplifier power dissipation. It can be minimized by avoiding TO-5 cans, using low supply current amplifiers, and by using the lowest possible supply voltages. Finally, it can be accommodated by calibrating and specifying the system after a five minute warm-up period.

Reversing the Polarity of the 10mV/°C Output

The LT1025 can be made to "stand on its head" to achieve a minus 10mV/°C output point. This is done as shown in Figure 3. The normal output (V_O) is grounded and feedback is established between the ground pin and the positive supply pin by feeding both of them with currents while coupling them with a 6V zener. The ground pin will now be forced by feedback to generate – 10mV/°C *as long as the grounded output is supplying a net "source" current into ground.* This condition is satisfied by selecting R1 such that the current through R1 (I^-) is more than the sum of the LT1025 supply current, the maximum load current (I_L), and the minimum zener current (≈ 50μA). R2 is then selected to supply more current than I^-.

$$R1 = \frac{V^-}{300\mu A + I_L}$$

$$R2 = \frac{V^+ - V_Z(\approx 6V)}{V^-/R1 + 280\mu A}$$

For ± 15V supplies, with I_L = 20μA maximum, R1 = 47k and R2 = 15k.

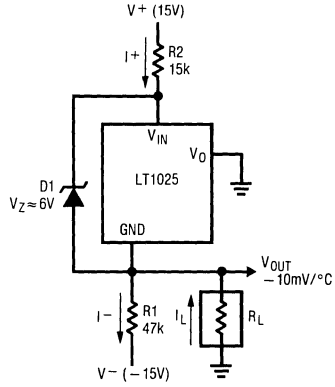


Figure 3

Amplifier Considerations

Thermocouple amplifiers need very low offset voltage and drift, and fairly low bias current if an input filter is used. The best precision bipolar amplifiers should be used for type J, K, E, and T thermocouples which have Seebeck coefficients of 40-60μV/°C. In particularly critical applications or for R and S thermocouples (6-15μV/°C), a chopper-stabilized amplifier is required. Linear Technology offers two amplifiers specifically tailored for thermocouple applications. The LTKA001 is a bipolar design with extremely low offset (<30μV), low drift (<1.5μV/°C), very low bias current (<1nA), and almost negligible warm-up drift (supply current is ≈400μA). It is very cost effective even when compared with "jellybean" op amps with vastly inferior specifications.

For the most demanding applications, the LT1052 CMOS chopper-stabilized amplifier offers 5μV offset and 0.05μV/°C drift (even over the full military temperature range!). Input bias current is 30pA, and gain is typically 30 million. This amplifier should be used for R and S thermocouples, especially if no offset adjustments can be tolerated, or a large ambient temperature swing is expected.

Regardless of amplifier type, it is suggested that for best possible performance, dual-in-line (DIP) packages be used to avoid thermocouple effects in the kovar leads of TO-5 metal can packages if amplifier supply current exceeds 500μA. These leads can generate both DC and AC offset terms in the presence of thermal gradients in the package and/or external air motion.

In many situations, thermocouples are used in high noise environments, and some sort of input filter is required. (See discussion of input filters). To reject 60Hz pick-up with reasonable capacitor values, input resistors in the 10k-100k range are needed. Under these conditions, bias current for the amplifier needs to be less than 1nA to avoid offset and drift effects.

To avoid gain error, high open loop gain is necessary for single-stage thermocouple amplifiers with 10mV/°C or higher outputs. A type K amplifier, for instance, with 100mV/°C output, needs a *closed* loop gain of ≈2,500. An ordinary op amp with a minimum open loop of 50,000 would have an initial gain error of (2,500)/(50,000) = 5%! Although closed loop gain is commonly trimmed, temperature drift of open loop gain will have a very deleterious effect on output accuracy. Minimum suggested open loop gain for type E, J, K, and T thermocouples is 250,000. This gain is adequate for type R and S if output scaling is 10mV/°C or less.

Thermocouple Nonlinearities

Thermocouples are linear over relatively limited temperature spans if accuracies of better than 2°C are needed. The graph in Figure 4 shows thermocouple nonlinearity for the temperature range of 0°C-400°C. Nonlinearities can be dealt with in hardware by using offsets, breakpoints, or power series generators. Software solutions include look-up tables, power series expansions, and piece-wise approximations. For tables and power series coefficients, the reader is referred to the ASTM Publication 470A.

Hardware correction for nonlinearity can be as simple as an offset term. This is shown in Figure 5. The thermocouple shown in the figure has an increasing slope (α) with temperature. The temperature range of interest is between T_L and T_H, with a calibration point at T_M. If a simple amplifier is used and calibrated at T_M, the output will be very high at T_L and very low at T_H. Adding the proper offset term and calibrating at T1/6 or T5/6 can significantly reduce errors. The technique is as follows:

1. Calculate amplifier gain:

$$G = \frac{(SF)(T_H - T_L)}{V_H - V_L}$$

SF = Output scale factor, e.g., 10mV/°C
V_H = Thermocouple output @ T_H
V_L = Thermocouple output @ T_L

2. Use precision resistors to set gain or calibrate gain by introducing a precision "delta" input voltage and trimming for proper "delta" output.

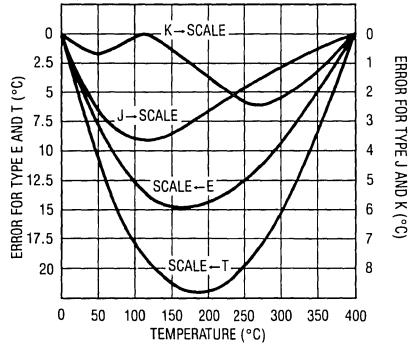


Figure 4. Thermocouple Nonlinearity, 0°C-400°C

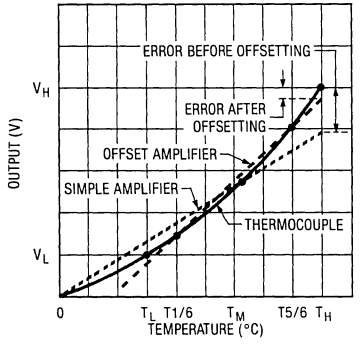


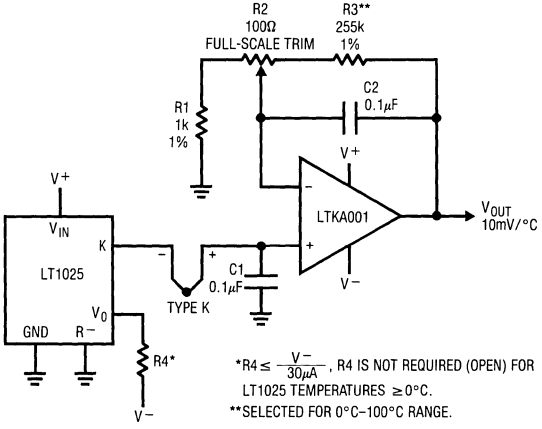
Figure 5. Offset Curve Fitting

3. Calibrate output by adding in a true offset term which does not affect gain (by summing, etc.). Calibration may be done at any temperature either by immersing the thermocouple in a calibrated bath or by substituting a precision input voltage. The method which tends to minimize worst-case error over the whole T_L to T_H range is to calibrate at 1/6 or 5/6 of span. This may be modified if best accuracy is desired at one particular point.

Breakpoint correction for nonlinearity is more complicated than a simple offset, but a single breakpoint combined with offset will reduce errors typically by 4:1 over a simple offset technique. An application note detailing this breakpoint method and power series correction techniques, as well as software methods, will be available shortly.

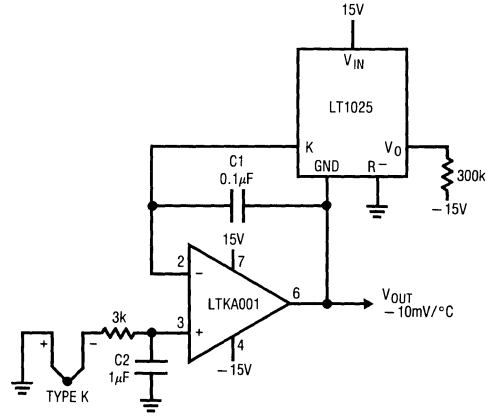
APPLICATION CIRCUITS

Type K 10mV/°C Thermometer

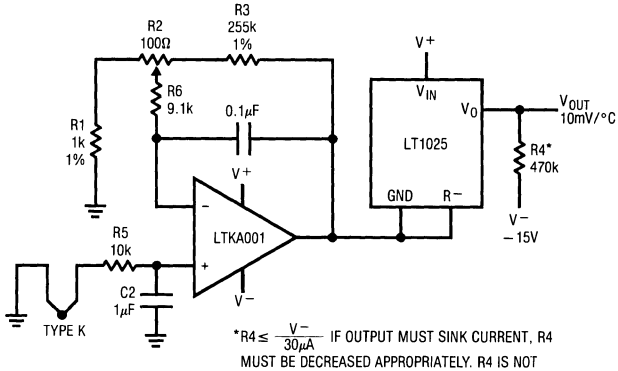


*$R4 \leq \frac{V-}{30\mu A}$, R4 IS NOT REQUIRED (OPEN) FOR LT1025 TEMPERATURES ≥0°C.
**SELECTED FOR 0°C–100°C RANGE.

Eliminating Amplifier Feedback Resistors (Output Goes Negative with Increasing Temperature)

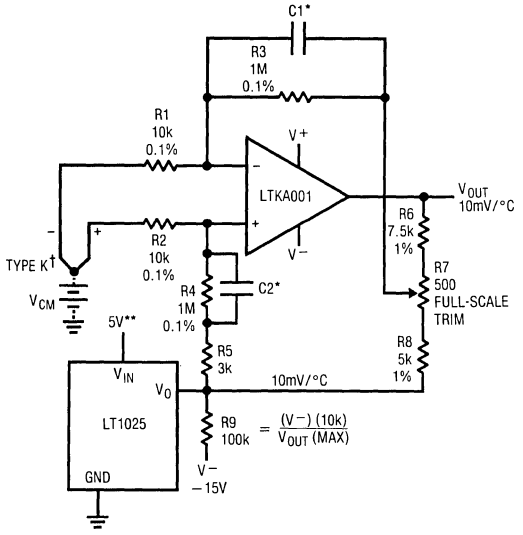


Type K Thermometer with Grounded Thermocouple



*$R4 \leq \frac{V-}{30\mu A}$ IF OUTPUT MUST SINK CURRENT, R4 MUST BE DECREASED APPROPRIATELY. R4 IS NOT REQUIRED (OPEN) FOR LT1025 TEMPERATURES ≥0°C WHEN SOURCING CURRENT ONLY.

Differential Thermocouple Amplifier

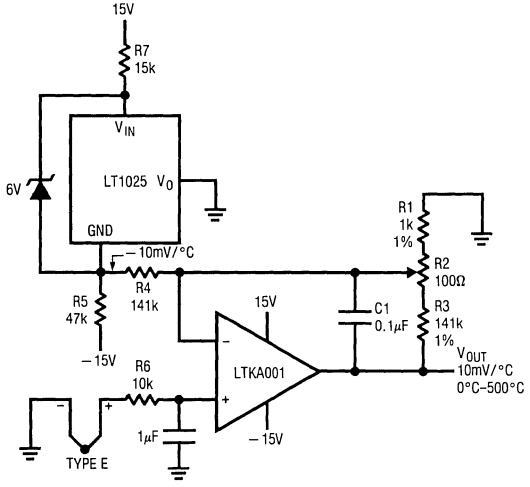


*C1 AND C2 FILTER RIPPLE AND NOISE, BUT WILL LIMIT AC COMMON-MODE REJECTION IF NOT MATCHED. SUGGESTED VALUES ARE 0.001μF TO 0.1μF.

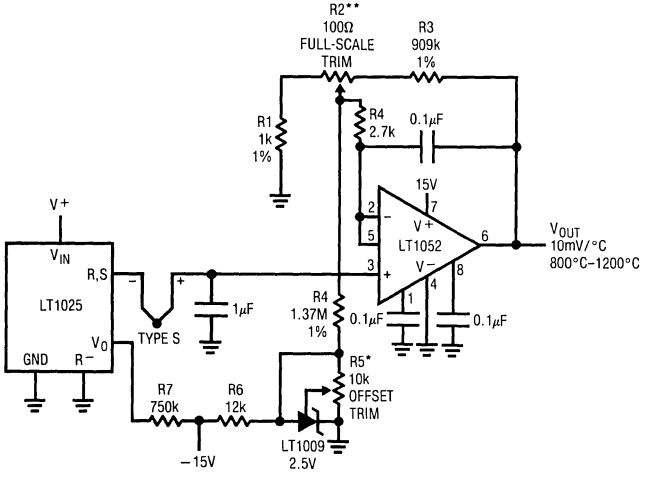
**USE LOWEST POSSIBLE SUPPLY VOLTAGE TO MINIMIZE INTERNAL TEMPERATURE RISE.

†FOR BEST ACCURACY, THERMOCOUPLE RESISTANCE SHOULD BE LESS THAN 100Ω.

Utilizing Negative LT1025 Drive to Accommodate Grounded Thermocouple



Type S Thermocouple Amplifier with Ultra-Low Offset and Drift†

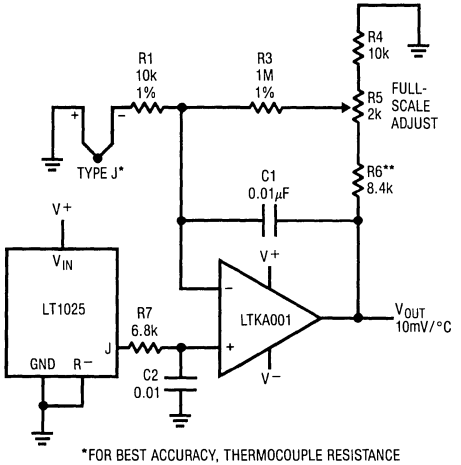


*TRIM R5 FOR V_{OUT} = 1.669V@V_{IN} = 0.000mV (+INPUT OF AMPLIFIER GROUNDED)

**TRIM R2 FOR V_{OUT} = 9.998V@T = 1000°C, OR FOR V_{IN}@ + INPUT OF AMPLIFIER = 9.585mV

†THIS AMPLIFIER HAS A DELIBERATE OFFSET TO ALLOW OUTPUT SLOPE (10mV/°C) TO BE SET INDEPENDENTLY FROM AN ARBITRARY HIGH TEMPERATURE CENTER POINT (1000°C). THIS IS REQUIRED BECAUSE THE SLOPE OF TYPE "S" THERMOCOUPLES VARIES RAPIDLY WITH TEMPERATURE, INCREASING FROM 6μV/°C@25°C TO 11μV/°C@1000°C. NONLINEARITY LIMITS ACCURACY TO ≈3°C OVER THE 800°C TO 1200°C RANGE EVEN WITH OFFSET CORRECTION.

Grounded Thermocouple Amplifier with Positive Output



*FOR BEST ACCURACY, THERMOCOUPLE RESISTANCE SHOULD BE LESS THAN 50Ω.

**SELECTED FOR 0°C TO 200°C RANGE.

PRELIMINARY

LT1026

Dual Output Switched Capacitor Voltage Generator

FEATURES

- 4V to 10V Input
- Up to ±18V Output
- 20mA Output Current
- Only 1μF Capacitors Needed
- 8 Pin miniDIP

APPLICATIONS

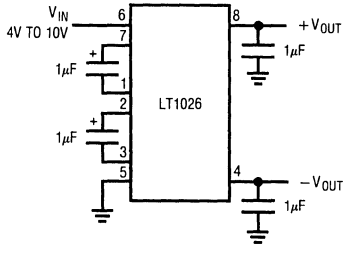
- ± Supply Generator
- RS232 Interface Supply
- Op Amp Supplies

DESCRIPTION

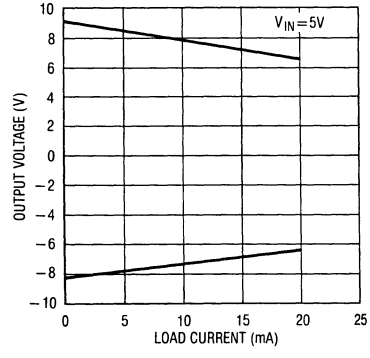
The LT1026 power supply generator converts a single input supply to a dual output of higher voltage. For example, a single 5V supply can be converted to ±9V for op amps. A 9V battery can be converted to ±18V.

Switched capacitors are used, so no inductors are needed. Manufactured using Linear Technology's bipolar process, the LT1026 is an easy, reliable method of generating additional power supply voltages.

TYPICAL APPLICATION



Load Regulation (Both Outputs Loaded)



LT1072

1.25A High Efficiency Switching Regulator

FEATURES

- Wide Input Voltage Range 3V-60V
- Low Quiescent Current—6mA
- Internal 1.25A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages
- Can be Externally Synchronized

APPLICATIONS

- Logic Supply 5V @ 2.5A
- 5V Logic to ±15V Op Amp Supply
- Offline Converter up to 50W
- Battery Upconverter
- Power Inverter (+ to −) or (− to +)
- Fully Floating Multiple Outputs

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1072. Application circuits are included to show the capability of the LT1072. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1072 by factoring in the lower switch current rating.

DESCRIPTION

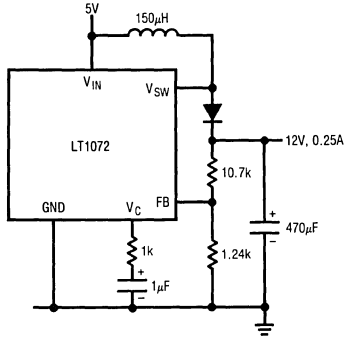
The LT1072 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1072 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1072 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 100 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

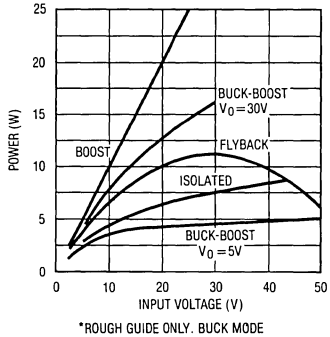
The LT1072 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1072, without the need for optocouplers or extra transformer windings.

TYPICAL APPLICATION

Boost Converter (5V to 12V)



Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 1A \times V_{OUT}$. SPECIAL TOPOLOGIES DELIVER MORE POWER.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1072HV (See Note 1) 60V
- LT1072 (See Note 1) 40V

Switch Output Voltage
- LT1072HV (Note 2) 75V
- LT1072 ..... 65V

Feedback Pin Voltage (Transient, 1ms) ..... ±15V

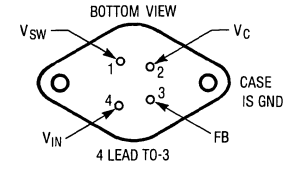
Operating Junction Temperature Range
- LT1072HVM, LT1072M ..... −55°C to +150°C
- LT1072HVC, LT1072C (Oper.) ..... 0°C to +100°C
- LT1072HVC, LT1072C (Sh. Ckt.) ... 0°C to +125°C

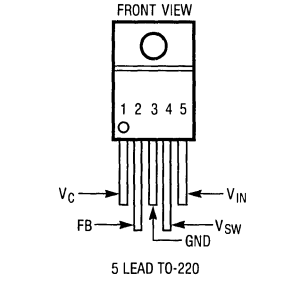
Storage Temperature Range ..... −65°C to +150°C

Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Minimum switch "on" time for the LT1072 in current limit is ≈0.7μsec. This limits the maximum input voltage during short circuit conditions, *in the buck and inverting modes only,* to ≈40V. Normal (unshorted) conditions are not affected.

PACKAGE/ORDER INFORMATION





ORDER PART NUMBER
LT1072HVMK LT1072MK LT1072HVCK LT1072CK
LT1072HVCT LT1072CT

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin	 ●	1.224 1.214	1.244 1.244	1.264 1.274	V
I_B	Feedback Input Current	V_{FB} = V_{REF}	 ●		350	750 1100	nA
gm	Error Amplifier Transconductance	ΔI_C = ±25μA	 ●	3000 2400	4400	6000 7000	μmho
	Error Amplifier Source or Sink Current	V_C = 1.5V	 ●	150 120	200	350 400	μA μA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V Lo Clamp, V_{FB} = 1.5V		1.8 0.25	0.38	2.3 0.52	V V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.7V ≤ V_C ≤ 1.4V		500	800	2000	V/V
	Minimum Input Voltage		●		2.6	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			6	9	mA
	Control Pin Threshold	Duty Cycle = 0	 ●	0.8 0.6	0.9	1.08 1.25	V
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	I_{FB} = 50μA	 ●	15 14	16.3	17.6 18	V
	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 50μA 3V ≤ V_{IN} ≤ V_{MAX}			0.01	0.03	%/V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Flyback Amplifier Transconductance (gm)	ΔI_C = ±10μA		150	300	500	μmho
	Flyback Amplifier Source and Sink Current	V_C = 1.5V Source I_{FB} = 50μA Sink	● ●	15 25	32 40	50 70	μA μA
BV	Output Switch Breakdown Voltage (Note 2)	3V ≤ V_{IN} ≤ V_{MAX} I_{SW} = 5mA	● ●	65 75	90 90		V V
V_{SAT}	Output Switch (Note 1) "On" Resistance	I_{SW} = 1.25A			0.6	1	Ω
	Control Voltage to Switch Current Transconductance				2		A/V
I_{LIM}	Switch Current Limit	Duty Cycle = 50% 50% < Duty Cycle = 80%	● ●	1.25 1		3.5 2.5	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				25	35	mA/A
f	Switching Frequency		 ●	35 33	40	45 47	kHz
DC (max)	Maximum Switch Duty Cycle			90	92	97	%
	Flyback Sense Delay Time				1.5		μs
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ V_{MAX} V_C = 0.05V			100	250	μA
	Shutdown Mode Threshold Voltage	3V ≤ V_{IN} ≤ V_{MAX}	 ●	100 50	150	250 300	mV mV

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

LT1072 OPERATION

The LT1072 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. The switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1072. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1072 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1072 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional trans-

LT1072 OPERATION

former coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1072 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1072 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing. See AN-19 for full application details.

LT1072 Synchronizing

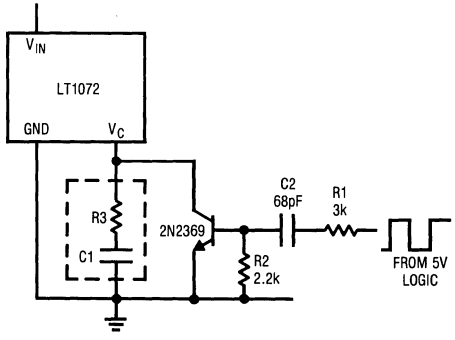
The LT1072 can be externally synchronized in the frequency range of 48kHz to 70kHz. This is accomplished as shown in the accompanying figures. Synchronizing occurs when the V_C pin is pulled to ground with an external transistor. To avoid disturbing the DC characteristics of the internal error amplifier, the width of the synchronizing pulse should be under 0.1μs. C2 sets the pulse width at ≈ 0.35μs. The effect of a synchronizing pulse on the LT1072 amplifier offset can be calculated from:

$$\Delta V_{OS} = \left(\frac{KT}{q}\right)(t_S)(f_S)\left(I_C + \frac{V_C}{R3}\right)/(I_C)$$

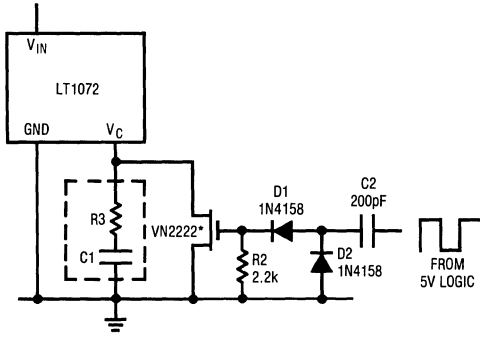
$\frac{KT}{q}$ = 26mV@25°C
t_S = pulse width
f_S = pulse frequency
I_C = LT1072 V_C source current (≈200μA)
V_C = LT1072 operating V_C voltage (1V-2V)
R3 = resistor used to set mid-frequency "zero" in LT1072 frequency compensation network.

With t_S = 0.35μs, f_S = 50kHz, V_C = 1.5V, and R3 = 2KΩ, offset voltage shift is ≈2.2mV. This is not particularly bothersome, but note that high offsets could result if R3 were reduced to a much lower value. Also, the synchronizing transistor must sink higher currents with low values of R3, so larger drives may have to be used. The transistor must be capable of pulling the V_C pin to within 200mV of ground to ensure synchronizing.

Synchronizing with Bipolar Transistor



Synchronizing with MOS Transistor



*SILICONIX OR EQUIVALENT

LT1078/LT1079

Micropower, Dual and Quad, Single Supply, Precision Op Amps

FEATURES

- 38μA Supply Current per Amplifier
- 70μV Max Offset Voltage
- 0.3nA Max Offset Current
- 0.75μVp-p 0.1Hz to 10Hz Voltage Noise
- 7pAp-p 0.1Hz to 10Hz Current Noise
- 0.4μV/°C Offset Voltage Drift
- 200kHz Gain-Bandwidth-Product
- 0.08V/μs Slew Rate
- Single Supply Operation
  - Input Voltage Range Includes Ground
  - Output Swings to Ground while Sinking Current
- Output Sources and Sinks 5mA Load Current

APPLICATIONS

- Battery or Solar Powered Systems
  - Portable Instrumentation
  - Remote Sensor Amplifier
  - Satellite Circuitry
- Micropower Sample and Hold
- Thermocouple Amplifier

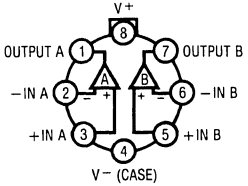
DESCRIPTION

The LT1078 is a micropower dual op amp in the standard 8-pin configuration; the LT1079 is a micropower quad op amp offered in the standard 14-pin packages.

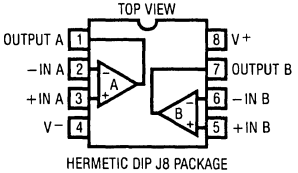
Micropower performance of competing devices is achieved at the expense of seriously degrading precision, noise, speed, and output drive specifications.

The design effort of the LT1078/1079 was concentrated on reducing supply current without sacrificing other parameters. The offset voltage achieved is the lowest on any dual or quad op amp—micropower or otherwise. Offset current, voltage and current noise, slew rate and gain-bandwidth-product are all two to ten times better than on previous micropower op amps.

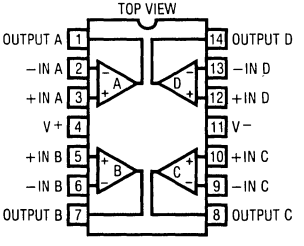
Both the LT1078 and LT1079 can be operated from a single supply (as low as one lithium cell or two Ni-cad batteries). The input range goes below ground. The all-NPN output stage swings to within a few millivolts of ground while sinking current.



METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE



HERMETIC DIP J14 PACKAGE
PLASTIC DIP N14 PACKAGE

PRELIMINARY

LT1083/4/5/6-5
LT1083/4/5/6-12

1.5A, 3A, 5A, 7.5A Low Dropout Positive Fixed Regulators

FEATURES

- Three Terminal Fixed 5V and 12V
- Output Current of 1.5A, 3A, 5A or 7.5A
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.015% Line Regulation
- 0.01% Load Regulation
- 100% Thermal Limit Burn-In

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

DEVICE	OUTPUT CURRENT
LT1083	7.5 Amps
LT1084	5.0 Amps
LT1085	3.0 Amps
LT1086	1.5 Amps

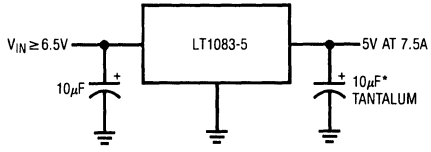
DESCRIPTION

The LT1083 series of positive fixed regulators are designed to provide 1.5A, 3A 5A and 7.5A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

The LT1083 series devices are pin compatible with older 3 terminal regulators. A 10μF output capacitor is required on these new devices; however, this is usually included in most regulator designs.

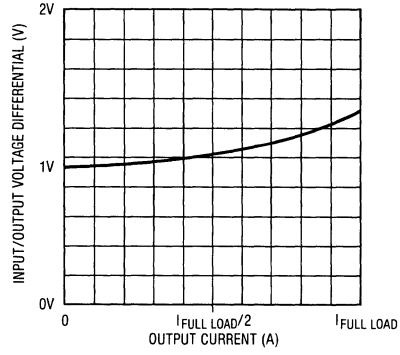
Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1083 quiescent current flows into the load, increasing efficiency.

1.5A, 3A, 5A, 7.5A Regulator



*REQUIRED FOR STABILITY

Dropout Voltage vs Output Current



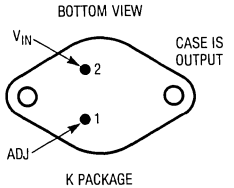
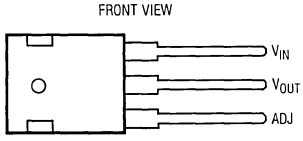
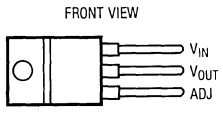
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input Voltage 30V
Operating Junction Temperature Range
"M" Grades
Control Section ..... –55°C to 150°C
Power Transistor ..... –55°C to 200°C
"C" Grades
Control Section..... 0°C to 125°C
Power Transistor..... 0°C to 150°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PRECONDITIONING

100% Thermal Limit Burn-In

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 K PACKAGE TO-3 METAL CAN	LT1083-5MK LT1083-12MK LT1083-5CK LT1083-12CK LT1084-5MK LT1085-5MK LT1086-5MK LT1086-5CK LT1086-12MK LT1086-12CK
 P PACKAGE TO-247 PLASTIC	LT1083-5CP LT1083-12CP LT1084-5CP LT1084-12CP
 T PACKAGE TO-220 PLASTIC	LT1085-5CT LT1085-12CT LT1086-5CT LT1086-12CT

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage						
LT1083/4/5/6-5	I_{OUT} = 0mA, T_j = 25°C, V_{IN} = 8V (K Package Only)		4.950	5.000	5.050	V
	$0 \le I_{OUT} \le I_{FULL\ LOAD}$, $6.5V \le V_{IN} \le 30V$	●	4.900	5.000	5.100	V
LT1083/4/5/6-12	I_{OUT} = 0mA, T_j = 25°C, V_{IN} = 15V (K Package Only)		11.880	12.000	12.120	V
	$0 \le I_{OUT} \le I_{FULL\ LOAD}$, $13.5V \le V_{IN} \le 30V$	●	11.760	12.000	12.240	V
Line Regulation						
LT1083/4/5/6-5	I_{OUT} = 0mA, T_j = 25°C, $6.5V \le V_{IN} \le 20V$			0.5	10	mV
		●		1.0	10	mV
	$6.5V \le V_{IN} \le 30V$	●		2.0	25	mV
LT1083/4/5/6-12	I_{OUT} = 0mA, T_j = 25°C, $13.5V \le V_{IN} \le 25V$			1.0	25	mV
		●		2.0	25	mV
	$13.5V \le V_{IN} \le 30V$	●		4.0	60	mV

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation						
LT1083/4/5/6-5	V_{IN} = 8V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, T_j = 25°C			5	20	mV
		●		10	35	mV
LT1083/4/5/6-12	V_{IN} = 15V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, T_j = 25°C			12	36	mV
		●		24	72	mV
Dropout Voltage						
LT1083/4/5/6-5	ΔV_{OUT} = 50mV, I_{OUT} = $I_{FULL\ LOAD}$	●		6.3	6.5	V
LT1083/4/5/6-12	ΔV_{OUT} = 120mV, I_{OUT} = $I_{FULL\ LOAD}$	●		13.3	13.5	V
Current Limit						
LT1083-5	V_{IN} = 10V		8.0	9.5		A
LT1083-12	V_{IN} = 17V		8.0	9.5		A
LT1084-5	V_{IN} = 10V		5.5	6.5		A
LT1084-12	V_{IN} = 17V		5.5	6.5		A
LT1085-5	V_{IN} = 10V		3.2	4.0		A
LT1085-12	V_{IN} = 17V		3.2	4.0		A
LT1086-5	V_{IN} = 10V		1.6	1.8		A
LT1086-12	V_{IN} = 17V		1.6	1.8		A
Quiescent Current	V_{IN} ≤ 30V			5.0	10.0	mA
Thermal Regulation	T_A = 25°C, 30ms pulse					
LT1083-5/12				0.002	0.01	%/W
LT1084-5/12				0.003	0.015	%/W
LT1085-5/12				0.004	0.02	%/W
LT1086-5/12				0.008	0.04	%/W
Ripple Rejection	f = 120Hz, C_{OUT} = 25μF Tantalum, I_{OUT} = $I_{FULL\ LOAD}$					
LT1083/4/5/6-5	V_{IN} = 8V	●		63		dB
LT1083/4/5/6-12	V_{IN} = 15V	●		55		dB
Temperature Stability		●		0.5		%
Long Term Stability	T_A = 125°C, 1000 Hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.003		%

LT1086

1.5A Low Dropout Positive Adjustable Regulators

FEATURES

- Three Terminal Adjustable
- Output Current of 1.5A
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.015% Line Regulation
- 0.01% Load Regulation
- 100% Thermal Limit Burn-In

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

PRECONDITIONING

100% Thermal Limit Burn-In

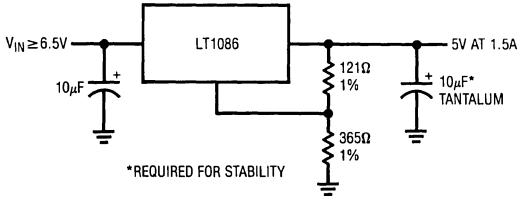
DESCRIPTION

The LT1086 is a positive adjustable regulator designed to provide 1.5A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

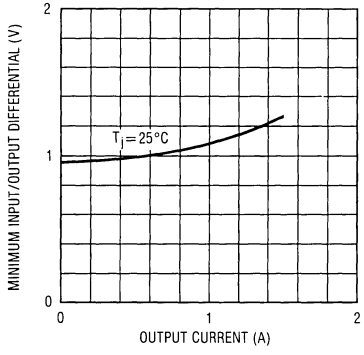
The LT1086 is pin compatible with older 3 terminal regulators. A 10μF output capacitor is required on this new device; however, this is usually included in most regulator designs.

Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1086 quiescent current flows into the load, increasing efficiency.

1.5A Regulator



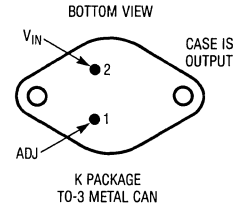
LT1086 Dropout Voltage vs Output Current



ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential
"M" Grades 35V
"C" Grades 30V
Operating Junction Temperature Range
"M" Grades
Control Section ..... –55°C to 150°C
Power Transistor ..... –55°C to 200°C
"C" Grades
Control Section ..... 0°C to 125°C
Power Transistor ..... 0°C to 150°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

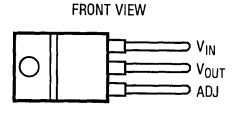
PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN

ORDER PART NUMBER

LT1086MK
LT1086CK



T PACKAGE
TO-220 PLASTIC

LT1086CT

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	I_{OUT} = 10mA, T_j = 25°C, ($V_{IN} - V_{OUT}$) = 3V (K Package Only)		1.238	1.250	1.262	V
	10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 25V (Note 3)	●	1.225	1.250	1.270	V
Line Regulation	I_{LOAD} = 10mA, 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 15V, T_j = 25°C			0.015	0.2	%
		●		0.035	0.2	%
	M Grade 15V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V	●		0.05	0.5	%
	C Grade 15V ≤ ($V_{IN} - V_{OUT}$) ≤ 30V (Notes 1, 2)	●		0.05	0.5	%
Load Regulation	($V_{IN} - V_{OUT}$) = 3V 10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$ T_j = 25°C (Notes 1, 2, 3)			0.1	0.3	%
		●		0.2	0.4	%
Dropout Voltage	$\triangle V_{REF}$ = 1%, I_{OUT} = $I_{FULL\ LOAD}$	●		1.3		V
Current Limit	($V_{IN} - V_{OUT}$) = 5V	●		1.8		A
	($V_{IN} - V_{OUT}$) = 25V	●		0.2		A
Minimum Load Current	($V_{IN} - V_{OUT}$) = 25V	●		5	10	mA
Thermal Regulation	T_A = 25°C, 30ms Pulse			0.010	0.05	%/W
Ripple Rejection	f = 120Hz C_{ADJ} = 25μF, C_{OUT} = 25μF Tantalum I_{OUT} = $I_{FULL\ LOAD}$, ($V_{IN} - V_{OUT}$) = 3V	●	60	75		dB
Adjust Pin Current	T_j = 25°C			55		μA
		●			120	μA
Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$ 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 25V	●		0.2	5	μA
Temperature Stability		●		0.5		%
Long Term Stability	T_A = 125°C, 1000 Hrs.			0.3	1	%
RMS Output Noise (% of V_{OUT})	T_A = 25°C 10Hz = ≤ f ≤ 10kHz			0.003		%

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (15W for the LT1086). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range.

Note 3: $I_{FULL\ LOAD}$ is defined in the current limit curves. $I_{FULL\ LOAD}$ curve is defined as the minimum value of current limit as a function of input to output voltage. Note that the 15W power dissipation for the LT1086 is only achievable over a limited range of input to output voltage.

LT1089

High Side Switch

FEATURES

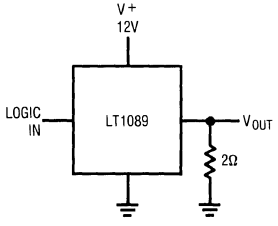
- 7.5A Switch Current Capability
- Low Series Drop (<1.5V@7.5A)
- Logic Input
- 30V Breakdown
- Current Limited
- Thermal Overload Protection
- 5mA Supply Current
- 5μs Rise Time

DESCRIPTION

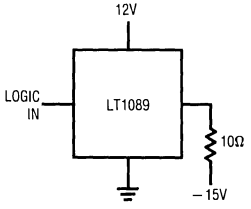
The LT1089 is a logic driven, high current, high side switch utilizing bipolar technology. The device is capable of driving loads up to 7.5A with a low series drop of only 1.5V max. The device has internal current limiting and thermal overload protection. The switch output can drive loads referenced to ground or voltages below ground. The device will be available in both TO-3 metal can and TO-220 plastic package.

APPLICATIONS

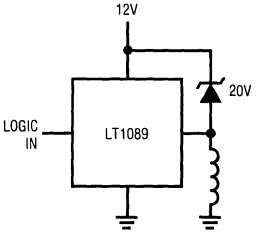
Driving Ground Referred Loads



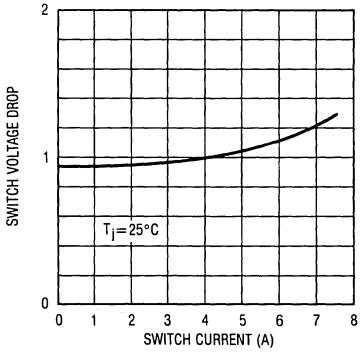
Driving Negative Referred Loads

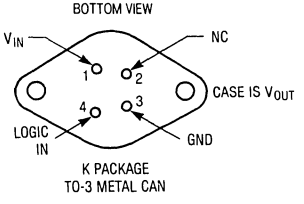


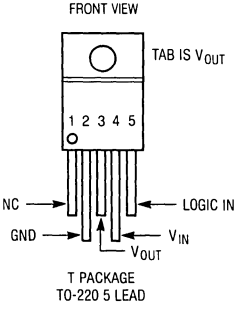
Driving Inductive Loads



Switch Voltage Drop







PRELIMINARY

LTC1092

10-Bit, 8-Pin A/D with Serial Output

FEATURES

- 10-Bit Resolution
- Differential Inputs
- Analog and Rererence Inputs Common-Mode to V_{CC} and GND
- Single Supply (5V or 10V) Operation
- Direct 3 Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- Operates Ratiometrically or with Absolute Reference

KEY SPECIFICATIONS

■ Resolution	10 Bits
■ Total Unadjusted Error (LTC1092A)	± 1/2LSB
■ Fast Conversion Time	20μs
■ Low Supply Current	2.5mA max.
	1mA typ.

DESCRIPTION

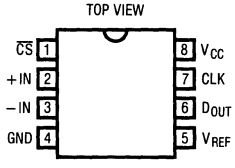
The LTC1092 is a serial output successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform 10-bit conversions on a differential input pair.

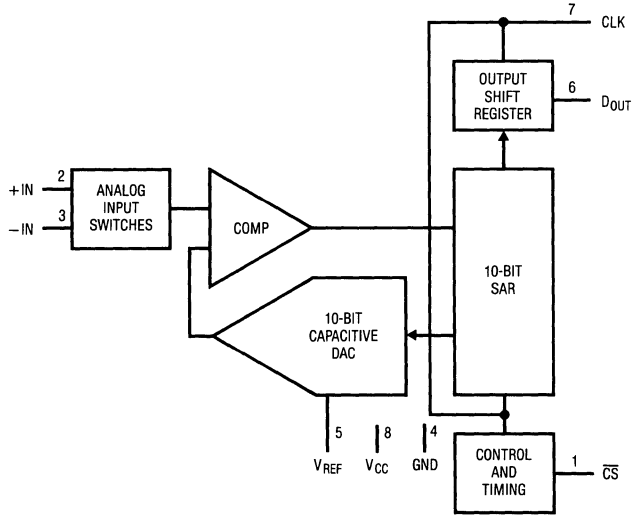
A separate reference pin allows the LTC1092 to be used in reduced span applications.

The serial output is designed to be compatible with industry standard serial interfaces. It provides both MSB or LSB first data. This allows easy interface to shift registers and a variety of processors.

LTCMOS is a trademark of Linear Technology Corp.

CONNECTION AND FUNCTIONAL DIAGRAMS



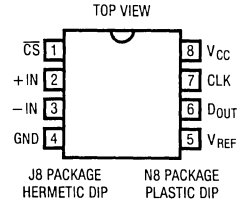


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC} to GND) 12V
Voltage
  Analog, Reference and Digital
    Inputs..... $-0.3V$ to $V_{CC}+0.3V$
  Digital Output ..... $-0.3V$ to $V_{CC}+0.3V$
Power Dissipation..... 500mW
Operating Temperature Range
  LTC1092AC, LTC1092C ..... $-40°C$ to $85°C$
  LTC1092AM, LTC1092M ..... $-55°C$ to $125°C$
Storage Temperature Range..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE HERMETIC DIP

N8 PACKAGE PLASTIC DIP

ORDER PART NUMBER
LTC1092AMJ8 LTC1092MJ8 LTC1092ACJ8 LTC1092CJ8
LTC1092ACN8 LTC1092CN8

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1092A MIN	LTC1092A TYP	LTC1092A MAX	LTC1092 MIN	LTC1092 TYP	LTC1092 MAX	UNITS
Offset Error		●			±0.5			±0.5	LSB
Linearity Error	(Note 4)	●			±0.5			±0.5	LSB
Gain Error		●			±0.5			±2.0	LSB
Total Unadjusted Error	$V_{REF}=5.000V$ (Note 5)	●			±0.5				LSB
Reference Input Resistance				10			10		kΩ
Analog and REF Input Range	(Note 6)			$-0.05V$ to $V_{CC}+0.05V$					V
On Channel Leakage Current (Note 7)	On Channel = 5V Off Channel = 0V	●			±1			±1	μA
	On Channel = 0V Off Channel = 5V	●			±1			±1	μA
Off Channel Leakage Current (Note 7)	On Channel = 5V Off Channel = 0V	●			±1			±1	μA
	On Channel = 0V Off Channel = 5V	●			±1			±1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1092A/LTC1092 MIN	LTC1092A/LTC1092 TYP	LTC1092A/LTC1092 MAX	UNITS
f_{CLK}	Clock Frequency		0.01		0.5	MHz
t_{ACQ}	Analog Input Sample Time	See Operating Sequence		3		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence		10		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence				μs
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	MSB First Data			850	ns
		LSB First Data				ns
t_{dis}	D_{OUT} Output Disable Time				450	ns

AC CHARACTERISTICS (Note 3)

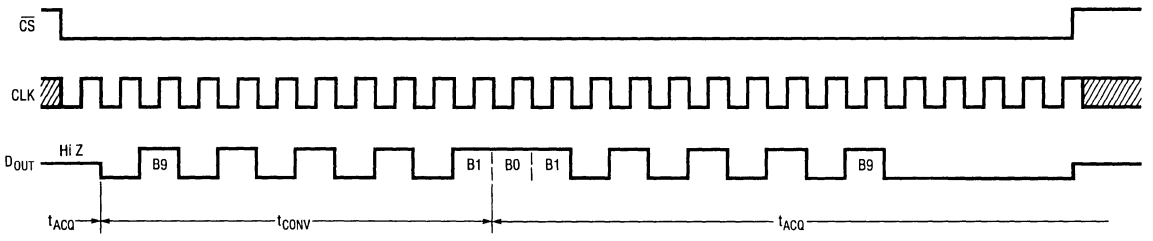
SYMBOL	PARAMETER	CONDITIONS	LTC1092A/ LTC1092 MIN	TYP	MAX	UNITS
t_{en}	D_{OUT} Output Enable Time				450	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓			50		ns
t_f	D_{OUT} Fall Time				300	ns
t_r	D_{OUT} Rise Time				300	ns
$t_{su\overline{CS}}$	Set-up Time, $\overline{CS}$↓ Before First Rising SCLK		1			μs
$t_{wH\overline{CS}}$	$\overline{CS}$ High Time		2			μs
$t_{wL\overline{CS}}$	$\overline{CS}$ Low Time		12			CLK Cycles
C_{IN}	Input Capacitance	Analog Inputs Digital Inputs		60 5		pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1092A/ LTC1092 MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$			2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$			−2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V$, $I_O = -10\mu A$ $I_O = -360\mu A$	4.5 2.4			V V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V$, $I_O = 1.6mA$			0.4	V
I_{OZ}	High Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High			3	μA
		$V_{OUT} = 0V$, $\overline{CS}$ High			−3	μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		10		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High		1.0	2.5	mA
I_{REF}	Reference Current	$V_{REF} = 5V$		0.5	1.0	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note 2: All voltage values are with respect to ground (unless otherwise noted).
Note 3: $V_{CC} = 5V$, $V_{REF} = 5V$, CLK = 0.5MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits $T_A = 25°C$.
Note 4: Linearity error is specified between the actual end points of the A/D transfer curve.
Note 5: Total unadjusted error includes offset, full-scale, linearity, multiplexer and hold step errors.
Note 6: Two on-chip diodes are tied to each reference and anlog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.
Note 7: Channel leakage current is measured with the CLK stopped.

Operating Sequence



FUNCTIONAL DESCRIPTION

Serial Output Data Format

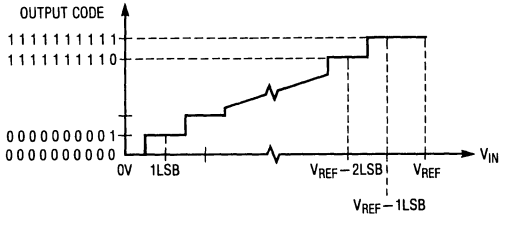
Data transfer is initiated in the LTC1092 by a falling $\overline{CS}$ signal (see Operating Sequence). After $\overline{CS}$ falls, the LTC1092 will wait for one rising and one falling CLK edge. Then the conversion will begin (t_{CONV}). As the conversion runs, one data bit will be clocked out on each falling CLK edge. These bits will be available to be captured on the rising CLK edges by the receiving system. One leading zero will be clocked out first. Following this the MSB first data will be transmitted. LSB first data will follow after the MSB first data is sent.

A/D Input Span

The span of the LTC1092 is defined by the reference voltage applied to the V_{REF} pin. The V_{REF} voltage can be operated at any value within the power supplies. The A/D will convert the difference voltage between the + input (pin 2) and the – input (pin 3). The A/D transfer curve is shown below.

Transfer Curve

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
1111111111	V_{REF} – 1LSB	4.9951V
1111111110	V_{REF} – 2LSB	4.9902V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0049V
0000000000	0V	0V



PRELIMINARY

LTC1099

High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold

FEATURES

- Built-In Sample-and-Hold
- No Missing Codes
- No User Trims Required
- All Timing Inputs Edge Sensitive for Easy Processor Interface
- Fast Conversion Time: 2.5μs Max.
- Latched Three-State Outputs
- Single 5V Operation
- No External Clock
- Overflow Output Allows Cascading
- T_C Input Allows User Adjustable Conversion Time
- 0.3″ Wide 20-Pin DIP

KEY SPECIFICATIONS

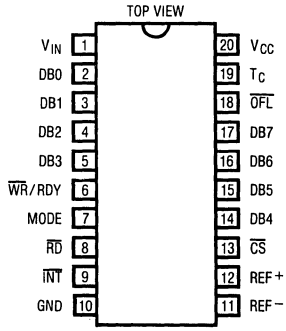
■ Resolution	8 Bits
■ Conversion Time	2.5μs (RD Mode) 2.5μs (WR-RD Mode)
■ Slew Rate Limit (Internal S/H)	5V/μs
■ Low Power	75mW Max
■ Total Unadjusted Error	±1/2 and ±1LSB

DESCRIPTION

The LTC1099 is a high speed, microprocessor compatible, 8-bit analog-to-digital converter (A/D). An internal sample-and-hold (S/H) allows the A/D to convert inputs up to the full Nyquist limit. With a conversion rate of 2.5μs, this allows 200kHz 5Vp-p input signals, or slew rates as high as 5V/μs, to be digitized without the need for an external S/H.

Two modes of operation, READ (RD) mode and WRITE-READ (WR-RD) mode, allow easy interface with processors. All timing is internal and edge sensitive which eliminates the need for external pulse shaping circuits. The Stand-Alone (SA) mode is convenient for those applications not involving a processor.

Digital data outputs are latched with three-state control to allow easy interface to a processor data bus or I/O port. An overflow output (OFL) is provided to allow cascading for higher resolution.



Pin #	Name	Description
1	V_{IN}	Analog input voltage.
2-5	DB0-DB3	Data outputs DB0 = LSB.
6	$\overline{WR}$/RDY	WR starts conversion when mode = V_{CC}. Ready out when mode = GND.
7	MODE	WR-RD mode when = V_{CC}. RD mode when = GND.
8	$\overline{RD}$	Read strobe—activates three-state outputs. Starts conversion in RD mode.
9	$\overline{INT}$	Goes low when conversion is complete. Goes high after data is read.
10	GND	Ground connection.
11	REF^-	Low reference potential (analog GND).
12	REF^+	High reference potential $V_{REF} = (REF^+) - (REF^-)$.
13	$\overline{CS}$	Chip select.
14-17	DB4-DB7	Data outputs DB7 = MSB.
18	$\overline{OFL}$	Overflow—goes high when $V_{IN} > V_{REF}$.
19	T_C	User adjustable conversion time.
20	V_{CC}	Positive supply connection.

Extended Temperature Range Linear ICs (200°C)

Linear Technology now offers a number of its high performance products fully characterized, tested, and with specification limits guaranteed over an extended operating temperature range of from −55°C to +200°C.

The list of extended temperature range products being offered by Linear Technology continues to grow. At the time this catalog was printed, the company offered for sale the following products.

Op Amps:
- LT1001XH Precision Op Amp
- LT1007XH Low Noise, High Speed Precision Op Amp
- LM101AXH Uncompensated General Purpose Op Amp
- LM118XH High Slew Rate Op Amp

Precision References:
- LM129XH 6.9V Precision Voltage Reference

Comparators:
- LM111XH General Purpose Comparator
- LM119XH High Speed Dual Comparator

Complete specifications on Linear Technology's 200°C product offerings can be obtained from your local LTC sales representative or directly from the factory.

SECTION 11— SURFACE MOUNT PRODUCTS

SECTION 11—SURFACE MOUNT PRODUCTS

Introduction

Linear Technology Corporation was founded in 1981 to address the growing demand for high performance and superior quality linear integrated circuits.

Today, Linear Technology has successfully established a leadership position by introducing and supplying leading edge products in each of the industry's basic functional groups—op amps, comparators, voltage regulators, references, switched-capacitor filters, interface, data conversion, and a variety of special function CMOS devices, in all major package styles.

Early on, Linear Technology made the commitment to provide advanced technology, *surface mount packaging*. This makes Linear Technology the first company to offer true precision and high performance linear devices across the full range of functional categories, plus many of the popular second-source devices in JEDEC Standard SO-8, 14, 16 and SOL-16, 18 and 20 pin packages.

Support for Linear Technology's surface mount devices includes service for tape and reel, anti-static rails, quality and reliability data, and datasheets on each product.

Linear Technology intends to address customer demand for surface mount devices where technology and die sizes permit, making the combination of small package size and high performance linear devices readily available to our users.

This section contains information summarizing Linear Technology's capabilities and services for surface mount packaged products, as well as specific device datasheets.

Package Descriptions

Linear Technology's SO packages conform to Standard JEDEC SOIC outlines. Figure 1 represents the 8, 14 and 16-lead narrow (150 mil width) SO packages. The 300 mil width large cavity SOL package is pictured in Figure 2.

In some instances, an LTC product available in an 8-pin standard DIP package is offered in a 16-pin SOL package. This covers the situation where the die is too large to be accommodated by the smaller SO-8 package. Although it is preferable for an SO-8 device to have the same pin-out as the standard 8-pin dual-in-line version, some devices necessitate a rotation of the die to fit in the SO-8 package. Please refer to the applicable SO device datasheet, or consult with the factory to verify exact pinouts for each device.

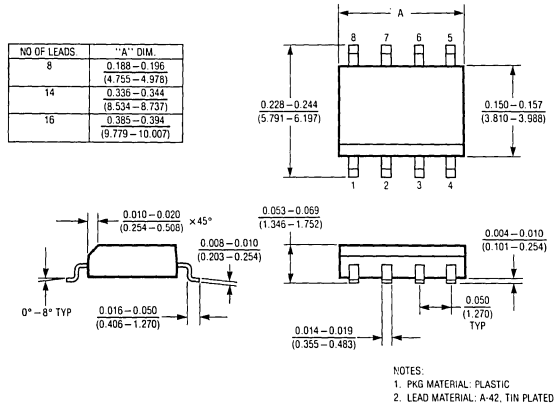


Figure 1

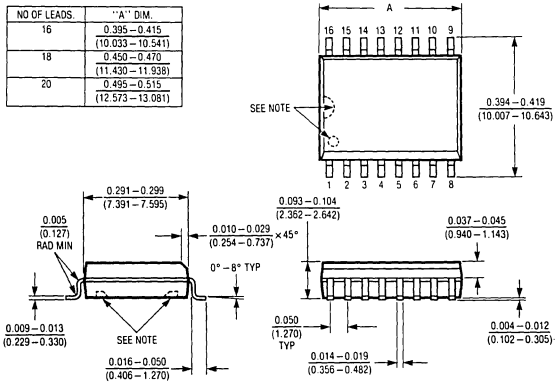


Figure 2

Electrical Specifications

Wherever possible, electrical specifications for an SO device are the same as the plastic molded equivalent. Exceptions to this are identified by the omission of the standard product electrical grade designator from the part number. For example:

—LT1013DS8 has the same electrical specifications as LT1013DN8, since the "D" is common to both product numbers.

—LT1012S8 has one or more different electrical specifications than LT1012CN8, as the "C" is missing from this product designator suffix.

Please consult the appropriate SO package datasheet for complete electrical specifications.

Marking

Because of the limited space available for part marking on some SO packages, abbreviated marking codes are used to identify the device. These codes, if used, are identified in the individual SO package datasheets.

Lead Finish and Solderability

Lead finish is electroplated, matte-tin, with a low carbon content. Solderability meets the requirements of MIL-STD-883C, Method 2003. Recommended solder pads are given in Figure 3.

Wave and Reflow Soldering

Following are the recommended procedures for soldering surface mount packages to PC boards.

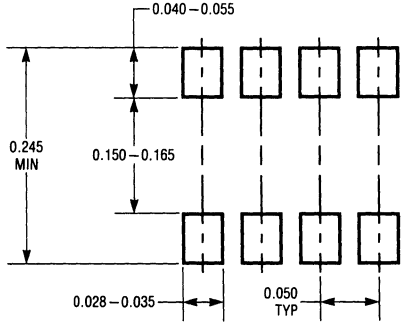
1. Wave Soldering

- Use solder plating boards.
- Dispense adhesive to hold components on board.
- Place components on board.
- Cure adhesive per adhesive manufacturer's specification.
- Foam flux using RMA (Rosin Mildly Activating) flux or an organic acid flux if more aggressive flux is required.
- *• Wave solder using a dual wave soldering system at 240°C to 260°C for 2 seconds per wave.
- Clean board.

*Note: LTC packages will survive temperatures of 260°C for 10 seconds.

Recommended Solder Pads

SO-8, SO-14, SO-16



SOL-16, SOL-18, SOL-20

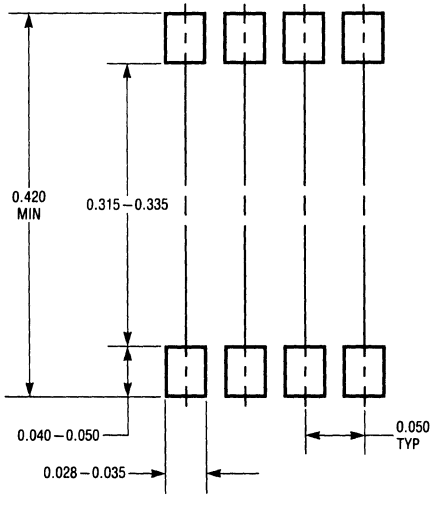


Figure 3. Wave and Reflow Soldering

2. Reflow Soldering

- Use solder plating boards.
- Screen solder paste on board.
- Mount components on board.
- Bake for 15-20 minutes at 65°C-90°C.
- Reflow solder paste. The solder paste temperature must be 200°C for at least 30 seconds. LTC recommends vapor phase or infra red reflow systems for best performance.
- Clean boards.

Thermal Information

Table 1 shows the range of junction-to-ambient thermal resistance of devices mounted on a PCB of FR4 material with copper traces, in still air at 25°C. θ_{JA} with a ceramic substrate is about 70% of the FR4 value. Maximum power dissipation may be calculated by the following formula:

$$P_{D\,MAX}[TA] = \frac{T_{j\,MAX} - T_A}{\theta_{JA}}$$

where $T_{j\,MAX}$ = Maximum operating junction temperature.
T_A = Desired ambient operating temperature.
θ_{JA} = Junction to ambient thermal resistance.

SO-8	150 to 200°C/W	SOL-16	85 to 100°C/W
SO-14	100 to 140°C/W	SOL-18	70 to 100°C/W
SO-16	90 to 130°C/W	SOL-20	70 to 90°C/W

Conditions: PCB mount on FR4 material, still air at 25°C, copper trace.

Table 1. Typical Thermal Resistance Values

Product Reliability

Linear Technology Corporation publishes a reliability data pak on a quarterly basis for our complete range of hermetic and plastic devices. The data generated on the SO-8 compares favorably with that generated for dual-in-line packages. The tests that are run to assess package and device reliability are high temperature operating life with electrical bias, temperature and humidity under bias (85/85), autoclave, temperature cycle, and thermal shock. A sample of the data for the S8 (SO-8 small outline plastic DIP) is shown below.

S8 (8 Lead Small Outline Plastic DIP)
Reliability Data • October 1986

• Operating Life

DEVICE TYPE	SS	# DEVICE HOURS AT 150°C	# DEVICE HOURS AT 125°C[1]	# DEVICE HOURS AT 55°C[1]	# FAILURES
OP07	200	211.8K	1186.1K	591.9KK	0
LT385-1.2	40	41.9K	234.7K	117.1KK	0
LT1012	46	29.4K	164.6K	82.1KK	0
LTC1044/7660	59	47.4K	265.6K	132.5KK	0
LT1021	45	23.4K	131.0K	65.4KK	0
	390	353.9K	1982.0K	989.0KK	0[4]

• 85/85 With Bias

DEVICE TYPE	SS	TOTAL DEVICE HOURS	# FAILURES
OP07	153	234.3K	0
LTC1044C	78	114.2K	0
		348.5K	0

• Autoclave

DEVICE TYPE	SS	TOTAL DEVICE HOURS	# FAILURES
OP07	304	260.4K	0
LTC1044C	103	161.8K	1[3]
LM385B-1.2	85	129.6K	0
LT1012	148	38.0K	1
		589.8K	2

• Temperature Cycle (Air to Air) – 65°C to 150°C

DEVICE TYPE	SS	TOTAL DEVICE CYCLES	# FAILURES
OP07	155	465.0K	0
LTC1044C	96	192.0K	0
		657.0K	0

• Thermal Shock (Liquid to Liquid) – 65°C to 150°C

DEVICE TYPE	SS	TOTAL DEVICE CYCLES	# FAILURES
OP07	156	312.0K	0
LTC1044C	96	91.7K	0
		403.7K	0

Note 1: Assumes $E_a = 1.0eV$.
Note 2: 1 Fit = 1 failure in 10^9 device hours.
Note 3: Non-functional—Bonding pad corrosion.
Note 4: Failure rate at 55°C 1.2 fits[2] to a 60% confidence level.

More current data, by device type, may be obtained by contacting Linear Technology Corporation, Marketing Department.

Tape and Reel Packing

Tape and reel packing is available for all SO and SOL packages (except 18-lead) in accordance with EIA Specification 481-A. Table 2 lists the applicable tape widths, dimensions, and quantities for all LTC small-outline products. Consult factory for tape and reel pricing and minimum order requirements.

PACKAGE	TAPE SIZE	COMPONENT PITCH	HOLE PITCH	REEL DIAMETER	PARTS PER REEL
SO-8	12mm	8mm	4mm	13″	2500
SO-14	16mm	8mm	4mm	13″	2500
SO-16	16mm	8mm	4mm	13″	2500
SOL-16	16mm	12mm	4mm	13″	1000
SOL-18*	—	—	—	—	—
SOL-20	24mm	12mm	4mm	13″	1000

*Unavailable at this time.

Table 2. Tape and Reel Packing Specifications

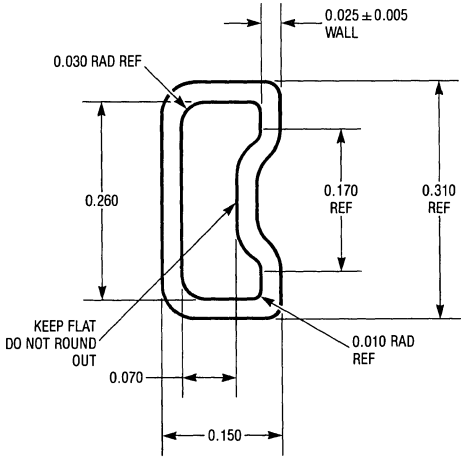
Plastic Tube Packing

Linear Technology SO and SOL packaged devices are packed in conductive plastic tubes with the dimensions indicated in Figure 4. Unit quantities per tube are as listed in Table 3.

SO-8	100 ea.	SOL-16	50 ea.
SO-14	60 ea.	SOL-18	40 ea.
SO-16	50 ea.	SOL-20	40 ea.

Table 3. Devices Per Tube

SO Package Shipping Tube



SOL Package Shipping Tube

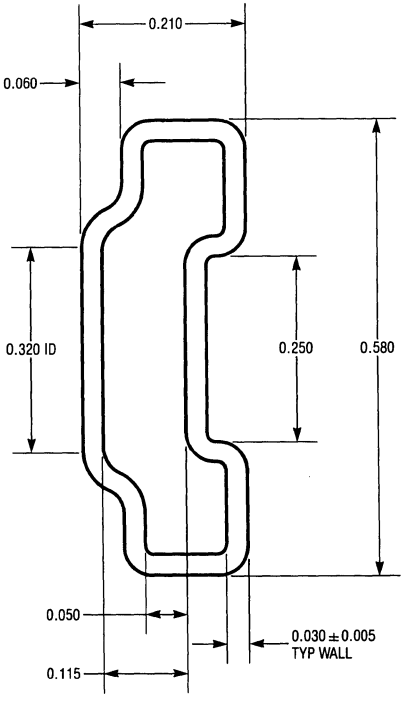


Figure 4

Precision Sample and Hold Amplifier

FEATURES

- 4μs Typical Acquisition Time
- *Guaranteed* 0.01% Max. Gain Error
- 2mV Typ. Offset Voltage
- 2.5mV Max. Hold Step
- Very Low Feedthrough 80dB Min.
- High Input Impedance Under All Conditions
- Logic Inputs Compatible with All Logic Families

APPLICATIONS

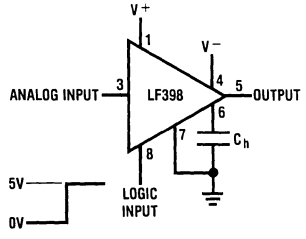
- 12-Bit Data Acquisition Systems
- Ramp Generators
- Analog Switches
- Staircase Generators
- Sample and Difference Circuits

DESCRIPTION

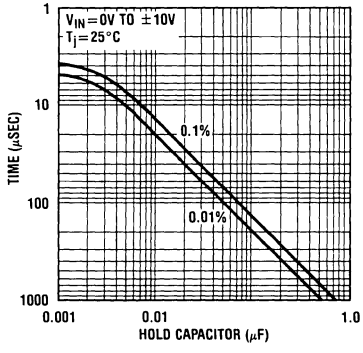
The LF398 is a precision sample and hold amplifier which uses a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. A typical offset voltage of 2mV and gain error of 0.004% allow this sample and hold amplifier to be used in 12-bit systems. Dynamic performance can be optimized by proper selection of the external hold capacitor. Acquisition times can be as low as 4μs for small capacitors while hold step and droop errors can be held below 0.1mV and 30μV/sec respectively when using larger capacitors.

The LF398 is fixed at unity gain with $10^{10}\Omega$ input impedance independent of sample/hold mode. The logic inputs are high impedence differential to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The device will operate over a wide supply voltage range from ±5V to ±18V with very little change in performance, and key parameters are specified over this full supply range.

Basic Sample and Hold



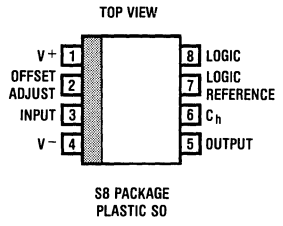
Acquisition Time



ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... Equal to Supply Voltage
Logic to Logic Reference Differential
Voltage (Note 2) ..... +30V, −30V
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration ..... 10 sec
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Supply Voltage ..... ±18V
Power Dissipation (Package Limitation)
(Note 1) 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LF398S8
PART MARKING
398

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF398 MIN	LF398 TYP	LF398 MAX	UNITS
Input Offset Voltage (Note 6)				2	7	mV
		●			10	mV
Input Bias Current (Note 6)				10	50	nA
		●			100	nA
Input Impedance				10^{10}		Ω
Gain Error	$R_L = 10k$			0.004	0.01	%
		●			0.02	%
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$		80	96		dB
Output Impedance	"HOLD" Mode			0.5	4	Ω
		●			6	Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F$, $V_{OUT} = 0$			0.5	2.5	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	6.5	mA
Logic and Logic Reference Input Current				2	10	μA
Leakage Current Into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			30	200	pA
Acquisition Time to 0.1%	$\triangle V_{OUT} = 10V$, $C_h = 1000pF$			4		μs
	$C_h = 0.01\mu F$			16		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		80	110		dB
Differential Logic Threshold			0.8	1.4	2.4	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: T_j max for the LF398S8 is 100°C.

Note 2: The logic inputs are protected to ±30V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both logic and logic reference pins must be at least 2V below the positive supply and one of these pins must be at least 3V above the negative supply.

Note 3: Unless otherwise noted, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq = +11.5V$, $C_h = 0.01\mu F$, $R_L = 10k\Omega$ and unit is in "sample" mode. Logic reference = 0V and logic voltage = 2.5V.

Note 4: The hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters are guaranteed over a supply voltage range of ±5V to ±18V.

High Speed Operational Amplifier

FEATURES

- 4mV Typ. Input Offset Voltage
- *Guaranteed* 25,000 Min. Gain
- *Guaranteed* 50V/μs Slew Rate
- 30nA Typ. Input Offset Current
- 15MHz Bandwidth
- Unity Gain Stable

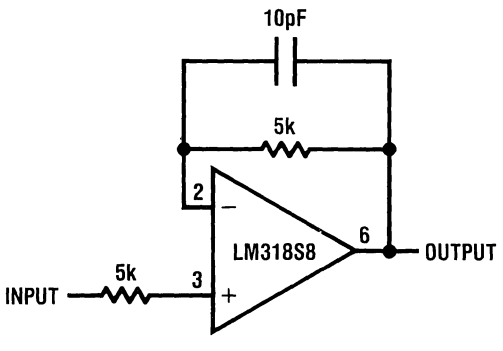
APPLICATIONS

- Wideband Amplifiers
- High Frequency Absolute Value Circuits
- D/A Converter Amplifiers
- Fast Integrators

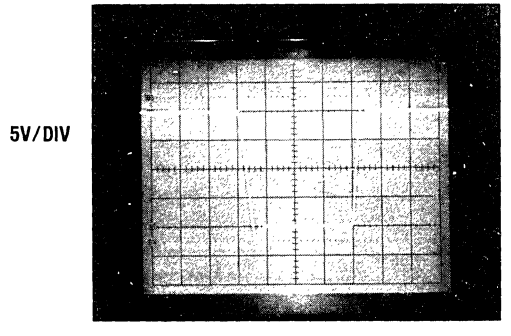
DESCRIPTION

The LM318 is a high speed, unity gain stable operational amplifier designed for applications requiring high slew rate and wide bandwidth. Although the device is internally compensated for unity gain operation, external compensation can be added for increased stability in reduced bandwidth applications. With a single capacitor, the 0.1% settling time is reduced to under 1μs. Feedforward compensation can be used in inverting applications to increase slew rate to over 150V/μs and almost double the bandwidth.

Voltage Follower



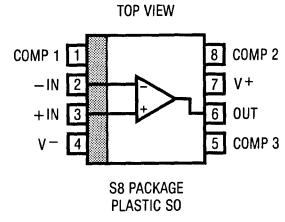
Voltage Follower Pulse Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LM318S8
PART MARKING
318

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LM318 MIN	LM318 TYP	LM318 MAX	UNITS
V_{OS}	Input Offset Voltage				4	10	mV
			●			15	mV
I_{OS}	Input Offset Current				30	200	nA
			●			300	nA
I_B	Input Bias Current				150	500	nA
			●			750	nA
R_{IN}	Input Resistance			0.5	3		MΩ
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$		25	200		V/mV
			●	20			V/mV
SR	Slew Rate	$V_S = \pm 15V$, $A_V = 1$		50	70		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$			15		MHz
	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$	●	±12	±13		V
	Input Voltage Range	$V_S = \pm 15V$	●	±11.5			V
I_S	Supply Current				5	10	mA
CMRR	Common-Mode Rejection Ratio		●	70	100		dB
PSRR	Power Supply Rejection Ratio		●	65	80		dB

The ● denotes those specifications which apply over the full operating temperature range.

Note 1: The inputs are shunted with back-to-back zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$. The power supplies must be bypassed with a 0.1μF or greater disc capacitor within 4 inches of the device.

Constant Current Source and Temperature Sensor

FEATURES

- 1μA to 10mA Operation
- 0.02%/V Regulation
- 0.8V to 30V Operating Voltage
- Can Be Used as Linear Temperature Sensor
- Draws No Reverse Current

APPLICATIONS

- Current Mode Temperature Sensing
- Constant Current Source for Shunt References
- Cold Junction Compensation
- Constant-Gain Bias for Bipolar Differential Stage
- Micropower Bias Networks
- Buffer for Photoconductive Cell
- Current Limiter

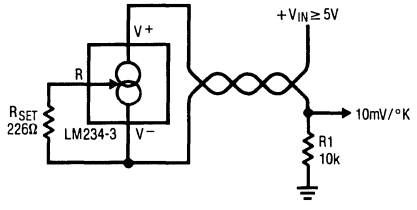
DESCRIPTION

The LM334 is a three-terminal current source designed to operate at current levels from 1μA to 10mA, as set by an external resistor. The device operates as a true two-terminal current source, requiring no extra power connections or input signals. Regulation is typically 0.02%/V and terminal-to-terminal voltage can range from 800mV to 30V.

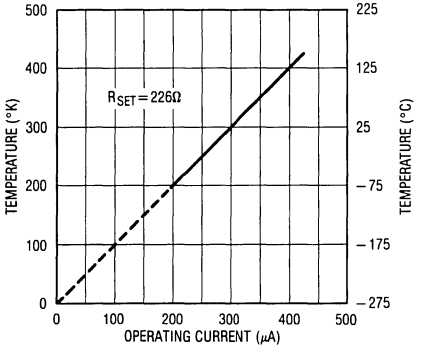
Because the operating current is *directly proportional to absolute temperature* in degrees Kelvin, the device will also find wide applications as a temperature sensor. The temperature dependence of the operating current is +0.336%/°C at room temperature. For example, a device operating at 298μA will have a temperature coefficient of +1μA/°C. The temperature dependence is extremely accurate and repeatable.

If a zero temperature coefficient current source is required, this is easily achieved by adding a diode and a resistor.

Remote Temperature Sensor with Voltage Output



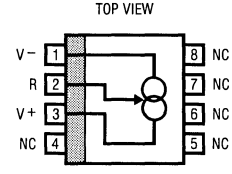
Operating Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

V^+ to V^- Forward Voltage 30V
V^+ to V^- Reverse Voltage 20V
R Pin to V^- Voltage 5V
Set Current 10mA
Power Dissipation 200mW
Operating Temperature Range ..... 0°C to 70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LM334S8
PART MARKING
334

ELECTRICAL CHARACTERISTICS CURRENT SOURCE (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM334 MIN	LM334 TYP	LM334 MAX	UNITS
ΔI_{SET}	Set Current Error, $V^+ = 2.5V$ (Note 2)	$10\mu A \le I_{SET} \le 1mA$			6	%
		$1mA < I_{SET} \le 5mA$			8	%
		$2\mu A \le I_{SET} < 10\mu A$			12	%
	Ratio of Set Current to V^- Current	$10\mu A \le I_{SET} \le 1mA$	14	18	26	
		$1mA \le I_{SET} \le 5mA$		14		
		$2\mu A \le I_{SET} \le 10\mu A$		18	26	
V_{MIN}	Minimum Operating Voltage	$2\mu A \le I_{SET} \le 100\mu A$		0.8		V
		$100\mu A < I_{SET} \le 1mA$		0.9		V
		$1mA < I_{SET} \le 5mA$		1.0		V
$\frac{\Delta I_{SET}}{\Delta V_{IN}}$	Average Change in Set Current with Input Voltage	$1.5V \le V^+ \le 5V$ $2\mu A \le I_{SET} \le 1mA$		0.02	0.1	%/V
		$5V \le V^+ \le 30V$		0.01	0.05	%/V
		$1.5V \le V \le 5V$ $1mA < I_{SET} \le 5mA$		0.03		%/V
		$5V \le V \le 30V$		0.02		%/V
	Temperature Dependence of Set Current (Note 3)	$25\mu A \le I_{SET} \le 1mA$	0.96T	T	1.04T	
C_S	Effective Shunt Capacitance			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25°C$ with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V^+ pin. It is determined by the following formula: $I_{SET} = 67.7mV/R_{SET}$ (@25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C@$T_j = 25°C$.

Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_O (T/T_O)$ where I_O is I_{SET} measured at T_O (°K).

Micropower Voltage Reference

FEATURES

- 15μA to 20mA Operating Range—1.2V Version
- 20μA to 20mA Operating Range—2.5V Version
- *Guaranteed* 1Ω Dynamic Impedance
- Very Low Power Consumption

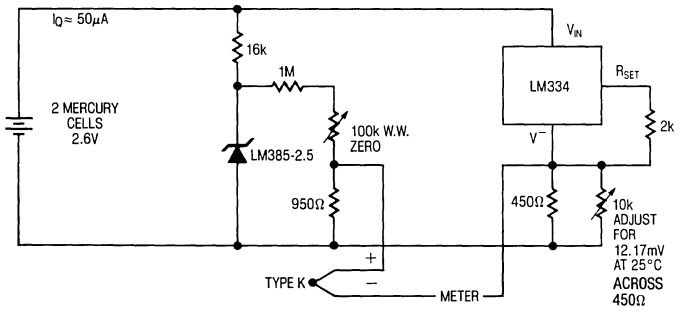
APPLICATIONS

- Portable Meter References
- Portable Test Instruments
- Battery Operated Systems
- Panel Meters
- Current Loop Instrumentation

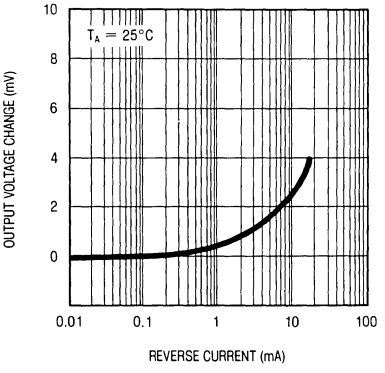
DESCRIPTION

The LM385 series are two terminal band gap reference diodes that have been designed for applications which require precision performance with micropower operation. The devices provide guaranteed operating specifications at currents as low as 15μA. Some additional features are: maximum dynamic impedance of 1Ω, low noise and excellent stability over time and temperature. The advanced design, processing and testing techniques make Linear's LM385 series a superior choice over previous designs. A circuit for cold junction compensation of a thermocouple is shown below.

Thermocouple Cold Junction Compensator



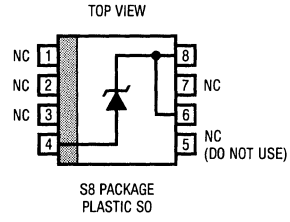
Reverse Voltage Change with Current (LM385-1.2)



ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current 30mA
Forward Current 10mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LM385S8-1.2 LM385S8-2.5
PART MARKING
3851 (1.2V VERSION) 3852 (2.5V VERSION)

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LM385-1.2 MIN	LM385-1.2 TYP	LM385-1.2 MAX	LM385-2.5 MIN	LM385-2.5 TYP	LM385-2.5 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $20\mu A \le I_R \le 20mA$		1.205	1.235	1.260	2.425	2.5	2.575	V
$\frac{\Delta V_Z}{\Delta Temp}$	Average Temperature Coefficient	$I_{MIN} \le I_R \le 20mA$ (Note 2)			20			20		ppm/°C
I_{min}	Minimum Operating Current	$T_{min} \le T_A \le T_{max}$	●		8	15		8	20	μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{min} \le I_R \le 1mA$								
		$T_A = 25°C$				1			2	mV
		$T_{min} \le T_A \le T_{max}$	●			1.5			2.5	mV
		$1mA \le I_R \le 20mA$								
		$T_A = 25°C$				20			20	mV
		$T_{min} \le T_A \le T_{max}$	●			25			25	mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$								
		$T_A = 25°C$			0.4	1		0.4	1	Ω
		$T_{min} \le T_A \le T_{max}$	●			1.5			1.5	Ω
e_n	Wide Band Noise (RMS)	$10Hz \le f \le 10kHz$, $I_R = 100\mu A$			60			120		μV
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 100\mu A$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

Note 1: All specifications are for $T_A = 25°C$ unless otherwise noted. $T_{min} = 0°C$ and $T_{max} = +70°C$.

Note 2: For guaranteed TC and very low initial tolerance, consult LT1034CS8 data sheet. The LT1034CS8 is a low cost, pin for pin substitution device.

Precision Operational Amplifier

FEATURES

- *Guaranteed* Low Offset Voltage 60μV Max.
- *Guaranteed* Low Drift 1.0μV/°C Max.
- *Guaranteed* Low Bias Current 4nA Max.
- *Guaranteed* CMRR 110dB Min.
- *Guaranteed* PSRR 106dB Min.
- Low Power Dissipation 80mW Max.
- Low Noise 0.3μVp-p

APPLICATIONS

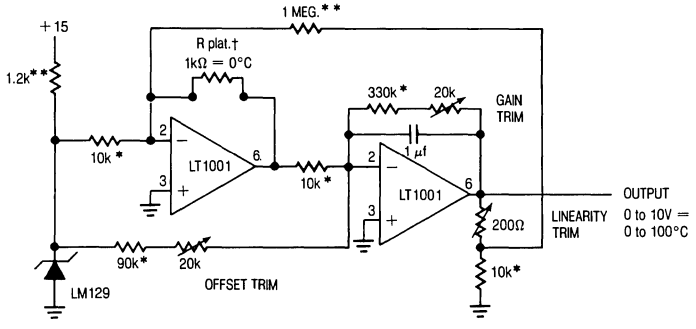
- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- High Accuracy Data Acquisition

DESCRIPTION

The LT1001 significantly advances the state-of-the-art of precision operational amplifiers. In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of the lowest cost, commercial temperature device, the LT1001C, have been dramatically improved when compared to equivalent grades of competing precision amplifiers.

Essentially, the input offset voltage of all units is less than 50μV (see distribution plot below). Input bias and offset currents, common-mode and power supply rejection of the LT1001C offer guaranteed performance which were previously attainable only with expensive, selected grades of other devices. Power dissipation is nearly halved compared to the most popular precision op amps, without adversely affecting noise or speed performance. A beneficial by-product of lower dissipation is decreased warm-up drift. Output drive capability of the L1001 is also enhanced with voltage gain guaranteed at 10mA of load current.

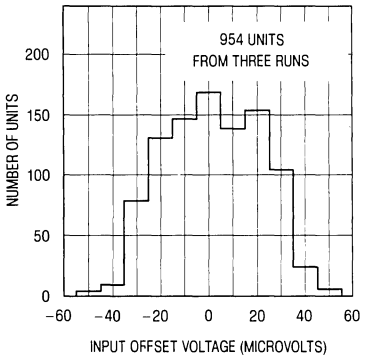
Linearized Platinum Resistance Thermometer with ±0.025°C Accuracy Over 0 to 100°C



* ULTRONIX 105A WIREWOUND
** 1% FILM
† PLATINUM RTD
118MF (ROSEMOUNT, INC.)

‡ Trim sequence: trim offset (0°C = 1000.0Ω), trim linearity (35°C = 1138.7Ω), trim gain (100°C = 1392.6Ω). Repeat until all three points are fixed with ±.025°C.

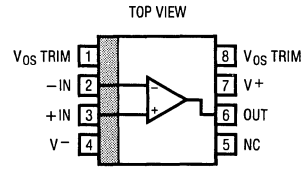
Typical Distribution of Offset Voltage $V_S = \pm 15V$, $T_A = 25°C$



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... ±22V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1001CS8
PART MARKING
1001

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A \leq 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001C MIN	LT1001C TYP	LT1001C MAX	UNITS
V_{OS}	Input Offset Voltage			18	60	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	Note 1 and Note 2		0.3	1.5	µV/month
I_{OS}	Input Offset Current			0.4	3.8	nA
I_b	Input Bias Current			±0.7	±4.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 1)		0.3	0.6	µVp-p
e_n	Input Noise Voltage Density	f_o = 10Hz (Note 1) f_o = 1000Hz (Note 1)		10.5 9.8	18.0 11.0	nV/√Hz
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 12V$ $R_L \geq 1k\Omega$, $V_o = \pm 10V$	400 250	800 500		V/mV V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	106	123		dB
R_{in}	Input Resistance Differential Mode		15	80		MΩ
	Input Voltage Range		±13	±14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13 ±12	±14 ±13.5		V V
S_R	Slew Rate	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.25		V/µs
GBW	Gain-Bandwidth Product	(Note 3)	0.4	0.8		MHz
P_d	Power Dissipation	No Load No Load, $V_S = \pm 3V$		48 4	80 8	mW mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001C MIN	LT1001C TYP	LT1001C MAX	UNITS
V_{OS}	Input Offset Voltage		●		30	110	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●		0.3	1.0	µV/°C
I_{OS}	Input Offset Current		●		0.6	5.3	nA
I_B	Input Bias Current		●		±1.0	±5.5	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	250	750		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	103	120		dB
	Input Voltage Range		●	±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.8		V
P_d	Power Dissipation	No Load	●		55	90	mW

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is tested on a sample basis only.

Note 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation, Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

Note 3: Parameter is guaranteed by design.

Micropower Voltage References

FEATURES

- *Guaranteed* ±4mV initial accuracy LT1004-1.2
- *Guaranteed* ±20mV accuracy LT1004-2.5
- *Guaranteed* 10μA operating current
- *Guaranteed* temperature performance
- Operates up to 20mA
- Very low dynamic impedance

APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Current loop instrumentation

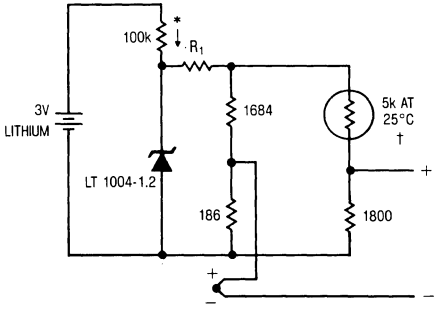
DESCRIPTION

The LT1004 Micropower Voltage References are two terminal bandgap reference diodes designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimization of the key parameters in the design, processing and testing of the device results in accuracy specifications previously attainable only with selected units. Below is a distribution plot of reference voltage for a typical lot of LT1004-1.2. Virtually all of the units fall well within the prescribed limits of ±4mV.

The LT1004 is a pin for pin replacement for the 385 series of references with improved accuracy specifications. More important, the LT1004 is an attractive device for use in systems where accuracy was previously obtained at the expense of power consumption and trimming.

For a low drift micropower reference with guaranteed temperature coefficient, see the LT1034CS8 data sheet.

Micropower Cold Junction Compensation For Thermocouples



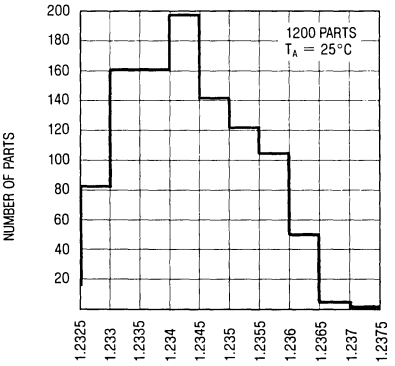
THERMOCOUPLE TYPE	R_1
J	233k
K	299k
T	300k
S	2.1M

* QUIESCENT CURRENT ≅ 15μA

† YELLOW SPRINGS INST. CO. PART #44007

COMPENSATES WITHIN ±1°C FROM 0°C TO 60°C

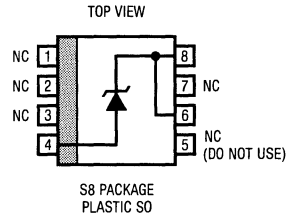
Typical Distribution of Reference Voltage (LT1004-1.2)



ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current..... 30mA
Forward Current..... 10mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LT1004CS8-1.2 LT1004CS8-2.5
PART MARKING
0412 (1.2V VERSION) 0425 (2.5V VERSION)

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1004-1.2 MIN	LT1004-1.2 TYP	LT1004-1.2 MAX	LT1004-2.5 MIN	LT1004-2.5 TYP	LT1004-2.5 MAX	UNITS
V_Z	Reverse Breakdown Voltage	$I_R = 100\mu A$		1.231	1.235	1.239	2.480	2.500	2.520	V
		LT1004C $0°C \leq T_A \leq 70°C$	●	1.225	1.235	1.245	2.470	2.500	2.530	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$I_{min} \leq I_R \leq 20mA$			20			20		ppm/°C
I_{min}	Minimum Operating Current		●		8	10		12	20	μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{min} \leq I_R \leq 1mA$				1			1	mV
			●			1.5			1.5	mV
		$1mA \leq I_R \leq 20mA$				10			10	mV
			●			20			20	mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$			0.2	0.6		0.2	0.6	Ω
			●			1.5			1.5	Ω
e_n	Wide Band Noise (RMS)	$I_R = 100\mu A$ $10Hz \leq f \leq 10kHz$			60			120		μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$I_R = 100\mu A$ $T_A = 25°C \pm 0.1°C$			20			20		ppm/kHr

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: All specifications are for $T_A = 25°C$ unless otherwise noted.

Low Noise, High Speed Precision Operational Amplifiers

FEATURES

- *Guaranteed* 4.5nV/$\sqrt{Hz}$ 10Hz Noise
- *Guaranteed* 3.8nV/$\sqrt{Hz}$ 1kHz Noise
- 0.1 Hz to 10Hz Noise, 60nVp-p, Typical
- *Guaranteed* 5 Million Min. Voltage Gain, $R_L = 2k\Omega$
- *Guaranteed* 2 Million Min. Voltage Gain, $R_L = 600\Omega$
- *Guaranteed* 60μV Max. Offset Voltage
- *Guaranteed* 1.0μV/°C Max. Drift with Temperature
- *Guaranteed* 11V/μsec Min. Slew Rate (LT1037)
- *Guaranteed* 110dB Min. CMRR

APPLICATIONS

- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Sine Wave Generators
- Tape Head Preamplifiers
- Microwave Preamplifiers

DESCRIPTION

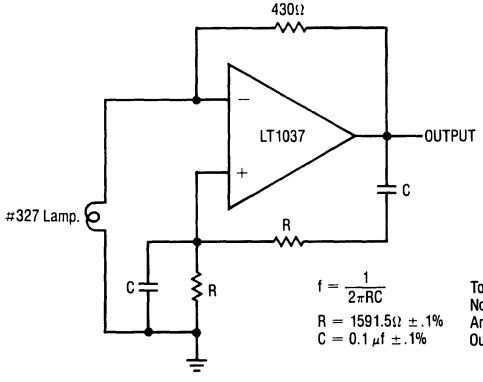
Next to the LT1028, the LT1007/LT1037 series features the lowest noise performance available to date for monolithic operational amplifiers: 2.5nV/$\sqrt{Hz}$ wideband noise (less than the noise of a 400Ω resistor), 1/f corner frequency of 2Hz and 60nV peak to peak 0.1Hz to 10Hz noise. Low noise is combined with outstanding precision and speed specifications: 20μV offset voltage, 0.3μV/°C drift, 126dB common-mode and power supply rejection, and 60MHz gain-bandwidth-product on the decompensated LT1037, which is stable for closed loop gains of 5 or greater.

The voltage gain of the LT1007/LT1037 is an extremely high 20 million driving a 2kΩ load and 12 million driving a 600Ω load to ± 10V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications have been spectacularly improved compared to competing amplifiers.

The sine wave generator application shown below utilizes the low noise and low distortion characteristics of the LT1037.

Ultra-Pure 1kHz Sine Wave Generator

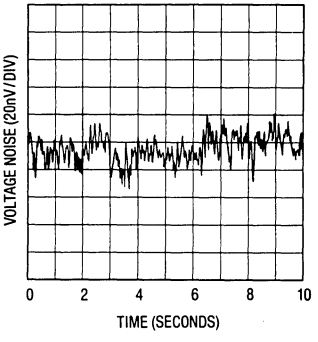


$f = \frac{1}{2\pi RC}$

R = 1591.5Ω ±.1%
C = 0.1 μf ±.1%

Total Harmonic Distortion = < .0025%
Noise = < .0001%
Amplitude = ± 8 volts
Output Frequency = 1.000kHz for values given ±.4%

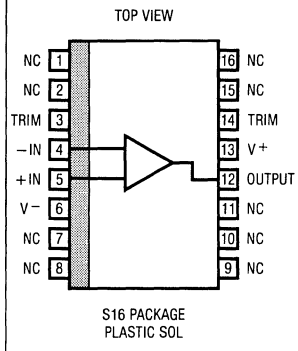
0.1Hz to 10Hz Noise



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Differential Input Current (Note 5) ..... ±25mA
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C

PACKAGE/ORDER INFORMATION



S16 PACKAGE
PLASTIC SOL

ORDER PART NUMBER
LT1007CS LT1037CS
PART MARKING
LT1007CS LT1037CS

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER		CONDITIONS	LT1007C LT1037C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		(Note 1)		20	60	μV
$\frac{V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability		(Notes 2 and 3)		0.2	1.0	μV/Mo
I_{OS}	Input Offset Current				12	50	nA
I_B	Input Bias Current				±15	±55	nA
e_n	Input Noise Voltage		0.1Hz to 10Hz (Note 3)		0.06	0.13	μVp-p
	Input Noise Voltage Density		f_o = 10Hz (Note 3) f_o = 1000Hz (Note 3)		2.8 2.5	4.5 3.8	nV/√Hz nV/√Hz
i_n	Input Noise Current Density		f_o = 10Hz (Note 3) f_o = 1000Hz (Note 3)		1.5 0.4	4.0 0.6	pA/√Hz pA/√Hz
	Input Resistance—Common-Mode				5		GΩ
	Input Voltage Range			±11.0	±12.5		V
CMRR	Common-Mode Rejection Ratio		V_{CM} = ±11V	110	126		dB
PSRR	Power Supply Rejection Ratio		V_S = ±4V to ±18V	106	126		dB
A_{VOL}	Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_O = ±12V $R_L \geq 1k\Omega$, V_O = ±10V $R_L \geq 600\Omega$, V_O = ±10V	5.0 3.5 2.0	20.0 16.0 12.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing		$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.5 ±10.5	±13.5 ±12.5		V V
SR	Slew Rate	LT1007 LT1037	$R_L \geq 2k\Omega$ $A_{VCL} \geq 5$	1.7 11	2.5 15		V/μs V/μs
GBW	Gain-Bandwidth Product	LT1007 LT1037	f_o = 100kHz (Note 4) f_o = 10kHz (Note 4) ($A_{VCL} \geq 5$)	5.0 45	8.0 60		MHz MHz
Z_o	Open Loop Output Resistance		V_O = 0, I_O = 0		70		Ω
P_d	Power Dissipation	LT1007 LT1037			80 85	140 140	mW mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0°C \leq T_A \leq 70°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1007C/LT1037C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		35	110	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 6)	●		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		15	70	nA
I_B	Input Bias Current		●		±20	±75	nA
	Input Voltage Range		●	±10.5	±11.8		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	102	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$ $R_L \geq 1k\Omega, V_O = \pm 10V$	● ●	2.5 2.0	18.0 14.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±13.6		V
P_d	Power Dissipation		●		90	160	mW

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation,changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 3: This parameter is tested on a sample basis only.

Note 4: This parameter is guaranteed by design and is not tested.

Note 5: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Note 6: The Average Input Offset Drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ.

FEATURES

- 0.4% Initial Tolerance Max
- *Guaranteed* Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LM336 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient

APPLICATIONS

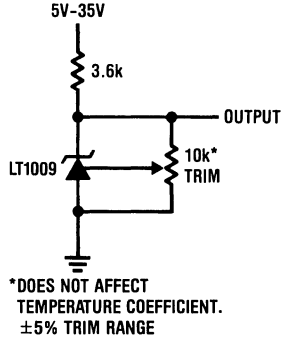
- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

DESCRIPTION

The LT1009 is a precision trimmed 2.500 Volt shunt regulator diode featuring a maximum initial tolerance of only ±10mV. The low dynamic impedance and wide operating current range enhances its versatility. The 0.4% reference tolerance is achieved by on-chip trimming which not only minimizes the initial voltage tolerance but also minimizes the temperature drift.

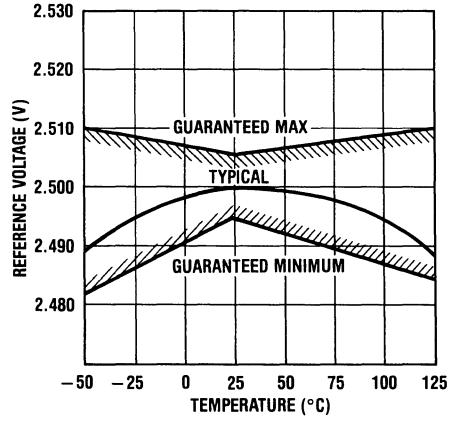
Even though no adjustments are needed with the LT1009, a third terminal allows the reference voltage to be adjusted ±5% to calibrate out system errors. In many applications, the LT1009 can be used as a pin-to-pin replacement of the LM336-2.5 and the external trim network eliminated.

2.5 Volt Reference



*DOES NOT AFFECT TEMPERATURE COEFFICIENT. ±5% TRIM RANGE

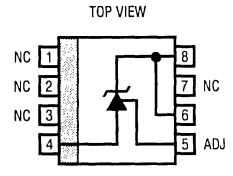
Output Voltage



ABSOLUTE MAXIMUM RATINGS

Reverse Current 20mA
Forward Current 10mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LT1009S8
PART MARKING
1009

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		LT1009S8 MIN	TYP	MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1mA$		2.490	2.500	2.510	V
ΔV_Z	Reverse Breakdown Change with Current	$400\mu A \le I_R \le 10mA$			2.6	10	mV
ΔI_R			●		3	12	mV
r_Z	Reverse Dynamic Impedance	$I_R = 1mA$			0.2	1.0	Ω
			●		0.4	1.4	Ω
$\frac{\Delta V_Z}{\Delta Temp}$	Temperature Stability Average Temperature Coefficient	$T_{MIN} \le T_A \le T_{MAX}$ $0°C \le T_A \le 70°C$ (Note 1)	●		1.8 15	4 25	mV ppm/°C
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1mA$			20		ppm/kHr

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

Picoamp Input Current, Microvolt Offset, Low Noise Op Amp

FEATURES

- Internally Compensated
- *Guaranteed* Offset Voltage 120μV Max.
- *Guaranteed* Bias Current
  - 25°C 300pA Max.
  - 0°C to 70°C 380pA Max.
- *Guaranteed* Drift 1.8μV/°C Max.
- Low Noise, 0.1Hz to 10Hz 0.5μVp-p
- *Guaranteed* Low Supply Current 600μA Max.
- *Guaranteed* CMRR 110dB Min.
- *Guaranteed* PSRR 110dB Min.
- *Guaranteed* Voltage Gain with 5mA Load Current

APPLICATIONS

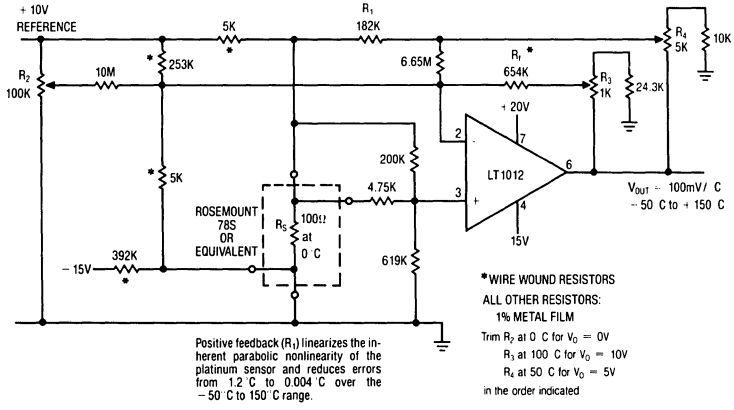
- Precision Instrumentation
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Standard Cell Buffers
- Thermocouple Amplifiers

DESCRIPTION

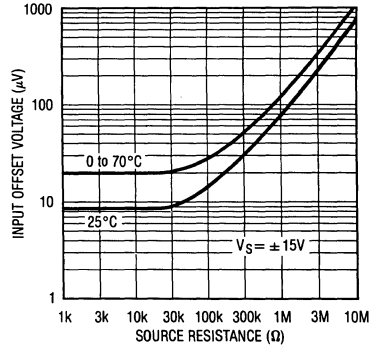
The LT1012 is an internally compensated universal precision operational amplifier which can be used in practically all precision applications. The LT1012 combines picoampere bias currents (which are maintained over the full 0°C to 70°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically unmeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1012's superb precision specifications.

The all around excellence of the LT1012 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1012 can be stocked as the universal internally compensated precision op amp.

Kelvin-Sensed Platinum Temperature Sensor Amplifier



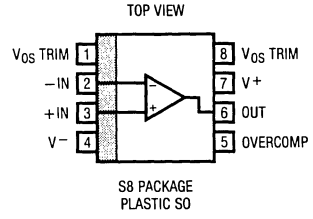
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Current (Note 1)..... ±10mA
Input Voltage..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1012S8
PART MARKING
1012

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012S8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			10	120	µV
		Note 2		25	180	µV
	Long Term Input Offset Voltage Stability			0.3		µV/month
I_{OS}	Input Offset Current			50	280	pA
		Note 2		60	380	pA
I_B	Input Bias Current			±80	±300	pA
		Note 2		±120	±400	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5		µVp-p
e_n	Input Noise Voltage Density	f_O = 10Hz (Note 3)		17	30	nV/√Hz
		f_O = 1000Hz (Note 3)		14	22	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz		20		fA/√Hz
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±12V, R_L ≥ 10kΩ	200	2000		V/mV
		V_{OUT} = ±10V, R_L ≥ 2kΩ	120	1000		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13.5V	110	132		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±20V	110	132		dB
	Input Voltage Range		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	R_L = 10kΩ	±13	±14		V
	Slew Rate		0.1	0.2		V/µs
I_S	Supply Current	Note 2		380	600	µA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq$, $T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1012S8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		20	200	μV
		Note 2	●		30	270	μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.2	1.8	μV/°C
I_{OS}	Input Offset Current		●		60	380	pA
		Note 2	●		80	500	pA
	Average Temperature Coefficient of Input Offset Current		●		0.4	4	pA/°C
I_B	Input Bias Current		●		±100	±420	pA
		Note 2	●		±150	±550	pA
	Average Temperature Coefficient of Input Bias Current		●		0.5	5	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	●	150	1500		V/mV
		$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	100	800		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	●	108	128		dB
	Input Voltage Range		●	±13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±14		V
I_S	Supply Current		●		400	800	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ ($\pm 2.5V \leq V_S \leq \pm 20V$ over the temperature range) and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$).

Note 3: This parameter is tested on a sample basis only.

Dual Precision Op Amp

FEATURES

- Single Supply Operation
  Input Voltage Range Extends to Ground
  Output Swings to Ground while Sinking Current
- Pin Compatible to 1458 and 324 with Precision Specs
- *Guaranteed* Offset Voltage 800μV Max.
- *Guaranteed* Low Drift 5μV/°C Max.
- *Guaranteed* Offset Current 1.5nA Max.
- *Guaranteed* High Gain
  5mA Load Current 1.2 Million Min.
  17mA Load Current 0.5 Million Min.
- *Guaranteed* Low Supply Current 550μA Max.
- Low Voltage Noise, 0.1Hz to 10Hz 0.55μVp-p
- Low Current Noise—Better than OP-07, 0.07pA/√Hz

APPLICATIONS

- Battery-Powered Precision Instrumentation
  Strain Gauge Signal Conditioners
  Thermocouple Amplifiers
  Instrumentation Amplifiers
- 4mA–20mA Current Loop Transmitters
- Multiple Limit Threshold Detection
- Active Filters
- Multiple Gain Blocks

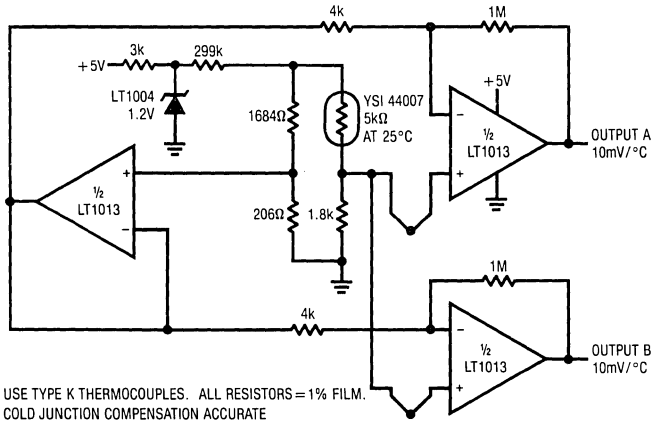
DESCRIPTION

The LT1013 is the first precision dual op amp in the 8-pin small outline (SO) package, upgrading the performance of such popular devices as the MC1458, LM358 and OP-221.

The LT1013's low offset voltage of 200μV, drift of 0.7μV/°C, offset current of 0.2nA, gain of 7 million, common-mode rejection of 114dB, and power supply rejection of 117dB qualify it as two truly precision operational amplifiers. Particularly important is the low offset voltage, since no offset null terminals are provided in the dual configuration. Although supply current is only 350μA per amplifier, a new output stage design sources and sinks in excess of 20mA of load current, while retaining high voltage gain.

The LT1013 can be operated off a single 5V power supply: input common-mode range includes ground; the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent on previous single-supply designs, is eliminated. A full set of specifications is provided with ± 15V and single 5V supplies.

3 Channel Thermocouple Thermometer

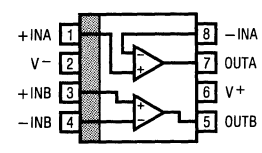


USE TYPE K THERMOCOUPLES. ALL RESISTORS = 1% FILM.
COLD JUNCTION COMPENSATION ACCURATE
TO ±1°C FROM 0°C → 60°C.
USE 4TH AMPLIFIER FOR OUTPUT C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... Equal to Positive Supply Voltage
..... 5V Below Negative Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range
All Grades ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE STANDARD 8-PIN DUAL-IN-LINE CONFIGURATION

ORDER PART NUMBER
LT1013DS8
PART MARKING
1013

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1013D MIN	LT1013D TYP	LT1013D MAX	UNITS
V_{OS}	Input Offset Voltage			200	800	µV
	Long Term Input Offset Voltage Stability			0.5		µV/Mo.
I_{OS}	Input Offset Current			0.2	1.5	nA
I_B	Input Bias Current			15	30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.55		µVp-p
e_n	Input Noise Voltage Density	$f_O = 10Hz$ $f_O = 1000Hz$		24 22		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_O = 10Hz$		0.07		$pA/\sqrt{Hz}$
	Input Resistance—Differential Common-Mode	(Note 1)	70	300 4		MΩ GΩ
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L \geq 2k$ $V_O = \pm 10V$, $R_L = 600\Omega$	1.2 0.5	7.0 2.0		V/µV V/µV
	Input Voltage Range		+13.5 –15.0	+13.8 –15.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$, –15.0V	97	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	100	117		dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$	120	137		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±12.5	±14		V
	Slew Rate		0.2	0.4		V/µs
I_S	Supply Current	Per Amplifier		0.35	0.55	mA

ELECTRICAL CHARACTERISTICS

$V_S^+ = +5V, V_S^- = 0V, V_{OUT} = 1.4V, V_{CM} = 0V, T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013D MIN	LT1013D TYP	LT1013D MAX	UNITS
V_{OS}	Input Offset Voltage			250	950	μV
I_{OS}	Input Offset Current			0.3	2.0	nA
I_B	Input Bias Current			18	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 5mV$ to $4V$, $R_L = 500Ω$		1.0		V/μV
	Input Voltage Range		+3.5 0	+3.8 −0.3		V V
V_{OUT}	Output Voltage Swing	Output Low, No Load Output Low, 600Ω to Ground Output Low, $I_{SINK} = 1mA$ Output High, No Load Output High, 600Ω to Ground	 4.0 3.4	15 5 220 4.4 4.0	25 10 350 	mV mV mV V V
I_S	Supply Current	Per Amplifier		0.32	0.50	mA

ELECTRICAL CHARACTERISTICS

$V_S = ±15V, V_{CM} = 0V, 0°C ≤ T_A ≤ 70°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1013D MIN	LT1013D TYP	LT1013D MAX	UNITS
V_{OS}	Input Offset Voltage		●		230	1000	μV
		$V_S = +5V, 0V; V_O = 1.4V$	●		280	1200	μV
	Average Input Offset Voltage Drift	(Note 2)	●		0.7	5.0	μV/°C
I_{OS}	Input Offset Current		●		0.3	2.8	nA
		$V_S = +5V, 0V; V_O = 1.4V$	●		0.5	6.0	nA
I_B	Input Bias Current		●		16	38	nA
		$V_S = +5V, 0V; V_O = 1.4V$	●		24	90	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = ±10V, R_L = 2k$	●	0.7	4.0		V/μV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = ±13.0V, -15.0V$	●	94	113		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2V$ to $±18V$	●	97	116		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12.0	±13.9		V
		$V_S = +5V, 0V; R_L = 600Ω$					
		Output Low	●		6	13	mV
		Output High	●	3.2	3.9		V
I_S	Supply Current per Amplifier		●		0.37	0.60	mA
		$V_S = +5V, 0V; V_O = 1.4V$	●		0.34	0.55	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is guaranteed by design and is not tested. Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1013s typically 120 op amps will be better than the indicated specification.

Note 2: This parameter is not 100% tested.

FEATURES

- Low Drift—20ppm/°C Max Slope*
- Trimmed Output Voltage*
- Operates in Series or Shunt Mode
- Output Sinks and Sources in Series Mode
- Very Low Noise <1ppm p-p (0.1Hz to 10Hz)
- >100dB Ripple Rejection
- Minimum Input-Output Differential of 1V
- 100% Noise Tested

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Digital Voltmeters
- Inertial Navigation Systems
- Precision Scales
- Portable Reference Standard

*Units specified at 10ppm/°C maximum drift and 0.1% output voltage tolerance are available on request.

DESCRIPTION

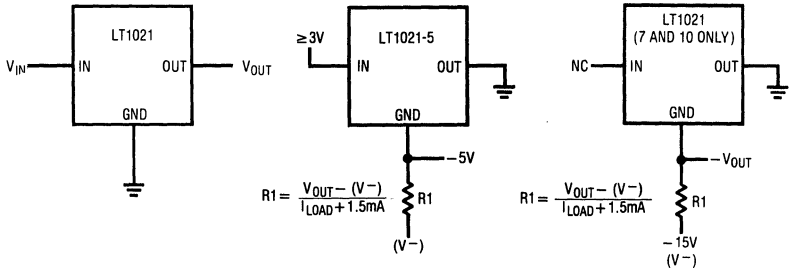
The LT1021 is a precision reference with ultra low drift and noise, extremely good long term stability, and almost total immunity to input voltage variations. The reference output will both source and sink up to 10mA. Three voltages are available; 5V, 7V and 10V. The 7V and 10V units can be used as shunt regulators (two terminal zeners) with the same precision characteristics as the three terminal connection. Special care has been taken to minimize thermal regulation effects and temperature induced hysteresis.

The LT1021 references are based on a buried zener diode structure which eliminates noise and stability problems associated with surface breakdown devices. Further, a subsurface zener exhibits better temperature drift and time stability than even the best band-gap references.

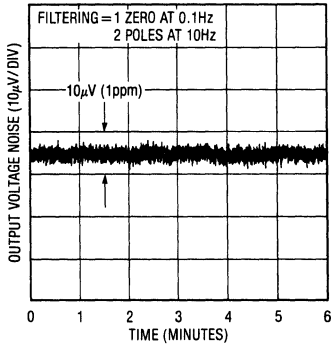
Unique circuit design makes the LT1021 the first IC reference to offer ultra low drift without the use of high power on-chip heaters.

The LT1021-7 uses no resistive divider to set output voltage, and therefore exhibits the best long term stability and temperature hysteresis. The LT1021-5 and LT1021-10 are intended for systems requiring a precise 5V or 10V reference, with an initial tolerance as low as 0.05%.*

Basic Positive and Negative Connections



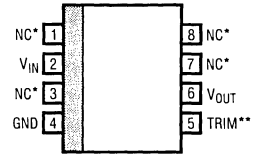
Output Noise 0.1Hz to 10Hz—LT1021-10



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Input-Output Voltage Differential 35V
Output to Ground Voltage (Shunt Mode Current Limit)
  LT1021-5 ..... 10V
  LT1021-7 ..... 10V
  LT1021-10 ..... 16V
Trim Pin to Ground Voltage
  Positive ..... Equal to V_{OUT}
  Negative ..... – 20V
Output Short Circuit Duration
  V_{IN} = 35V ..... 10 sec
  $V_{IN} \leq 20V$ ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range
  All Devices ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.
**NO TRIM PIN ON LT1021-7. DO NOT CONNECT EXTERNAL CIRCUITRY TO PIN 5 ON LT1021-7.

ORDER PART NUMBER
LT1021DCS8-5 LT1021DCS8-7 LT1021DCS8-10
PART MARKING
2105 (5V VERSION) 2107 (7V VERSION) 2110 (10V VERSION)

ELECTRICAL CHARACTERISTICS LT1021-5 V_{IN} = 10V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted

PARAMETER	CONDITIONS		LT1021D-5 MIN	LT1021D-5 TYP	LT1021D-5 MAX	UNITS
Output Voltage (Note 1)			4.95	5.00	5.05	V
Output Voltage Temperature Coefficient (Note 2)	0°C ≤ T_J ≤ 70°C			5	20	ppm/°C
Line Regulation (Note 3)	7.2V ≤ V_{IN} ≤ 10V			4	12	ppm/V
		●			20	ppm/V
	10V ≤ V_{IN} ≤ 40V			2	6	ppm/V
		●			10	ppm/V
Load Regulation (Sourcing Current)	0 ≤ I_{OUT} ≤ 10mA (Note 3)			10	20	ppm/mA
		●			35	ppm/mA
Load Regulation (Sinking Current)	0 ≤ I_{OUT} ≤ 10mA (Note 3)			60	100	ppm/mA
		●			150	ppm/mA
Supply Current				0.8	1.2	mA
		●			1.5	mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz			3		μVp-p
	10Hz ≤ f ≤ 1kHz			2.2	3.5	μVrms
Long Term Stability of Output Voltage				15		ppm/√khrs
Temperature Hysteresis of Output	ΔT = ± 25°C			10		ppm

ELECTRICAL CHARACTERISTICS LT1021-7 V_{IN} = 12V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted

PARAMETER	CONDITIONS	LT1021D-7 MIN	LT1021D-7 TYP	LT1021D-7 MAX	UNITS
Output Voltage (Note 1)		6.95	7.00	7.05	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$		5	20	ppm/°C

ELECTRICAL CHARACTERISTICS LT1021-7 V_{IN} = 12V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted

PARAMETER	CONDITIONS		LT1021D-7 MIN	LT1021D-7 TYP	LT1021D-7 MAX	UNITS
Line Regulation (Note 3)	8.5V ≤ V_{IN} ≤ 12V			1	4	ppm/V
		●		2	8	ppm/V
	12V ≤ V_{IN} ≤ 40V			0.5	2	ppm/V
		●		1	4	ppm/V
Load Regulation (Sourcing Current)	0 ≤ I_{OUT} ≤ 10mA			12	25	ppm/mA
	(Note 3)	●			40	ppm/mA
Load Regulation (Shunt Mode)	1.2mA ≤ I_{SHUNT} ≤ 10mA			50	100	ppm/mA
	(Notes 3, 4)	●			150	ppm/mA
Supply Current (Series Mode)				0.75	1.2	mA
		●			1.5	mA
Minimum Current (Shunt Mode)	V_{IN} is Open			0.7	1.0	mA
		●			1.2	mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz			4		μVp-p
	10Hz ≤ f ≤ 1kHz			2.5	4	μVrms
Long Term Stability of Output Voltage				7		ppm/√khrs
Temperature Hysteresis of Output	ΔT = ±25°C			3		ppm

ELECTRICAL CHARACTERISTICS LT1021-10 V_{IN} = 15V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted

PARAMETER	CONDITIONS		LT1021D-10 MIN	LT1021D-10 TYP	LT1021D-10 MAX	UNITS
Output Voltage (Note 1)			9.95	10.00	10.05	V
Output Voltage Temperature Coefficient (Note 2)	T_{MIN} ≤ T_J ≤ T_{MAX}			5	20	ppm/°C
Line Regulation (Note 3)	11.5V ≤ V_{IN} ≤ 14V.5			1	4	ppm/V
		●			6	ppm/V
	14.5V ≤ V_{IN} ≤ 40V			0.5	2	ppm/V
		●			4	ppm/V
Load Regulation (Sourcing Current)	0 ≤ I_{OUT} ≤ 10mA			12	25	ppm/mA
	(Note 3)	●			40	ppm/mA
Load Regulation (Shunt Mode)	1.7mA ≤ I_{SHUNT} ≤ 10mA			50	100	ppm/mA
	(Notes 3, 4)	●			150	ppm/mA
Series Mode Supply Current				1.2	1.7	mA
		●			2.0	mA
Shunt Mode Minimum Current	V_{IN} is Open			1.1	1.5	mA
		●			1.7	mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz			6		μVp-p
	0.1Hz ≤ f ≤ 1kHz			3.5	6	μVrms
Long Term Stability of Output Voltage	Δt = 1000 Hrs Non-Cumulative			15		ppm/√khrs
Temperature Hysteresis of Output	ΔT = ±25°C			5		ppm

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is guaranteed as a slope from room temperature (25°C) to 0°C and 70°C, also known as a "butterfly" specification.

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately. Package thermal resistance is 110°C/W.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

Note 5: RMS noise is measured with a single high pass filter at 10Hz and a 2-pole low pass filter at 1 kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS, and a second correction of 0.88 is used to correct for the non-ideal bandpass of the filters.

Peak-to-peak noise is measured with a single high pass filter at 0.1Hz and a 2-pole low pass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

Ultra-Low Noise Precision High Speed Op Amp

FEATURES

- Voltage Noise — 1.2nV/√Hz Max. at 1kHz; 0.9nV/√Hz Typ. at 1kHz; 1.0nV/√Hz Typ. at 10Hz; 35nVp-p Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product — 50MHz Min.
- Slew Rate — 11V/μs Min.
- Offset Voltage — 80μV Max.
- Voltage Gain — 5 Million Min.
- Drift with Temperature — 1μV/°C Max.

APPLICATIONS

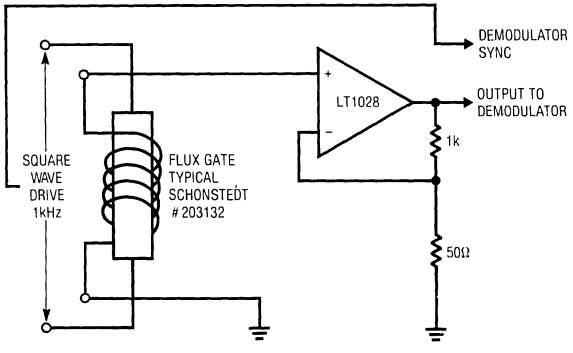
- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

DESCRIPTION

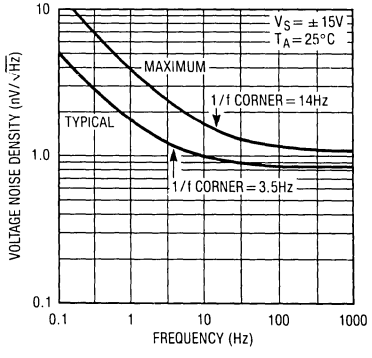
The LT1028 achieves a new standard of excellence in noise performance with 0.9nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz), distortion free output, and true precision parameters (0.2μV/°C drift, 20μV offset voltage, 30 million voltage gain). Although the LT1028 input stage operates at nearly 1mA of collector currents to achieve low voltage noise, input bias current is only 30nA.

The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

Flux Gate Amplifier



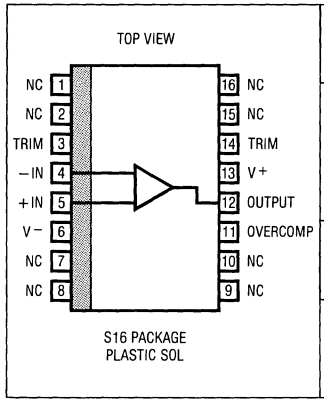
Voltage Noise vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Current (Note 4) ..... ±25mA
Input Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1028CS
PART MARKING
LT1028CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028CS MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		20	80	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3		µV/Mo
I_{OS}	Input Offset Current	$V_{CM} = 0V$		18	100	nA
I_B	Input Bias Current	$V_{CM} = 0V$		±30	±180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	90	nVp-p
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 3) $f_o = 1000Hz$, 100% tested		1.0 0.9	1.9 1.2	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_o = 10Hz$ (Notes 3 and 5) $f_o = 1000Hz$, 100% tested		4.7 1.0	12.0 1.8	$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance Common-Mode Differential Mode			 300 20		 MΩ kΩ
	Input Capacitance			5		pF
	Input Voltage Range		±11.0	±12.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$	110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	110	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 12V$ $R_L \geq 1k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	5.0 3.5 2.0	30.0 20.0 15.0		V/µV V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.5	±13.0 ±12.2		V V
SR	Slew Rate	$A_{VCL} = -1$	11	15		V/µs
GBW	Gain-Bandwidth Product	$f_o = 20kHz$ (Note 6)	50	75		MHz
Z_o	Open Loop Output Impedance	$V_o = 0$, $I_o = 0$		80		Ω
I_S	Supply Current			7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028CS MIN	LT1028CS TYP	LT1028CS MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	125	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	1.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		22	130	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±40	±240	nA
	Input Voltage Range		●	±10.5	±12.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	107	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$ $R_L \ge 1k\Omega$, $V_O = \pm 10V$	●	3.0 2.5	25.0 18.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±11.5	±12.7		V
I_S	Supply Current		●		8.2	11.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25°C$, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 3: This parameter is tested on a sample basis only.

Note 4: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 7: This parameter is not 100% tested.

Quad Low Power Line Driver

FEATURES

- Low Operating Voltage ±5V to ±15V
- 500μA Supply Current
- Zero Supply Current when Shut Down
- Outputs can be Driven ±30V
- Output "Open" when Off (3-State)
- 10mA Output Drive
- Pin Compatible with 1488
- Output of Several Devices can be Paralleled

APPLICATIONS

- RS232 Driver
- Micropower Interface
- Level Translator

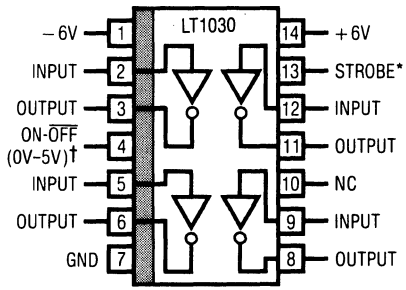
DESCRIPTION

The LT1030 is an RS232 line driver that operates over a ±5V to ±15V range on low supply current and can be shut down to zero supply current. Outputs are fully protected from externally applied voltages of ±30V by current limiting. Since the output swings to within 200mV of the positive supply and 1V of the negative supply, power supply needs are minimized.

A major advantage of the LT1030 is the high impedance output state when off or powered down, which allows several different drivers on the same bus.

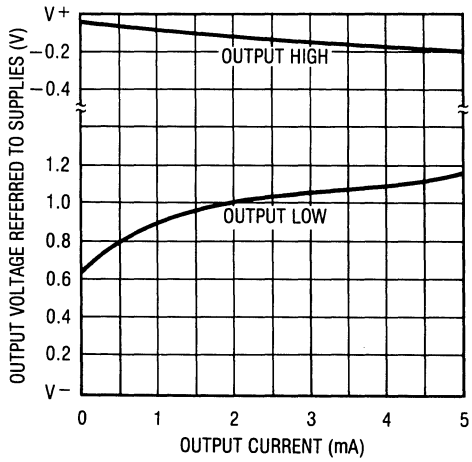
TYPICAL APPLICATION

RS232 Line Driver



*NO CONNECTION NEEDED WHEN NOT USED.
†5V = ON.

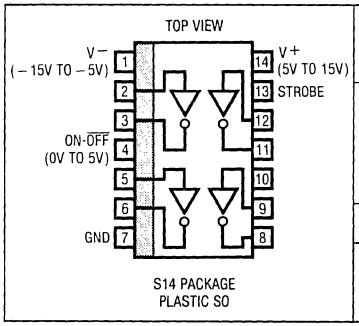
Output Swing vs Output Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±15V
Logic Input Pins ..... V^- to 25V
On-$\overline{\text{Off}}$ Pin ..... GND to 12V
Output (Forced) ..... V^- +30V, V^+ −30V
Short Circuit Duration (to ±30V) ..... Indefinite
Operating Temperature Range
LT1030C ..... 0°C to 70°C
Guaranteed Functional by Design ... −25°C to 85°C
Storage Temperature ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1030CS
PART MARKING
LT1030CS

ELECTRICAL CHARACTERISTICS (Supply Voltage = ±5V to ±15V)

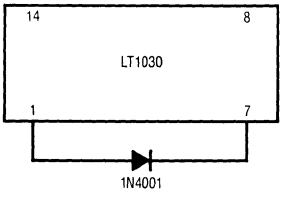
PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current	$V_{ON\text{-}\overline{OFF}} \geq 2.4V$, $I_{OUT} = 0$, All Outputs Low		●		500	1000	μA
Power Supply Leakage Current	$V_{ON\text{-}\overline{OFF}} \leq 0.4V$				1	10	μA
	$V_{ON\text{-}\overline{OFF}} \leq 0.1V$		●		10	150	μA
Output Voltage Swing	Load = 2mA	Positive		$V^+ - 0.3V$	$V^+ - 0.1V$		V
		Negative			$V^- + 0.9V$	$V^- + 1.4V$	V
Output Current	V_{SUPPLY} ±5V to ±15V			5	12		mA
Output Overload Voltage (Forced)	Operating or Shutdown		●	$V^+ - 30V$		$V^- + 30V$	V
Output Current	Shutdown $V_{OUT} = \pm 30V$				2	100	μA
Input Overload Voltage (Forced)	Operating or Shutdown		●	V^-		15	V
Logic Input Levels	Low Input (V_{OUT} = High)		●		1.4	0.8	V
	High Input (V_{OUT} = Low)		●	2	1.4		V
Logic Input Current	$V_{IN} > 2.0V$				2	20	μA
	$V_{IN} < 0.8V$				10	20	μA
On-$\overline{\text{Off}}$ Pin Current	$0 \leq V_{IN} \leq 5V$		●	−10	30	65	μA
Slew Rate				4	15	30	V/μS

The ● denotes specifications which apply over the operating temperature range.

Note 1: 3V applied to the strobe pin will force all outputs low. Strobe pin input impedance is about 2k to ground. Leave open when not used.

PIN FUNCTIONS

PIN	FUNCTION	COMMENT
1	Minus Supply	Operates −2V to −15V
2,5,9,12	Logic Input	Operates properly on TTL or CMOS levels. Output valid from $(V^- + 2V) \leq V_{IN} \leq 15V$. Connect to 5V when not used.
3,6,8,11	Output	Line drive output.
4	On-$\overline{\text{Off}}$	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect between 5V-10V.
7	Ground	Ground must be more positive than V^-
13	Strobe	Forces all outputs low. Drive with 3V.
14		Positive supply 5V to 15V.



Note: As with other bipolar ICs, forward biasing the substrate diode can cause problems. The LT1030 will draw high current from V^+ to ground if the V^- pin is open circuited or pulled above ground. If this is possible, connecting a diode from V^- to ground will prevent the high current state. Any low cost diode can be used.

Micropower Dual Reference

FEATURES

- *Guaranteed* 40 ppm/°C Drift
- 20μA to 20mA Operation (1.2V)
- 1Ω Dynamic Impedance
- 7V, 100μA Reference

APPLICATIONS

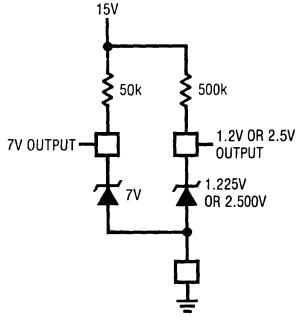
- Portable Meters
- Precision Regulators
- Calibrators

DESCRIPTION

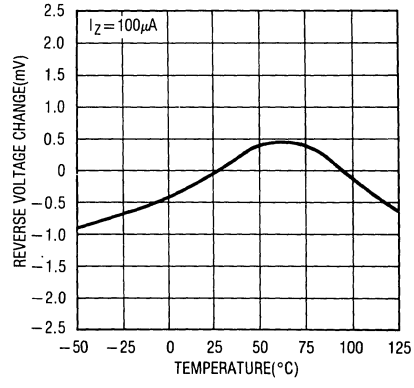
The LT1034 is a micropower, precision 1.2V/2.5V reference combined with a 7V auxiliary reference. The 1.2V/2.5V reference is a trimmed, thin-film, band-gap voltage reference with 1% initial tolerance and guaranteed 20ppm/°C temperature drift. Operating on only 20μA, the LT1034 offers guaranteed drift, low temperature cycling hysteresis and good long term stability. The low dynamic impedance makes the LT1034 easy to use from unregulated supplies. The 7V reference is a subsurface zener device for less demanding applications.

The LT1034 reference can be used as a high performance upgrade of the LM385 or LT1004, where guaranteed temperature drift is desired.

TYPICAL APPLICATION



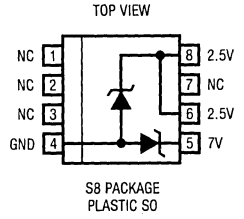
Temperature Drift
LT1034CS8-1.2



ABSOLUTE MAXIMUM RATINGS

Operating Current.....20mA
Forward Current (Note 1).....20mA
Operating Temperature Range .....0°C to 70°C
Storage Temperature..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LT1034CS8-1.2 LT1034CS8-2.5
PART MARKING
3401 (1.2V VERSION) 3402 (2.5V VERSION)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1034CS8-1.2 MIN	LT1034CS8-1.2 TYP	LT1034CS8-1.2 MAX	LT1034CS8-2.5 MIN	LT1034CS8-2.5 TYP	LT1034CS8-2.5 MAX	UNITS
Reverse Breakdown Voltage	$I_R = 100\mu A$	25°C	1.210	1.225	1.240	2.46	2.5	2.54	V
		●	1.205	1.225	1.245	2.43	2.5	2.57	V
Reverse Breakdown Change with Current	Note 3	25°C		0.5	2.0		1	3	mV
		●		1.0	4.0		1.5	6	mV
	$2mA \le I_R \le 20mA$	25°C		4	8.0		6	16	mV
		●		6.0	15.0		10	20	mV
Minimum Operating Current		●		10	20		15	30	μA
Temperature Coefficient	$I_R = 100\mu A$	●		20	40		20	40	ppm/°C
Reverse Dynamic Impedance (Note 2)	$I_R = 100\mu A$	25°C		0.25	1.0		0.5	1.5	Ω
		●		0.50	2.0		1	2.5	Ω
Low Frequency Noise	$I_R = 100\mu A$, $0.1Hz \le F \le 10Hz$	●		4			6		μVp-p
Long Term Stability	$I_R = 100\mu A$, T = 25°C	25°C		20			20		ppm/$\sqrt{khrs}$

ELECTRICAL CHARACTERISTICS 7V Reference

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$I_R = 100\mu A$	25°C	6.8	7.0	7.3	V
		●	6.75	7.0	7.4	V
Reverse Breakdown Change with Current	$100\mu A \le I_R \le 1mA$	25°C		90	140	mV
	$100\mu A \le I_R \le 1mA$	●		100	190	mV
	$1mA \le I_R \le 20mA$	25°C		160	250	mV
	$1mA \le I_R \le 20mA$	●		200	350	mV
Temperature Coefficient	$I_R = 100\mu A$	●		40		ppm/°C
Long Term Stability	$I_R = 100\mu A$	25°C		20		ppm/$\sqrt{khrs}$

The ● denotes specifications that apply over the operating temperature range.

Note 1: Forward biasing either diode will affect the operation of the other diode.

Note 2: This parameter guaranteed by "reverse breakdown change with current" test.

Note 3: For the LT1034CS8-1.2, $20\mu A \le I_R \le 2mA$. For the LT1034CS8-2.5, $30\mu A \le I_R \le 2mA$.

Precision, High Speed, JFET Input Operational Amplifiers

FEATURES

- *Guaranteed* Offset Voltage 1.5mV Max.
  0°C to 70°C 2.2mV Max.
- Low Drift 4μV/°C Typ.
- *Guaranteed* Bias Current
  70°C Warmed Up 400pA Max.
- *Guaranteed* Slew Rate 9V/μs Min.

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters
- Fast, Precision Sample and Hold

DESCRIPTION

The LT1055/LT1056 JFET input operational amplifiers combine precision specifications with high speed performance.

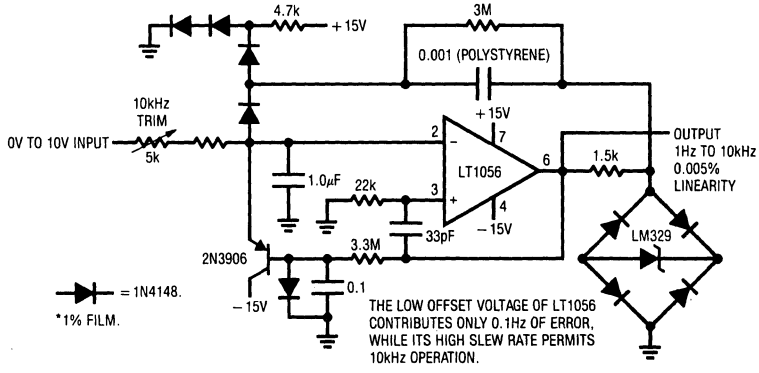
For the first time in an SO package, 14V/μs slew rate and 5.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 0.5mV, 4μV/°C drift, and bias currents of 60pA at 70°C.

The 1.5mV maximum offset voltage specification is the best available on any JFET input operational amplifier in the plastic SO package.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

The voltage to frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

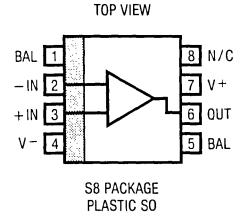
0 to 10kHz Voltage-to-Frequency Converter



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LT1055S8 LT1056S8
PART MARKING
1055 1056

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055S8 LT1056S8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 1)			500	1500	µV
I_{OS}	Input Offset Current	Fully Warmed Up		5	30	pA
I_B	Input Bias Current	Fully Warmed Up V_{CM} = +10V		±30 30	±100 150	pA pA
	Input Resistance —Differential —Common-Mode	 V_{CM} = –11V to +8V V_{CM} = +8V to +11V		0.4 0.4 0.05		TΩ TΩ TΩ
	Input Capacitance			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1055 LT1056		2.5 3.5		µVp-p µVp-p
e_n	Input Noise Voltage Density	f_O = 10Hz (Note 2) f_O = 1kHz (Note 2)		35 15	70 22	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, 1kHz (Note 3)		2.5	10	fA/√Hz
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V R_L = 2k R_L = 1k	120 100	400 300		V/mV V/mV
	Input Voltage Range		±11	±12		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±11V	83	98		dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V	88	104		dB
V_{OUT}	Output Voltage Swing	R_L = 2k	±12	±13.2		V
SR	Slew Rate	LT1055 LT1056	7.5 9.0	12 14		V/µs V/µs
GBW	Gain-Bandwidth Product	f = 1MHz LT1055 LT1056		4.5 5.5		MHz MHz
I_S	Supply Current	LT1055 LT1056		2.8 5.0	4.0 7.0	mA mA
	Offset Voltage Adjustment Range	R_{POT} = 100k		±5		mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055S8/1056S8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 1)		●		800	2200	μV
	Average Temperature Coefficient of Input Offset Voltage		●		4	15	μV/°C
I_{OS}	Input Offset Current	Warmed Up $T_A = 70°C$	●		18	150	pA
I_B	Input Bias Current	Warmed Up $T_A = 70°C$	●		±60	±400	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	60	250		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	82	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	87	103		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.1		V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25°C$ only, with the chip heated to approximately 38°C for the LT1055 and to 45°C for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 4: Offset voltage drift with temperature is practically unchanged when the offset voltage voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+.

5V Powered RS232 Driver/ Receiver with Shutdown

FEATURES

- Operates on Single 5V Power Supply
- Generates ±9V Supplies with Only 1μF Capacitors
- Fully Protected Against Output Overloads
- RS232 Outputs can be Forced ±30V without Damage
- Three-state Outputs are High Impedance when Off
- Bipolar Circuitry; No Latch Up
- ±30V Receiver Input Range
- Can Power Additional RS232 Drivers such as LT1039
- No Supply Current in Shutdown
- Meets All RS232 Specifications
- 16 Pin Version without Shutdown Available

APPLICATIONS

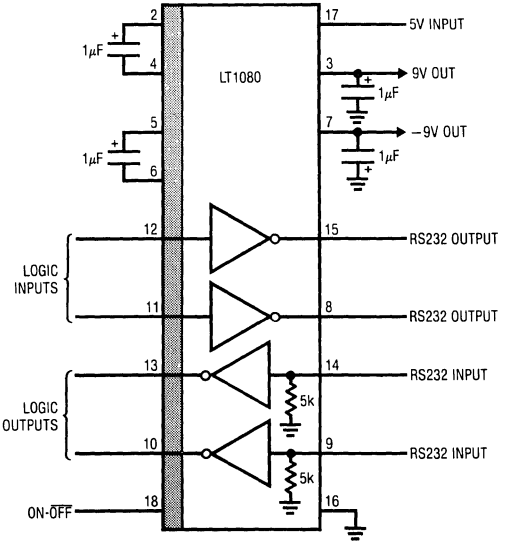
- RS232 Interface
- Battery Powered Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

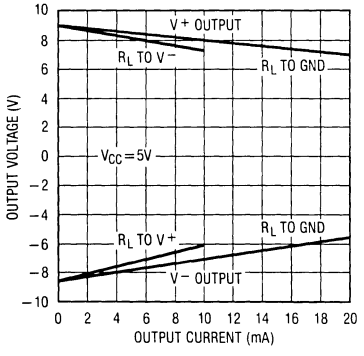
The LT1080 is a dual RS232 driver/receiver which includes a capacitive voltage generator to supply RS232 voltage levels from a single 5V supply. Each receiver will accept up to ±30V input and can drive either TTL or CMOS logic. The RS232 drivers accept logic inputs and output RS232 voltage levels. The driver outputs are fully protected against overload and can be shorted to ground or up to ±30V without damage. Additionally, when the system is in the SHUTDOWN mode the driver and receiver outputs are at a high impedance allowing data line sharing. Bipolar circuitry makes this driver/receiver exceptionally rugged against overloads or ESD damage.

The power supply generator doubles the 5V input supply to obtain 9V, and then inverts the 9V to obtain –8.5V. Up to 15mA of external current is available to power additonal RS232 drivers or other external circuitry. The SHUTDOWN mode disables the supply generators and reduces input supply current to zero. A version of the LT1080, the LT1081, is available without shutdown for 16 pin applications.

TYPICAL APPLICATION



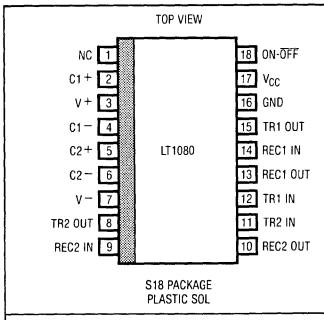
Supply Generator Outputs



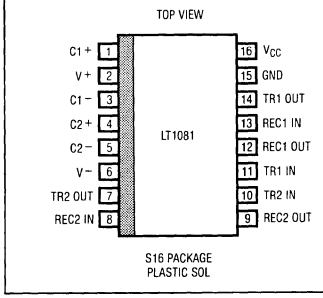
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
V^+ 12V
V^- ..... −12V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
  On-Off Pin ..... GND to 12V
Output Voltage
  Driver ..... V^- + 30V to V^+ − 30V
  Receiver ..... −0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 Seconds
  V^- ..... 30 Seconds
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1080C ..... 0°C to 70°C
  Guaranteed Functional ..... −25°C to 85°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1080CS
PART MARKING
LT1080CS



ORDER PART NUMBER
LT1081CS
PART MARKING
LT1081CS

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Driver							
Output Voltage Swing	Load = 3k to GND Both Outputs.	Positive Negative	● ●	5.0 −5.0	7.3 −6.5		V V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High) Input High Level (V_{OUT} = Low)		● ●	 2.0	1.4 1.4	0.8	V V
Logic Input Current	$V_{IN} \geq 2.0V$ $V_{IN} \leq 0.8V$		● ●	 	5 5	20 20	µA µA
Output Short Circuit Current	Sourcing Current, V_{OUT} = 0V Sinking Current, V_{OUT} = 0V			7 −7	12 −12		mA mA
Output Leakage Current	SHUTDOWN (Note 2), V_{OUT} = ±30V		●		10	100	µA
Slew Rate	R_L = 3kΩ, C_L = 51pF			4	15	30	V/µs
Receiver							
Input Voltage Thresholds	Input Low Threshold, (V_{OUT} = High) Input High Threshold, (V_{OUT} = Low)		● ●	0.2 	1.3 1.7	 3.0	V V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance				3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA Output High, I_{OUT} = 160µA (V_{CC} = 5V)		● ●	 3.5	0.2 4.8	0.4 	V V
Output Short Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V			−10 0.6	−20 1		mA mA
Output Leakage Current	SHUTDOWN (Note 2), $0V \leq V_{OUT} \leq V_{CC}$		●		1	10	µA

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator (Note 3)						
V+ Output Voltage	I_{OUT} = 0mA I_{OUT} = 10mA I_{OUT} = 15mA		8 7 6.5	9 8 7.5		V V V
V− Output Voltage	I_{OUT} = 0mA I_{OUT} = −10mA I_{OUT} = −15mA		−7.5 −5.5 −5	−8.5 −6.5 −6		V V V
Supply Current		●		10	22	mA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 2) (LT1080 Only)	●		1	100	μA
On-$\overline{Off}$ Pin Current	$0V \le V_{ON\text{-}\overline{OFF}} \le 5V$ (LT1080 Only)	●	−15		80	μA
Supply Rise Time	(Note 4)			1		ms

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$).The LT1080/LT1081 is guaranteed functional by design for $-25°C \le T_A \le 85°C$.

Note 1: These parameters apply for $4.5V \le V_{CC} \le 5.5V$ and $V_{ON\text{-}\overline{OFF}} = 3V$, unless otherwise specified.

Note 2: $V_{ON\text{-}\overline{OFF}} = 0.4V$. (LT1080 only)

Note 3: Unless otherwise specified, $V_{CC} = 5V$, external loading of V+ and V− equals zero and the driver outputs are low (inputs high).

Note 4: Time from either SHUTDOWN high (LT1080 only) or power on until V+ ≥ 6V and V− ≤ −6V. All external capacitors are 1μF.

PIN FUNCTIONS

V_{CC} (Pin 17): Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND (Pin 16): Ground pin.

On-$\overline{Off}$ (Pin 18): Controls the operation mode of the LT1080 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V+ (Pin 3): Positive supply for RS232 drivers. $V+ \approx 2V_{CC} - 1.5V$. Requires an external capacitor (≥1μF) for charge storage. May be loaded (up to 15mA) for external system use. Loading does reduce V+ voltage (see graphs.)

V− (Pin 7): Negative supply for RS232 drivers. $V- \approx -(2V_{CC} - 2.5V)$. Requires an external capacitor (≥1μF) for charge storage. May be loaded (up to −15mA) for external system use. Loading does reduce V− voltage (see graphs).

TR1 IN; TR2 IN (Pins 12, 11): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT; TR2 OUT (Pins 15, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off ($V_{CC} = 0V$) to allow data line sharing. Outputs are fully short circuit protected from V− +30V to V+ −30V with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than ±45V and higher applied voltages will not damage the device if moderately current limited.

REC1 IN; REC2 IN (Pins 14, 9): Receiver inputs. Accepts RS232 voltage levels (±30V) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5kΩ.

REC1 OUT; REC2 OUT (Pins 13, 10): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

C1+; C1−; C2+; C2− (Pins 2, 4, 5, 6): No user applications. Requires an external capacitor (≥1μF) from C1+ to C1− and another from C2+ to C2−.

Dual Precision Instrumentation Switched-Capacitor Building Block

FEATURES

- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 3V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Low Power
- Two Independent Sections with One Clock

APPLICATIONS

- Precision Instrumentation Amplifiers
- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V–F and F–V Converters
- Sample and Hold
- Switched-Capacitor Filters

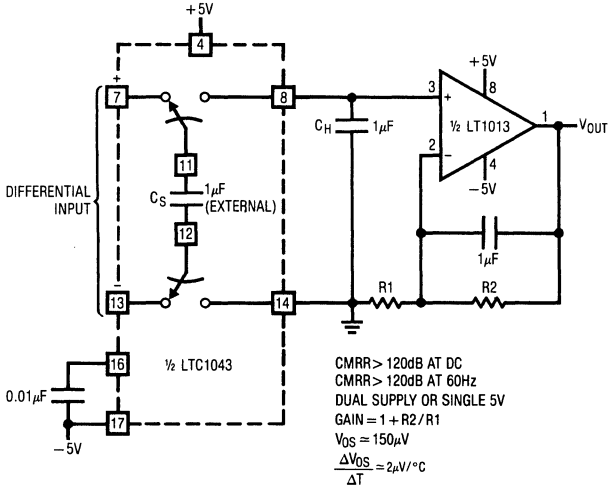
DESCRIPTION

The LTC1043 is a monolithic, charge-balanced, dual switched-capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V–F and F–V circuits without trimming, and it is also a building block for switched-capacitor filters, oscillators and modulators.

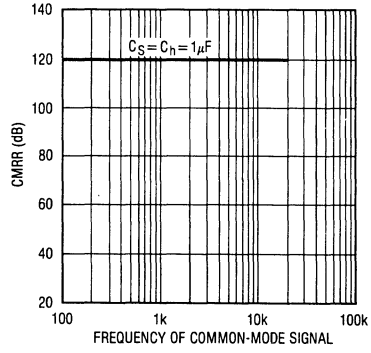
The LTC1043 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

Instrumentation Amplifier



CMRR > 120dB AT DC
CMRR > 120dB AT 60Hz
DUAL SUPPLY OR SINGLE 5V
GAIN = 1 + R2/R1
$V_{OS} \approx 150\mu V$
$\frac{\Delta V_{OS}}{\Delta T} \approx 2\mu V/°C$
COMMON-MODE INPUT VOLTAGE INCLUDES THE SUPPLIES

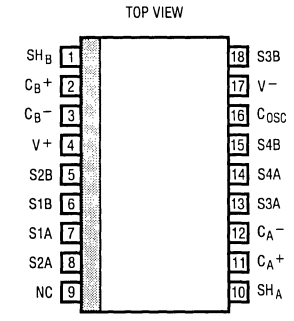
CMRR vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Input Voltage
at Any Pin ..... $-0.3V \le V_{IN} \le V^+ + 0.3V$
Operating Temperature Range..... $-40°C \le T_A \le 85°C$
Storage Temperature Range..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



S18 PACKAGE
PLASTIC SOL

ORDER PART NUMBER
LTC1043CS
PART MARKING
LTC1043CS

ELECTRICAL CHARACTERISTICS

$V^+ = 10V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1043C MIN	TYP	MAX	UNITS
I_S	Power Supply Current	Pin 16 Connected High or Low			0.25	0.4	mA
			●			0.7	mA
		C_{OSC} (Pin 16 to V^-) = 100pF			0.4	0.65	mA
			●			1	mA
I_I	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 1)			6	100	pA
			●		6		nA
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 7V$, $I = \pm 0.5mA$			240	400	Ω
		$V^+ = 10V$, $V^- = 0V$	●			700	Ω
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 3.1V$, $I = \pm 0.5mA$			400	700	Ω
		$V^+ = 5V$, $V^- = 0V$	●			1	kΩ
f_{OSC}	Internal Oscillator Frequency	C_{OSC} (Pin 16 to V^-) = 0pF			185		kHz
		C_{OSC} (Pin 16 to V^-) = 100pF		20	34	50	kHz
		Test Circuit 3	●	15		75	kHz
I_{OSC}	Pin Source or Sink Current	Pin 16 at V^+ or V^-			40	70	μA
			●			100	μA
	Break-Before-Make-Time				25		ns
	Clock to Switching Delay	C_{OSC} Pin Externally Driven			75		ns
f_M	Maximum External CLK Frequency	C_{OSC} Pin Externally Driven with CMOS Levels			5		MHz
CMRR	Common-Mode Rejection Ratio	$V^+ = 5V$, $V^- = -5V$, $-5V < V_{CM} < 5V$, DC to 400Hz			120		dB

The ● denotes specifications which apply over the full operating temperature range. LTC1043 operates from $-40°C \le T_A \le 85°C$.

Note 1: OFF leakage current is guaranteed but not tested at 25°C.

Switched Capacitor Voltage Converter

FEATURES

- Plug-In Compatible with 7660 with These Additional Features:
  - *Guaranteed* Operation to 9V, with No External Diode, Over Full Temperature Range
  - Boost Pin (Pin 1) for Higher Switching Frequency
  - Lower Quiescent Power
  - Efficient Voltage Doubler
- 200μA *Max.* No Load Supply Current at 5V
- 97% *Min.* Open Circuit Voltage Conversion Efficiency
- 95% *Min.* Power Conversion Efficiency
- Wide Operating Supply Voltage Range, 1.5V to 9V
- Easy to Use
- Commercial Device *Guaranteed* Over −40°C to 85°C Temperature Range

APPLICATIONS

- Conversion of +5V to ±5V Supplies
- Precise Voltage Division, $V_{OUT} = V_{IN}/2 \pm 20ppm$
- Voltage Multiplication, $V_{OUT} = \pm nV_{IN}$
- Supply Splitter, $V_{OUT} = \pm V_S/2$

DESCRIPTION

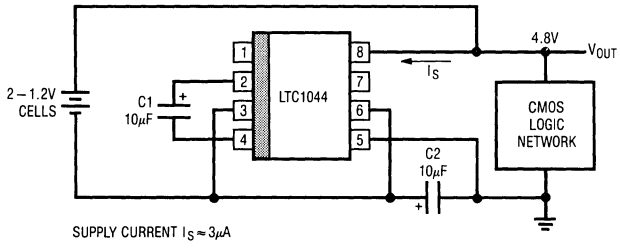
The LTC1044 is a monolithic CMOS switched capacitor voltage converter which is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. The LTC1044 provides several voltage conversion functions: the input voltage can be inverted ($V_{OUT} = -V_{IN}$), doubled ($V_{OUT} = 2V_{IN}$), divided ($V_{OUT} = V_{IN}/2$) or multiplied ($V_{OUT} = \pm nV_{IN}$).

Designed to be pin-for-pin and functionally compatible with the popular 7660, the LTC1044 provides significant features and improvements over earlier 7660 designs. These improvements include: full 1.5V to 9V supply operation over the entire operating temperature range, without the need for external protection diodes; 2½ times lower quiescent current for greater power conversion efficiency; and a "boost" function which is available to raise the internal oscillator frequency to optimize performance in specific applications.

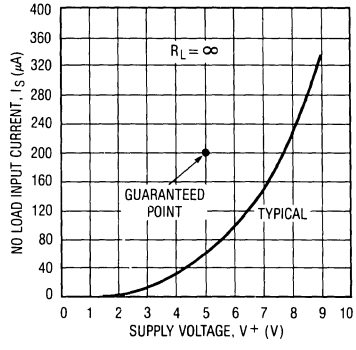
Although the LTC1044 provides significant design and performance advantages over the earlier 7660 device, it still maintains its compatibility with existing 7660 designs.

LTCMOS™ is a trademark of Linear Technology Corp.

Generating CMOS Logic Supply from 2 Mercury Batteries



Supply Current vs Supply Voltage

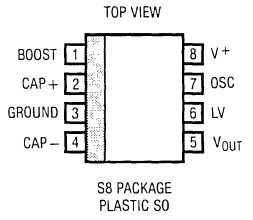


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage 9.5V
Input Voltage on Pins 1, 6 and 7
(Note 2) ..... $-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Current into Pin 6 ..... $20\mu A$
Output Short Circuit Duration
($V^+ \leq 5.5V$) ..... Continuous
Operating Temperature Range.... $-40°C \leq T_A \leq 85°C$
Storage Temperature Range..... $-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec.) .....300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LTC1044CS8
PART MARKING
1044

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, unless otherwise specified.
See LTC1044/7660 data sheet for test circuit.

SYMBOL	PARAMETER	CONDITIONS		LTC1044CS8 MIN	TYP	MAX	UNITS
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7 No Connection			60	200	μA
		$R_L = \infty$, Pins 1 and 7 V = 3V			20		μA
V^+_L	Minimum Supply Voltage	$R_L = 10k$	●	1.5			V
V^+_H	Maximum Supply Voltage	$R_L = 10k$ (Note 3)	●			9	V
R_{OUT}	Output Resistance	$I_L = 200mA$, $f_{OSC} = 5kHz$				100	Ω
			●			130	Ω
		$V^+ = 2V$, $I_L = 3mA$, $f_{OSC} = 1kHz$	●			325	Ω
f_{OSC}	Oscillator Frequency	$C_{OSC} = 1pF$ (Note 4)					
		$V^+ = 5V$	●	5			kHz
		$V^+ = 2V$	●	1			kHz
P_{EFF}	Power Efficiency	$R_L = 5k\Omega$, $f_{OSC} = 5kHz$		95	98		%
V_{OUTEFF}	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9		%
I_{OSC}	Oscillator Sink or Source Current	$V_{OSC} = 0V$ or V^+					
		Pin 1 = 0V	●			3	μA
		Pin 1 = V^+	●			20	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044.

Note 3: The LTC1044 is guaranteed to operate with alkaline, mercury or NiCad 9V batteries, even though the initial battery voltage may be slightly higher than 9.0V.

Note 4: f_{OSC} is tested with $C_{OSC} = 100pF$ to minimize the effects of test fixture capacitance loading. The 1pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

Chopper-Stabilized Operational Amplifier (CSOA™)

FEATURES

- *Guaranteed* Max. Offset 5μV
- *Guaranteed* Max. Offset Drift 0.05μV/°C
- Typ. Offset Drift 0.01μV/°C
- Excellent Long Term Stability 100nV/√Month
- *Guaranteed* Max. Input Bias Current 30pA
- Over Operating Temperature Range
  - *Guaranteed* Min. Gain 120dB
  - *Guaranteed* Min. CMRR 120dB
  - *Guaranteed* Min. PSRR 120dB
- Single Supply Operation 4.75V to 16V (Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V^- with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

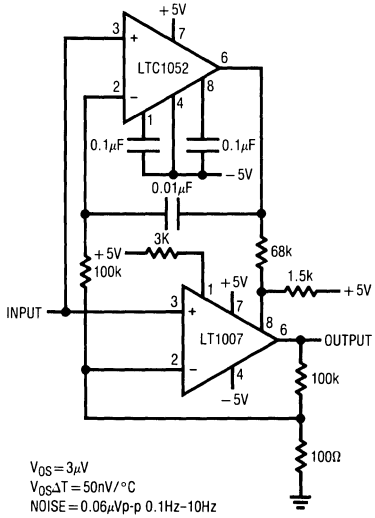
The LTC1052 is a low noise chopper-stabilized op amp (CSOA) manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common-mode voltage are corrected. This, coupled with picoampere input currents, gives this amplifier unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin version to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

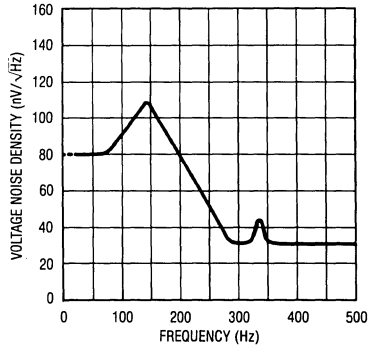
The LTC1052CS is a direct replacement for the ICL7652 in surface mounted packages.

Ultra Low Noise, Low Drift Amplifier



$V_{OS} = 3\mu V$
$V_{OS}\Delta T = 50nV/°C$
NOISE = 0.06μVp-p 0.1Hz–10Hz

LTC1052 Noise Spectrum

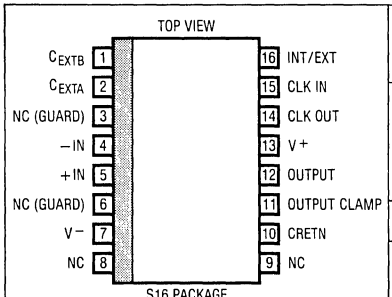


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Total Supply Voltage (V^+ to V^-)..... 18V
Input Voltage..... ($V^+ + 0.3V$) to ($V^- - 0.3V$)
Output Short Circuit Duration..... Indefinite
Operating Temperature Range..... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1052CS
PART MARKING
LTC1052CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, T_A = operating temperature range, test circuit TC1 (Note 6), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1052C MIN	LTC1052C TYP	LTC1052C MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25°C$ (Note 3)			±0.5	±5	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 3)	●		±0.01	±0.05	µV/°C
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Offset Voltage Stability				100		$nV/\sqrt{Month}$
I_{OS}	Input Offset Current	$T_A = 25°C$	 ●		±5	±30 ±350	pA pA
I_B	Input Bias Current	$T_A = 25°C$	 ●		±1	±30 ±175	pA pA
e_{np-p}	Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz, TC3 (Note 6) $R_S = 100\Omega$, DC to 1Hz, TC3 (Note 6)			1.5 0.5		µVp-p µVp-p
i_n	Input Noise Current	f = 10Hz (Note 5)			0.6		$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to +2.7V	●	120	140		dB
PSRR	Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 2.375V$ to $\pm 8V$	●	120	150		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = \pm 4V$	●	120	150		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 10k$ $R_L = 100k$	●	±4.7	±4.85 ±4.95		V V
SR	Slew Rate	$R_L = 10k$, $C_L = 50pF$			4		V/µs
GBW	Gain Bandwidth Product				1.2		MHz
I_S	Supply Current	No Load, $T_A = 25°C$	 ●		1.7	2.0 3.0	mA mA
f_S	Internal Sampling Frequency				330		Hz
	Clamp On Current	$R_L = 100k$	●	25	100		µA
	Clamp Off Current	$-4V < V_{OUT} < +4V$	 ●		10	100 1	pA nA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB}, A_{VOL}, CMRR and PSRR are measured to insure proper operation of the nulling loop to insure meeting the V_{OS} and V_{OS} drift specifications.

Note 4: Output clamp not connected.

Note 5: Current noise is calculated from the formula: $i_n = (2q\,I_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb.

Note 6: For description of test circuits see LTC1052 standard package data sheet.

High Performance Switched Capacitor Universal Filter

FEATURES

- All Filter Parameters *Guaranteed* over Temperature
- Wide Center Frequency Range (0.1Hz to 40kHz)
- Low Noise Wide Dynamic Range
- Operates from ±2.5V Supply up to ±8V
- Low Power Consumption
- *Guaranteed* Clock to Center Frequency Accuracy of 0.8% or Better
- *Guaranteed* Low Offset Voltages over Temperature
- Very Low Center Frequency and Q Tempco
- Clock Input T^2L or CMOS Compatible
- Separate Highpass (or Notch or Allpass), Bandpass, Lowpass Outputs

APPLICATIONS

- Sinewave Oscillators
- Sweepable Bandpass/Notch Filters
- Full Audio Frequency Filters
- Tracking Filters

DESCRIPTION

The LTC1059 consists of a general purpose, high performance, active filter building block and an uncommitted op amp. The filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce notch or highpass or allpass. The center frequency of these functions can be tuned from 0.1Hz to 40kHz and it is dependent on an external clock or an external clock and a resistor ratio. The filter can handle input frequencies up to 100kHz. The uncommitted op amp can be used to obtain additional allpass and notch functions, for gain adjustment or for cascading techniques.

Higher than second order filter functions can be obtained by cascading the LTC1059 with the LTC1060 dual universal filter or LTC1061 triple universal filter. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be formed.

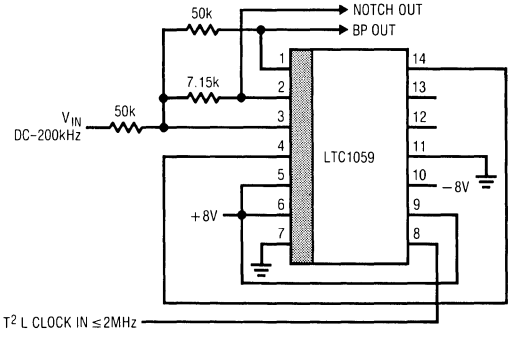
The LTC1059 can be operated with single or dual supplies ranging from ±2.37V to ±8V (or 4.74V to 16V single supply).

The LTC1059 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

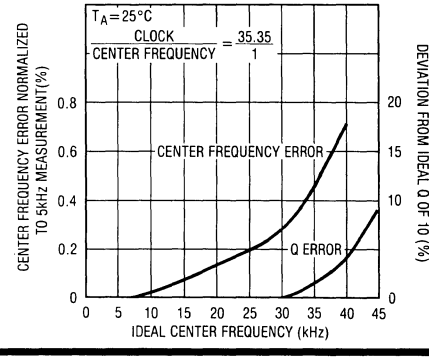
LTCMOS™ is a trademark of Linear Technology Corp.

TYPICAL APPLICATION

Wide Range 2nd Order Bandpass/Notch Filter with Q = 10



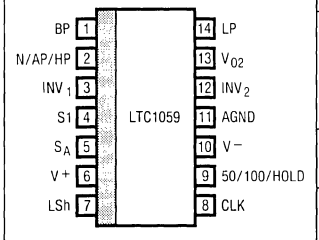
Center Frequency and Q Error



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Operating Temperature Range ..... $-40°C \leq T_A \leq 85°C$
Storage Temperature Range..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10sec) ..... $300°C$

PACKAGE/ORDER INFORMATION



S14 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LTC1059S
PART MARKING
LTC1059S

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, T^2L clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 400kHz$, Mode 1			0.1-40k		Hz
	$f_o \times Q \leq 1.6MHz$, Mode 1			0.1-18k		Hz
	$f_o \times Q \leq 250kHz$, Mode 3, $V_S = \pm 7.5V$			0.1-20k		Hz
	$f_o \times Q \leq 1MHz$, Mode 3, $V_S = \pm 7.5V$			0.1-16k		Hz
Input Frequency Range				0-200k		Hz
Clock to Center Frequency Ratio (Note 1)	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10	●			50 ± 0.8%	
	Mode 1, 100:1, $f_{CLK} = 500kHz$, Q = 10	●			100 ± 0.8%	
Q Accuracy (Note 1)	Mode 1, 50:1 or 100:1, $f_o = 5kHz$ Q = 10	●		±0.5	5	%
f_o Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$			5		ppm/°C
Q Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$, Q = 10			15		ppm/°C
DC Offset V_{OS1} (Note 2)		●		2	15	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ High	●		3	40	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ High	●		6	80	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ Low	●		2	30	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ Low	●		4	60	mV
V_{OS3}	$f_{CLK} = 250kHz$, 50:1	●		2	30	mV
V_{OS3}	$f_{CLK} = 500kHz$, 100:1	●		4	60	mV
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 50kΩ	●		±0.1	2	%
BP Gain Accuracy at f_o	Mode 1, Q = 10, $f_o = 5kHz$			±0.1		%
Clock Feedthrough	$f_{CLK} \leq 1MHz$			10		mV
Max. Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5V$			2		MHz
Power Supply Current				3.5	5.5	mA
		●			7	mA

Note 1: An LTC1059S with improved Q and clock to center frequency ratio accuracy can be made available upon special request.

Note 2: For definition of the DC offset voltages, refer to the LTC1059 data sheet. An LTC1059S with improved DC offset specifications can be made available upon special request.

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range	$f_o \times Q \leq 120kHz$, Mode 1, 50:1 $f_o \times Q \leq 120kHz$, Mode 3, 50:1		0.1-12k 0.1-10k		Hz Hz
Input Frequency Range			60k		Hz
Clock to Center Frequency Ratio	Mode 1, 50:1, $f_{CLK} = 250kHz$, Q = 10 Mode 1, 100:1, $f_{CLK} = 250kHz$, Q = 10		50 ± 0.8% 100 ± 0.8%		
Q Accuracy	Mode 1, $f_{CLK} = 250kHz$, Q = 10 50:1 and 100:1		±2		%
Max. Clock Frequency Power Supply Current			700k 1.5	 2.5	Hz mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			±2.375		±8	V
Voltage Swings	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 14) $R_L = 3.5k$ (Pins 2, 13)	 ●	±3.8 ±3.6	±4.2		V V
Input Offset Voltage		●		1	15	mV
Input Bias Current				3		pA
Output Short Circuit Current Source/Sink	$V_S = \pm 5V$			25/3		mA
DC Open Loop Gain	$V_S = \pm 5V$			80		dB
GBW	$V_S = \pm 5V$			2		MHz
Slew Rate	$V_S = \pm 5V$			7		V/μs

The ● denotes the specifications which apply over the full operating temperature range.

Universal Dual Filter Building Block

FEATURES

- Operates from ±2.5V supply up to ±8V
- Operates up to 30kHz
- Low Power and 88dB Dynamic Range at ±2.5V Supply
- Center Frequency Q Product up to 1.6MHz
- *Guaranteed* Offset Voltages
- *Guaranteed* Clock to Center Frequency Accuracy over Temperature, 0.8% or Better
- *Guaranteed* Q Accuracy over Temperature
- Low Temperature Coefficient of Q and Center Frequency
- Low Crosstalk, 70dB
- Clock Inputs TTL and CMOS Compatible

APPLICATIONS

- Single 5V Supply Medium Frequency Filters
- Very High Q and High Dynamic Range Bandpass, Notch Filters
- Tracking Filters
- Telecom Filters

DESCRIPTION

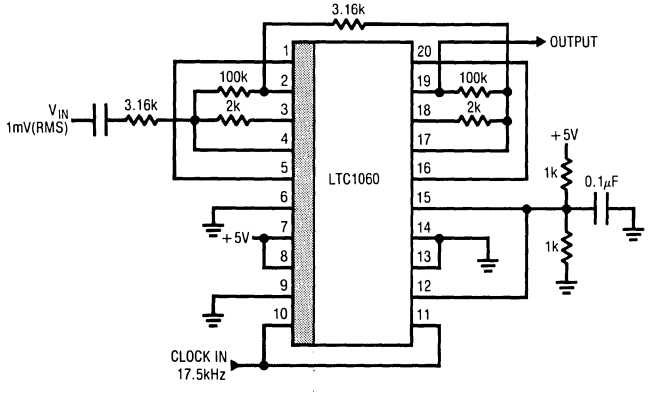
The LTC1060 consists of two high performance, switched capacitor filters. Each filter, together with 2 to 5 resistors, can produce various 2nd order filter functions such as low-pass, bandpass, highpass notch and allpass. The center frequency of these functions can be tuned by an external clock, or by an external clock and resistor ratio. Up to 4th order full biquadratic functions can be achieved by cascading the two filter blocks. Any of the classical filter configurations (like Butterworth, Chebyshev, Bessel, Cauer) can be formed.

The LTC1060 operates with either a single or dual supply from ±2.37V to ±8V. When used with low supply (i.e., single 5V supply), the filter typically consumes 12mW and can operate with center frequencies up to 10kHz. With ±5V supply, the frequency range extends to 30kHz and very high Q values can also be obtained.

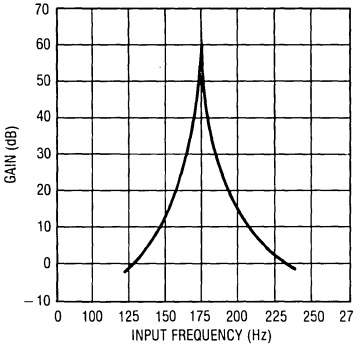
The LTC1060 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process. Because of this, low offsets, high dynamic range, high center frequency Q product and excellent temperature stability are obtained.

LTCMOS™ is a trademark of Linear Technology Corp.

Single 5V, Gain of 1000 4th Order Bandpass Filter



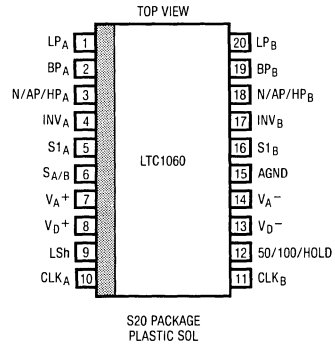
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Operating Temperature Range ..... $-40°C \le T_A \le 85°C$
Storage Temperature Range..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10 sec.)..... $300°C$

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1060S
PART MARKING
LTC1060S

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range	$f_0 \times Q \le 400kHz$, Mode 1			0.1-20k		Hz
	$f_0 \times Q \le 1.6MHz$, Mode 1			0.1-16k		Hz
Clock to Center Frequency Ratio (Note 1)	Mode 1, 50:1, $f_{CLK} = 250kHz$, $Q = 10$	●			$50 \pm 0.8\%$	
	Mode 1, 100:1, $f_{CLK} = 500kHz$, $Q = 10$	●			$100 \pm 0.8\%$	
Q Accuracy (Note 1)	Mode 1, 50:1 or 100:1, $f_0 = 5kHz$					
	$Q = 10$	●		± 0.5	5	%
f_0 Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$			−10		ppm/°C
Q Temperature Coefficient	Mode 1, $f_{CLK} < 500kHz$, $Q = 10$			+20		ppm/°C
DC Offset V_{OS1} (Note 2)		●		2	15	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ High	●		3	40	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ High	●		6	80	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ Low	●		2	30	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ Low	●		4	60	mV
V_{OS3}	$f_{CLK} = 250kHz$, 50:1, $S_{A/B}$ Low	●		2	30	mV
V_{OS3}	$f_{CLK} = 500kHz$, 100:1, $S_{A/B}$ Low	●		4	60	mV
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 50k			± 0.1	2	%
BP Gain Accuracy at f_0	Mode 1, $Q = 10$, $f_0 = 5kHz$			± 0.1		%
Clock Feedthrough	$f_{CLK} \le 1MHz$			10		mV(p-p)
Max. Clock Frequency				1.5		MHz
Power Supply Current			3	5	8	mA
		●			12	mA
Crosstalk				70		dB

Note 1: An LTC1060S with improved Q and clock to center frequency ratio accuracy can be made available upon special request.

Note 2: For definition of the DC offset voltages refer to the LTC1060 data sheet. An LTC1060S with improved DC offset specifications can be made available upon special request.

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25°C$

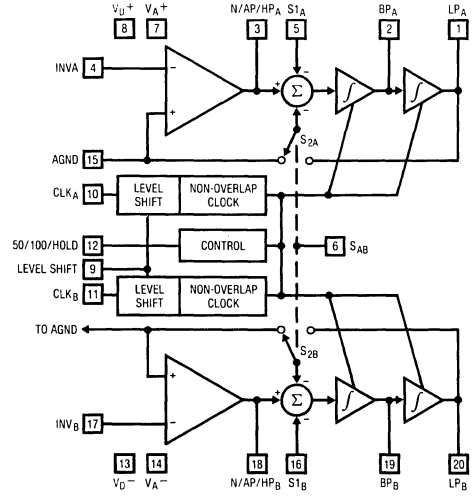
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range	$f_o \times Q \leq 100kHz$			0.1-10k		Hz
Clock to Center Frequency Ratio	Mode 1, 50:1, $f_{CLK} = 250kHz$, $Q = 10$ Mode 1, 100:1, $f_{CLK} = 250kHz$, $Q = 10$			50 ± 0.8% 100 ± 0.8%		
Q Accuracy	Mode 1, $f_o = 2.5kHz$, $Q = 10$ 50:1 and 100:1			± 2		%
Max Clock Frequency				500		kHz
Power Supply Current				2.5	4	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25°C$

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			± 2.37		± 8	V
Voltage Swings	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 19, 20)		± 3.8	± 4		V
	$R_L = 3.5k$ (Pins 3, 18)	●	± 3.6	± 4		V
Output Short Circuit Current	$V_S = \pm 5V$					
Source				25		mA
Sink				3		mA
Op Amp GBW Product	$V_S = \pm 5V$			2		MHz
Op Amp Slew Rate	$V_S = \pm 5V$			7		V/μs
Op Amp DC Open Loop Gain	$R_L = 10k$, $V_S = \pm 5V$			85		dB

The ● denotes the specifications which apply over the full operating temperature range.

BLOCK DIAGRAM



High Performance Triple Universal Filter Building Block

FEATURES

- Up to 6th Order Filter Functions with a Single 20 Pin Surface Mount Package
- Center Frequency Range up to 35kHz
- $f_0 \times Q$ Product Up to 1 MHz
- *Guaranteed* Center Frequency and Q Accuracy Over Temperature
- *Guaranteed* Low Offset Voltages Over Temperature
- 90dB Dynamic Range
- Filter Operates From Single 4.7V Supply and Up to ±8V Supplies
- Low Power
- Clock Inputs T^2L and CMOS Compatible

APPLICATIONS

- High Order, Wide Frequency Range Bandpass, Lowpass, Notch Filters
- Low Power Consumption, Single 5V Supply Clock Tunable Filters
- Tracking Filters

DESCRIPTION

The LTC1061 consists of three high performance, universal filter building blocks. Each filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce highpass or notch or allpass. The center frequency of these functions can be tuned from 0.1Hz to 35kHz and is dependent on an external clock or an external clock and a resistor ratio.

The LTC1061 can be used with single or dual supplies ranging from ±2.37V to ±8V (or 4.74V to 16V). When the filter operates with supplies of ±5V and above, it can handle input frequencies up to 100kHz.

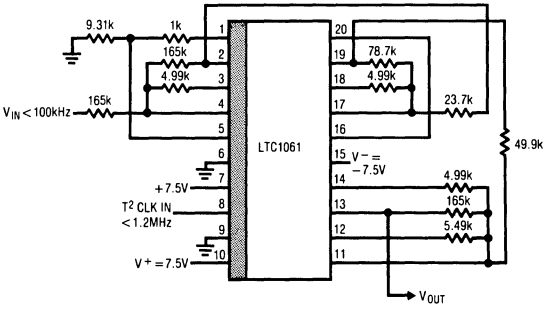
The LTC1061 is compatible with the LTC1059 single universal filter and the LTC1060 dual. Higher than 6th order functions can be obtained by cascading the LTC1061 with the LTC1059 or LTC1060. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be obtained by the appropriate choice of the external resistors.

The LTC1061 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

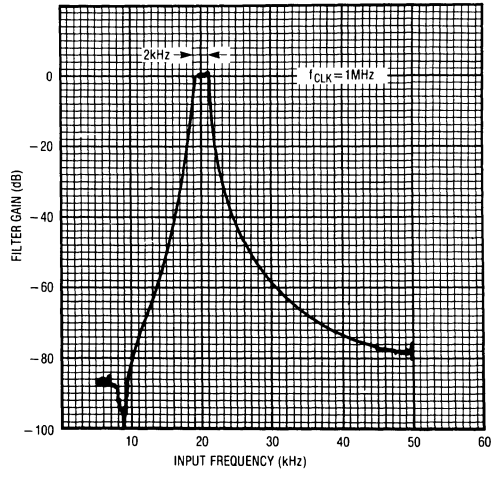
LTCMOS™ is a trademark of Linear Technology Corp.

TYPICAL APPLICATION

6th Order, Clock Tunable, 0.5dB Ripple Chebyshev BP Filter



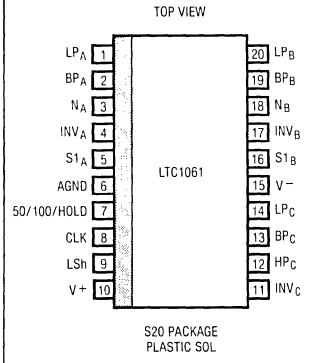
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Operating Temperature Range ..... $-40°C \leq T_A \leq 85°C$
Storage Temperature Range..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10sec)..... $300°C$

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1061S
PART MARKING
LTC1061S

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 175kHz$, Mode 1, $V_S = \pm 7.5V$			0.1-35k		Hz
	$f_o \times Q \leq 1.6MHz$, Mode 1, $V_S = \pm 7.5V$			0.1-25k		Hz
	$f_o \times Q \leq 75kHz$, Mode 3, $V_S = \pm 7.5V$			0.1-25k		Hz
	$f_o \times Q \leq 1MHz$, Mode 3, $V_S = \pm 7.5V$ (Note 1)			0.1-17k		Hz
Input Frequency Range				0-200k		Hz
Clock to Center Frequency Ratio, f_{CLK}/f_o (Note 1)	Sides A, B: Mode 1, R1 = R3 = 50kΩ R2 = 5kΩ, Q = 10, f_{CLK} = 250kHz Pin 7 High. Side C: Mode 3, R1 = R3 = 50k R2 = R4 = 5k, f_{CLK} = 250kHz	●			50 ± 1.2%	
	Same as Above but Pin 7 at Mid-Supplies, f_{CLK} = 500kHz	●			100 ± 1.2%	
Clock to Center Frequency Ratio, Side to Side Matching		●			1.2%	
Q Accuracy (Note 1)	Sides A, B, Mode 1 } 50:1 or 100:1 Side C, Mode 3 } f_o = 5kHz, Q = 10	●		±3	5	%
f_o Temperature Coefficient	Mode 1, 50:1, $f_{CLK} < 300kHz$			±1		ppm/°C
Q Temperature Coefficient	Mode 1, 100:1, $f_{CLK} < 500kHz$			±5		ppm/°C
	Mode 3, $f_{CLK} < 500kHz$			±5		ppm/°C

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Offset Voltage (Note 2)						
V_{OS1}		●		2	15	mV
V_{OS2}	$f_{CLK} = 250kHz$, 50:1	●		3	25	mV
V_{OS2}	$f_{CLK} = 500kHz$, 100:1	●		6	50	mV
V_{OS3}	$f_{CLK} = 250kHz$, 50:1	●		3	25	mV
V_{OS3}	$f_{CLK} = 500kHz$, 100:1	●		6	50	mV
Clock Feedthrough	$f_{CLK} < 1MHz$			0.4		mV_{RMS}
Max. Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5V$			2.5		MHz
Power Supply Current			6	8	12	mA
		●			16	mA

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 120kHz$, Mode 1, 50:1		0.1–12k		Hz
	$f_o \times Q \leq 120kHz$, Mode 3, 50:1		0.1–10k		Hz
Input Frequency Range			0–20k		Hz
Clock to Center Frequency Ratio	50:1, $f_{CLK} = 250kHz$, $Q = 10$				
	Sides A, B: Mode 1				
	Side C: Mode 3		50 ± 1%		
	100:1, $f_{CLK} = 500kHz$, $Q = 10$				
	Sides A, B: Mode 1		100 ± 1%		
	Side C: Mode 3				
Q Accuracy	Same as Above, 100:1 or 50:1		±3		%
Max. Clock Frequency			700k		Hz
Power Supply Current			4.5	6	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			±2.37		±9	V
Voltage Swings	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 13, 14, 19, 20)		±3.8	±4.2		V
	$R_L = 3.5k$ (Pins 3, 12, 18)	●	±3.6			V
Output Short Circuit Current Source/Sink	$V_S = \pm 5V$			40/3		mA
DC Open Loop Gain	$V_S = \pm 5V$, $R_L = 5k$			80		dB
GBW Product	$V_S = \pm 5V$			3		MHz
Slew Rate	$V_S = \pm 5V$			7		V/μs

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: An LTC1061S with improved Q and clock to center frequency ratio accuracy can be made available upon special request.

Note 2: For definition of the DC offset voltages refer to the LTC1061 data sheet. An LTC1061S with improved DC offset specifications can be made available upon special request.

5th Order Low Pass Filter

FEATURES

- Lowpass Filter with No DC Error
- Low Passband Noise
- Operates DC to 20kHz
- Operates on a Single 5V Supply or Up to ±8V
- 5th Order Filter
- Maximally Flat Response
- Internal or External Clock
- Cascadable for Faster Rolloff
- Buffer Available

APPLICATIONS

- 60Hz Lowpass Filters
- Anti-Aliasing Filter
- Low Level Filtering
- Rolling Off AC Signals from High DC Voltages
- Digital Voltmeters
- Scales
- Strain Gauges

DESCRIPTION

The LTC1062 is a 5th order all pole maximally flat lowpass filter with no DC error. Its unusual architecture puts the filter outside the DC path so DC offset and low frequency noise problems are eliminated. This makes the LTC1062 very useful for lowpass filters where DC accuracy is important.

The filter input and output are simultaneously taken across an external resistor. The LTC1062 is coupled to the signal through an external capacitor. This R,C reacts with the internal switched capacitor network to form a 5th order rolloff at the output.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff frequency ratio is typically 100:1, allowing the clock ripple to be easily removed.

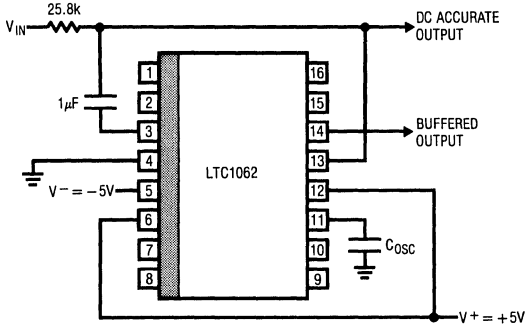
Two LTC1062s can be cascaded to form a 10th order quasi max flat lowpass filter. The device can be operated with single or dual supplies ranging from ±2.5V to ±9V.

The LTC1062 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

LTCMOS™ is a trademark of Linear Technology Corp.

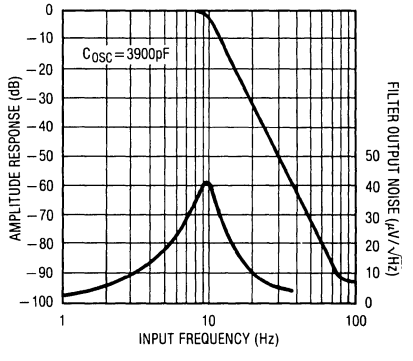
TYPICAL APPLICATION

10Hz 5th Order Butterworth Lowpass Filter



NOTE: TO ADJUST OSCILLATOR FREQUENCY, USE A 6800pF CAPACITOR IN SERIES WITH A 50k POT FROM PIN 5 TO GROUND.

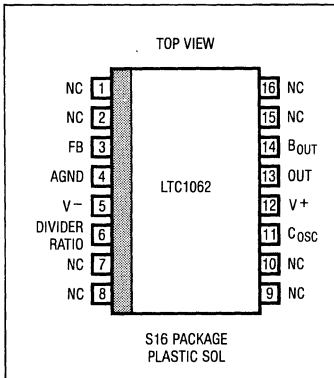
Filter Amplitude Response and Noise



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage at Any Pin ..... $V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$
Operating Temperature Range ..... $-40°C \leq T_A \leq 85°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature Range (Soldering, 10 sec.) ..... $300°C$

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1062CS
PART MARKING
LTC1062CS

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$ unless otherwise specified, AC output measured at pin 7

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Current	C_{OSC} (Pin 5 to V^-) = 100 pF	●		4.5	7 10	mA mA
Input Frequency Range				0-20k		Hz
Filter Gain at $f_{IN} = 0$	f_{CLK} = 100kHz, Pin 4 at V^+			0		dB
$f_{IN} = 0.5f_C$ (Note 1)	C = 0.01μF, R = 25.78k			–0.02	–0.3	dB
$f_{IN} = f_C$		●	–2	–3		dB
$f_{IN} = 2f_C$		●	–28	–30		dB
$f_{IN} = 4f_C$		●	–54	–60		dB
Clock to Cutoff Frequency Ratio, f_{CLK}/f_C	Same as above			100 ± 1		%
Filter Gain at f_{IN} = 16kHz	f_{CLK} = 400kHz, Pin 4 at V^+ C = 0.01μF, R = 6.5k	●	–46	–52		dB
f_{CLK}/f_C Tempco	Same as above			10		ppm/°C
Filter Output (Pin 7) DC Swing	Pin 7 bufffered with an external op amp	●	±3.5	±3.8		V
Clock Feedthrough				10		mVp-p
Internal Buffer						
Bias Current				2	50	pA
Bias Current		●		170	1000	pA
Offset Voltage				2	20	mV
Voltage Swing	R1 = 20kΩ	●	±3.5	±3.8		V
Short Circuit Current Source/Sink				40/3		mA
Clock (Note 3)						
Internal Oscillator Frequency	C_{OSC} (Pin 5 to V^-) = 100pF C_{OSC} (Pin 5 to V^-) = 100pF	 ●	25 15	32	50 65	kHz kHz
Max Clock Frequency				4		MHz
Pin 5 Source or Sink Current		●		40	80	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: f_C is the frequency where the gain is –3dB with respect to the input signal.

Note 2: The LTC1062C operates from $-40°C \leq T_A \leq 85°C$.

Note 3: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+, ratio = 1; when pin 4 = GND, ratio = 2; when pin 4 = V^-, ratio = 4.

Precision Operational Amplifier

FEATURES

- *Guaranteed* 150μV *max.* Offset Voltage
- *Guaranteed* 1.8μV/°C *max.* Offset Voltage Drift with Temperature
- *Excellent* 2.0μV/Month *max.* Long Term Stability
- *Guaranteed* 0.65μVp-p *max.* Noise
- *Guaranteed* 7nA *max.* Input Bias Current

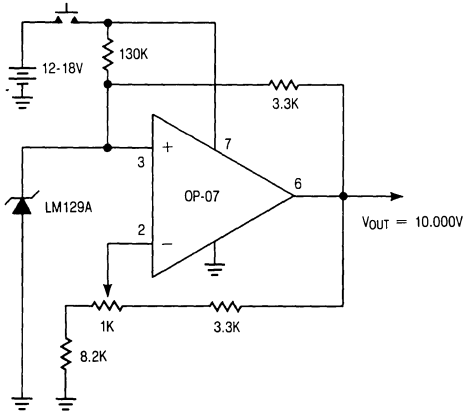
APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

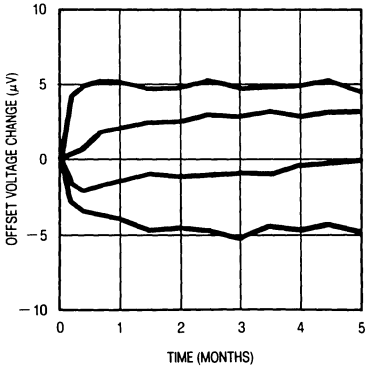
The OP-07 offers excellent performance in applications requiring low offset voltage, low drift with time and temperature and very low noise. Linear's OP-07 is interchangeable with many of the precision op amp device types. The OP-07 also offers a wide input voltage range, high common-mode rejection and low input bias current. These features result in optimum performance for small signal level and low frequency applications. Use of advanced design, processing and testing techniques make Linear's OP-07 a superior choice over similar products. A buffered reference application is shown below. For single op amp applications requiring higher performance in the SO package, see the LT1001CS8.

Precision Buffered Single Supply Reference



The OP-07 contributes less than 5% of the total drift with temperature, noise and long term drift of the reference application.

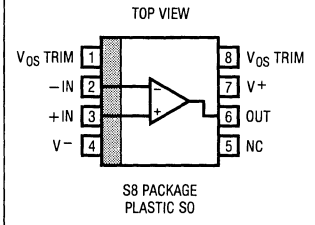
Long Term Stability of Four Representative Units



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
OP-07CS8
PART MARKING
OP07CS8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07CS8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		60	150	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.4	2.0	µV/Month
I_{OS}	Input Offset Current			0.8	6.0	nA
I_B	Input Bias Current			±1.8	±7.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.65	µVp-p
	Input Noise Voltage Density	f_O = 10Hz f_O = 100Hz (Note 2) f_O = 1000Hz		10.5 10.2 9.8	20.0 13.5 11.5	nV/√Hz nV/√Hz nV/√Hz
I_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		15	35	pAp-p
	Input Noise Current Density	f_O = 10Hz f_O = 100Hz (Note 2) f_O = 1000Hz		0.32 0.15 0.13	0.90 0.27 0.18	pA/√Hz pA/√Hz pA/√Hz
R_{in}	Input Resistance Differential Mode	(Note 4)	8	33		MΩ
	Input Resistance Common-Mode			120		GΩ
	Input Voltage Range		±13.0	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	100	120		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	90	104		dB
A_{VOL}	Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V R_L = 500Ω, V_O = ±0.5V V_S = ±3V (Note 4)	120 100	400 400		V/mV V/mV
V_O	Maximum Output Voltage Swing	R_L = 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±12.5 ±11.5	±13.0 ±12.8 ±12.0		V V V
SR	Slewing Rate	R_L ≥ 2kΩ (Note 2)	0.1	0.25		V/µs
GBW	Closed Loop Bandwidth	A_{VOL} = +1 (Note 2)	0.4	0.6		MHz
Z_o	Open Loop Output Impedance	V_O = 0, I_o = 0, f = 10Hz		60		Ω
P_d	Power Dissipation	V_S = ±15V V_S = ±3V		80 4	150 8	mW mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4		mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0°C \leq T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-07CS8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		85	250	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	 Null Pot = 20kΩ (Note 2)	●		 0.5 0.4	 1.8 1.6	 μV/°C μV/°C
I_{OS}	Input Offset Current		●		1.6	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		12	50	pA/°C
I_B	Input Bias Current		●		±2.2	±9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		18	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	97	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	86	100		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	100	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±11.0	±12.6		V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Offset voltage is measured with high speed test equipment, approximately 1 second after power is applied.

Note 2: This parameter is tested on a sample basis only.

Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.

Note 4: This parameter is guaranteed by design.

SG3524S

Regulating Pulse Width Modulator

FEATURES

- ±5% Typ. Oscillator Tolerance
- 20mV/1000 Hrs Typ. Long Term Stability
- Interchangeable with all SG3524 or LM3524 Devices
- Operates Above 100kHz

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Off-Line Power Converters

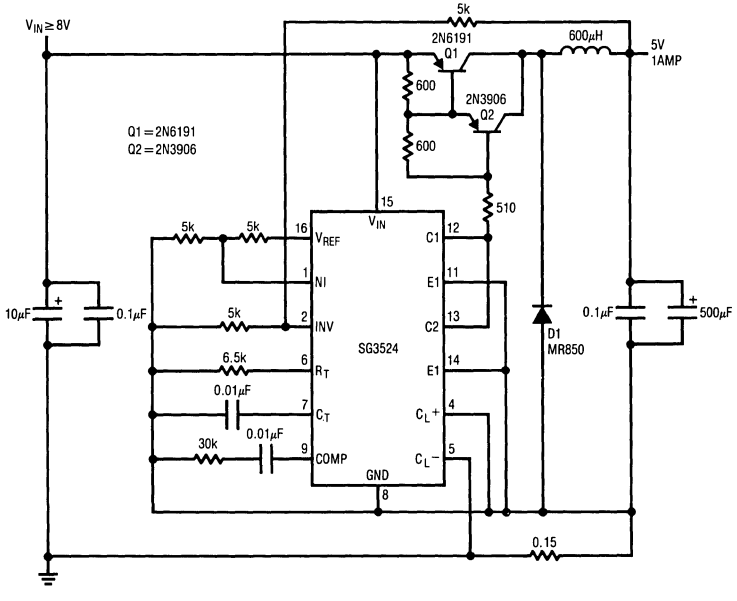
DESCRIPTION

The SG3524 PWM switching regulator control circuit contains all the essential circuitry to implement single-ended or push-pull switching regulators. Included on the circuit are oscillator, voltage reference, a pulse width modulator, error amplifier, overload protection circuitry and output drivers.

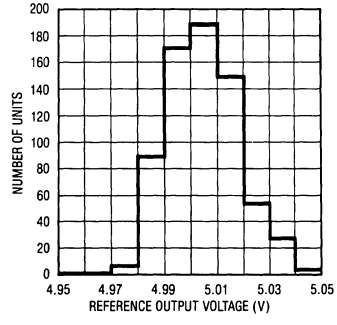
Although pin-for-pin and functionally compatible with industry standard 3524 devices, Linear Technology has incorporated several improvements in the design of the 3524. A subsurface zener reference has been used to provide excellent stability with time and the reference is trimmed at the wafer level.

Linear Technology Corporation's advanced processing, design and passivation techniques make the SG3524 a superior and more reliable choice over previous devices.

5V, 1 Amp Regulator



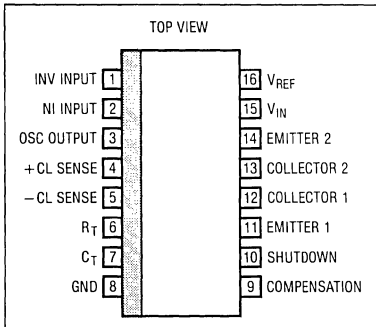
Distribution of Reference Output Voltage



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Reference Output Current 50mA
Output Current (Each Output) 100mA
Oscillator Charging Current (Pin 6 or 7) 5mA
Internal Power Dissipation (Note 1) 1W
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
SG3524S
PART MARKING
SG3524S

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		SG3524 MIN	SG3524 TYP	SG3524 MAX	UNITS
Reference Section:						
Output Voltage		●	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8V to 40V	●		10	30	mV
Load Regulation	I_L = 0mA to 20mA	●		20	50	mV
Ripple Rejection	f = 120Hz			66		dB
Short Circuit Current Limit	V_{REF} = 0			100		mA
Temperature Stability		●		0.3	1	%
Long Term Stability				20		mV/$\sqrt{khr}$
Oscillator Section:						
Maximum Frequency	C_T = 0.001μF, R_T = 2kΩ	●		300		kHz
Initial Accuracy	R_T and C_T Constant			5		%
Voltage Stability	V_{IN} = 8V to 40V				1	%
Temperature Stability	Note 3	●		2		%
Output Amplitude	Pin 3			3.5		V
Output Pulse Width	C_T = 0.01μF, T_A = 25°C			0.5		μs
Error Amplifier Section:						
Input Offset Voltage	V_{CM} = 2.5V	●		2	10	mV
Input Bias Current	V_{CM} = 2.5V	●		2	10	μA
Open Loop Voltage Gain		●	60	80		dB
Common-Mode Voltage			1.8		3.4	V
Common-Mode Rejection Ratio				70		dB
Small Signal Bandwidth	A_V = 0dB			3		MHz
Output Voltage			0.5		3.8	V
Comparator Section:						
Duty Cycle	% Each Output On	●	0		45	%
Input Threshold	Zero Duty Cycle	●		1		V
Input Threshold	Max Duty Cycle	●		3.5		V
Input Bias Current		●		1		μA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		SG3524 MIN	SG3524 TYP	SG3524 MAX	UNITS
Current Limiting Section:						
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out		180	200	220	mV
Sense Voltage T.C.		●		0.2		mV/°C
Common-Mode Voltage		●	–1		1	V
Output Section: (Each Output)						
Collector-Emitter Voltage		●	40			V
Collector Leakage Current	V_{CE} = 40V	●		0.1	50	μA
Saturation Voltage	I_C = 50mA	●		1	2	V
Emitter Output Voltage	V_{IN} = 20V	●	17	18		V
Rise Time	R_C = 2kΩ			0.2		μs
Fall Time	R_C = 2kΩ			0.1		μs
Total Standby Current:	V_{IN} = 40V (Note 4)	●		8	10	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: For operating at elevated temperatures, the device in the SO package must be derated at 100°C/W to a maximum junction temperature of 115°C.

Note 2: These specifications apply for V_{IN} = 20V, f = 20kHz. T_A = 25°C unless otherwise noted.

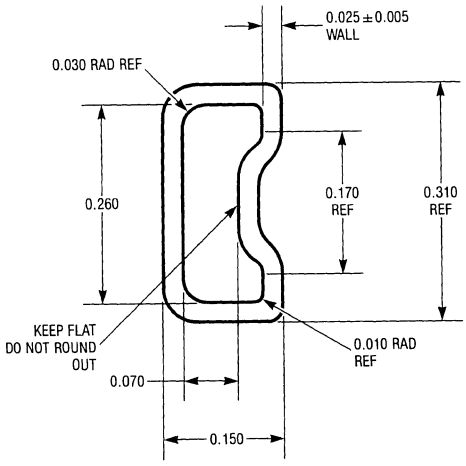
Note 3: Although many manufacturers specify a maximum specification of 2%, Linear Technology's experience is that this specification is not being presently met by other manufacturers. Linear Technology's basic design, although improved, is essentially identical to other manufacturer's devices. Linear Technology is, however, unwilling to place a maximum specification on its data sheet which cannot be met or guaranteed.

Note 4: Standby current does not include the oscillator charging current, error and current limit dividers, and the outputs are open circuit.

Linear Technology Corp. packs their SO and SOL products in either conductive plastic tubes or tape and reel, depending on customer preference. Plastic tubes are manufactured to LTC specifications, while tape and reel packing follows EIA specification 481-A, and is an extra cost item. The following pages describe and detail these packing methods.

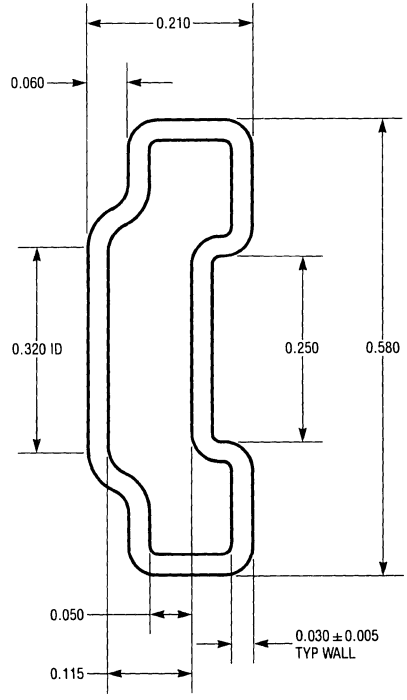
PLASTIC TUBE SPECIFICATIONS

SO Package Shipping Tube



Length: 20.50 $^{+1/16}_{-1/32}$ inches

SOL Package Shipping Tube



Length: 20.75 $^{+1/32}_{-1/16}$ inches

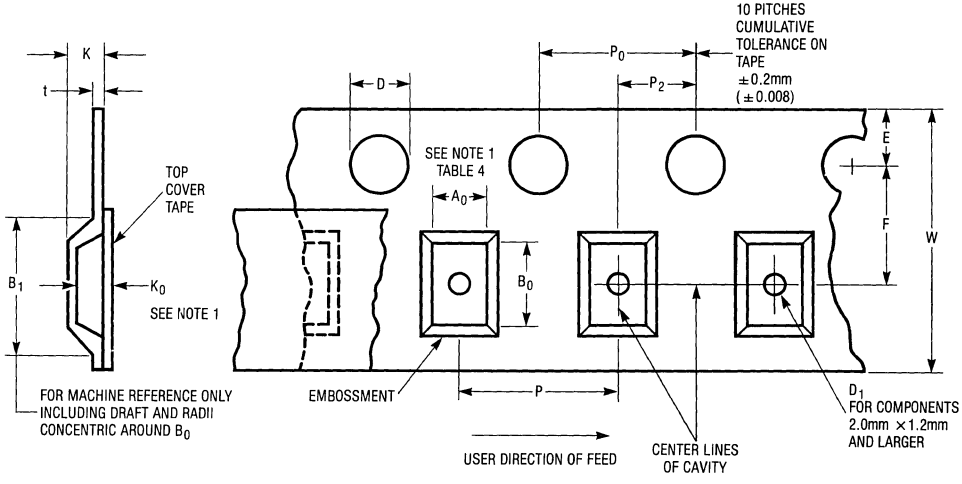
Note 1: Tolerances: ±0.010 unless otherwise specified.

Note 2: Material: anti-static treated rigid transparent PVC or rigid black conductive.

Note 3: Printing: "LTC logo, Linear Technology Corp., Antistatic" on top side of tube.

TAPE AND REEL SPECIFICATIONS

Embossed Carrier Dimensions (12, 16, 24mm Tape Only)



Embossed Tape—Constant Dimensions

Tape Size	D	E	P_0	t (Max.)	A_0 B_0 K_0
12, 16, 24mm	1.5 +0.10 −0.0 (0.059 +0.004 −0.0)	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	0.400 (0.016)	See Note 1

Embossed Tape—Variable Dimensions

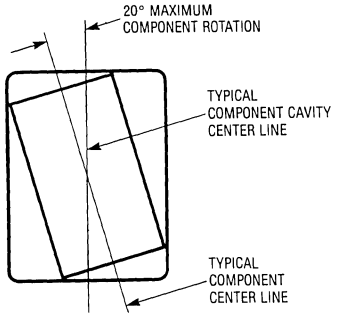
Tape Size	B_1 Max.	D_1 Min.	F	K Max.	P_2	R Min.	W	P (SO)	P (SOL)
12mm	8.2 (0.323)	1.5 (0.059)	5.5 ± 0.05 (0.217 ± 0.002)	4.5 (0.177)	2.0 ± 0.05 (0.079 ± 0.002)	30 (1.181)	12.0 ± 0.30 (0.472 ± 0.012)	8.0 ± 0.10 (0.315 ± 0.04)	12.0 ± 0.10 (0.472 ± 0.004)
16mm	12.1 (0.476)		7.5 ± 0.10 (0.295 ± 0.004)	6.5 (0.256)	2.0 ± 0.10 (0.079 ± 0.004)	40 (1.575)	16 ± 0.30 (0.630 ± 0.012)	8.0 ± 0.10 (0.315 ± 0.04)	
24mm	20.1 (0.791)		11.5 ± 0.10 (0.453 ± 0.004)			50 (1.969)	24 ± 0.30 (0.945 ± 0.012)		

Note 1: A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape and 0.05 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see Component Rotation, page 65.

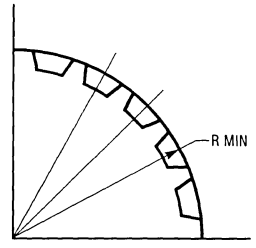
Note 2: Tape and components shall pass around radius "R" without damage.

TAPE AND REEL SPECIFICATIONS

Component Rotation

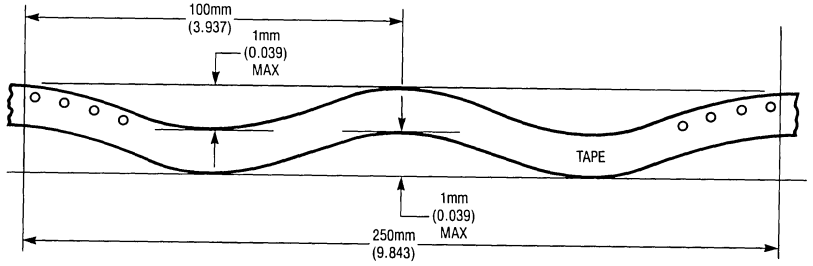


Bending Radius



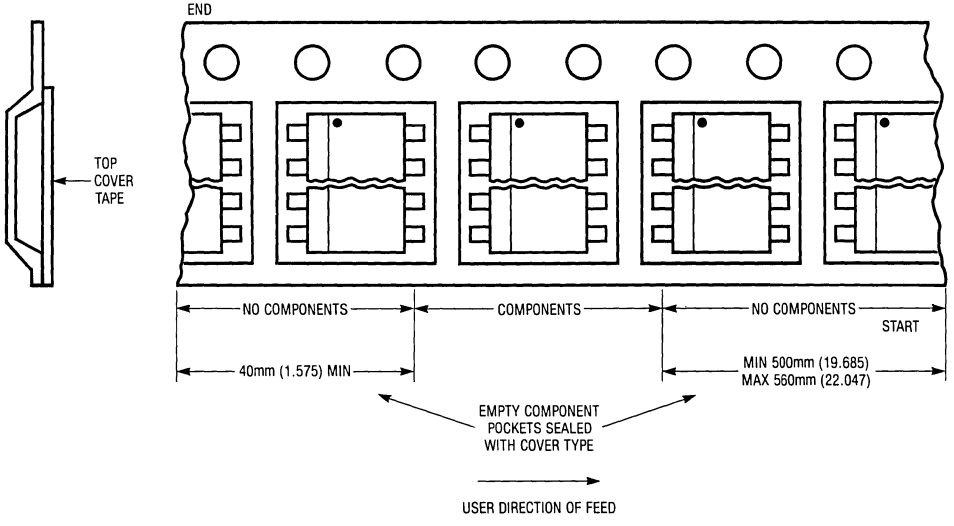
BENDING RADIUS
SEE NOTE 2, PAGE 64

Tape Camber (Top View)



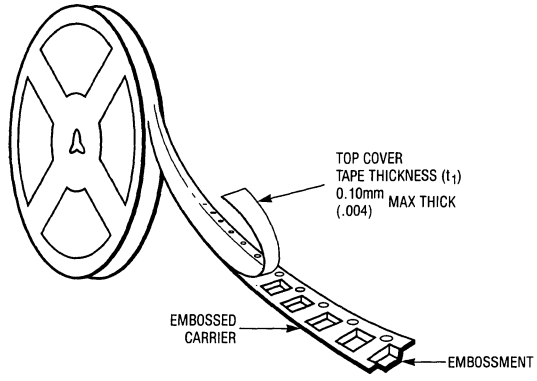
Allowable camber to be 1mm/100mm nonaccumulative over 250mm

Tape Leader (Start/End) Specification

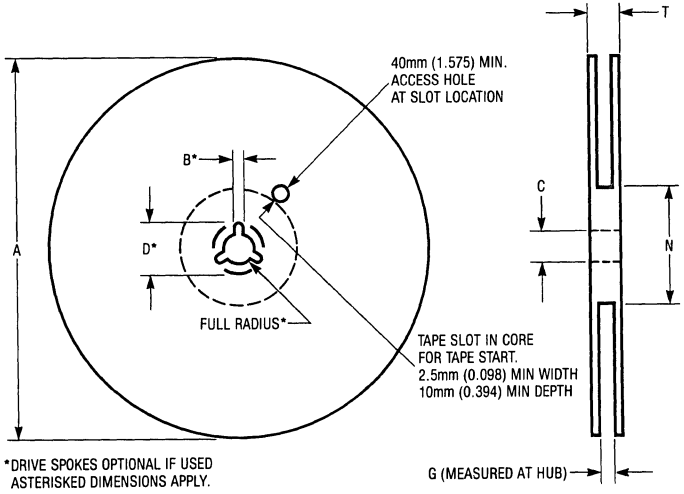


REEL DIMENSIONS

Direction of Feed



Reel Dimensions



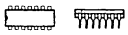
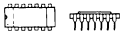
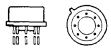
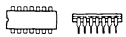
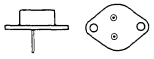
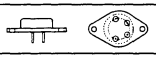
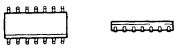
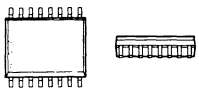
Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
12mm	330 (12.992)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$12.4^{+2.0}_{-0.0}$ $\left(0.488^{+0.078}_{-0.0}\right)$	18.4 (0.724)
16mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$16.4^{+2.0}_{-0.00}$ $\left(0.646^{+0.078}_{-0.00}\right)$	22.4 (0.882)
24mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$24.4^{+2.0}_{-0.00}$ $\left(0.961^{+0.078}_{-0.00}\right)$	30.4 (1.197)

*Metric dimensions will govern.
English measurements rounded and for reference only.

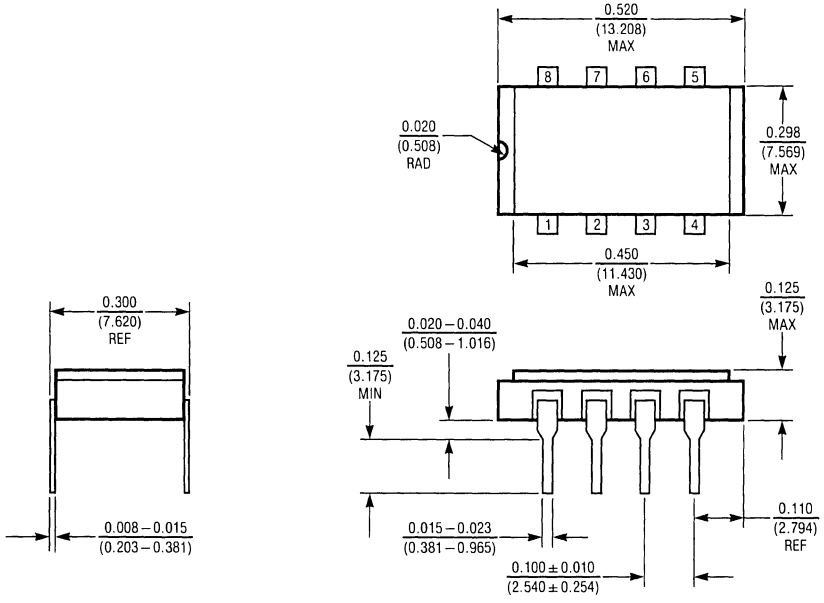
SECTION 12— PACKAGE DIMENSIONS

SECTION 12—PACKAGE DIMENSIONS

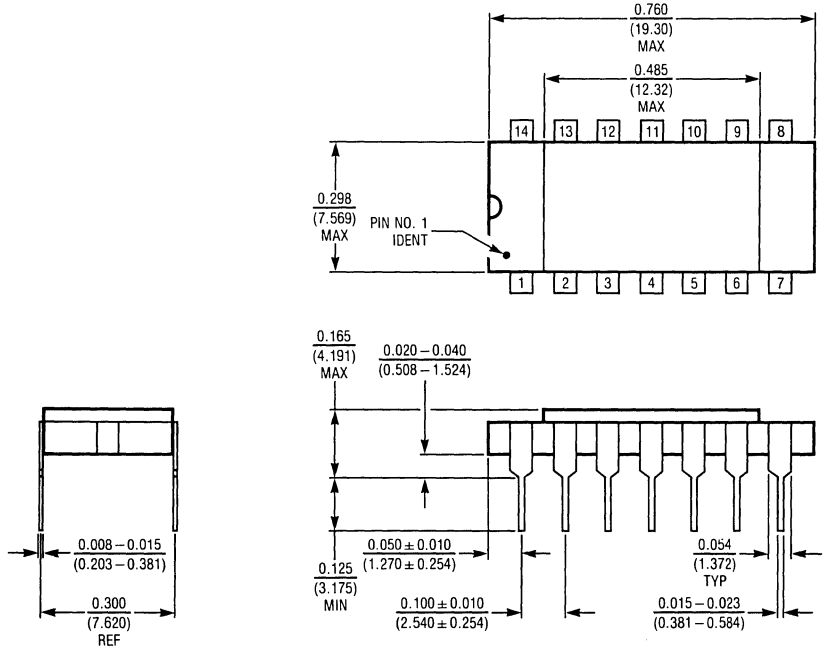
PACKAGE CROSS REFERENCE

	LTC	NSC	SIG	FSC	MOT	TI	SG	AMD	RAYTH	PMI
 Plastic DIP 8 Lead	N-8	N N-8	N	T	P1	P	M	P-8	P, NB	P
 Plastic DIP 14, 16, 18 and 20 Lead	N	N N-14	N	P	P2	N NE NG	N	P-14 P-16	P, N	P
 TO-220 3 Lead	T	T	—	U	T	KC	P	—	—	—
 TO-220 5 Lead	T	T	—	U	—	—	P	—	—	—
 Side Brazed Hermetic DIP 8 Lead	D-8	D	I	D	L	—	—	D-8	—	—
 Side Brazed Hermetic DIP 14, 16, 18 and 20 Lead	D	D	I	D	L	—	—	D-14 D-16 D-18	—	YB QB XB
 TO-92	Z	Z	—	W	P	LP	—	—	—	—
 TO-5, TO-39, TO-96 TO-99, TO-100 and TO-101	H	H	—	H	G H	—	T	H	T H	H J K
 Ceramic DIP 8 Lead	J-8	J J-8	F	R	U	JG	Y	D-8	DE	Z
 Ceramic DIP 14, 16, 18 and 20 Lead	J	J J-14	F	D	L	J	J	D-14 D-16	DB DC J	Y Q X
 TO-3 (Steel)	K	K Steel	—	K	K	—	K	—	—	—
(Aluminum)	—	K	—	K	K	—	—	—	—	—
 TO-3 4 Lead	K	K	—	K	—	—	K	—	—	—
 TO-46 2, 3, 4 Lead	H	H	—	—	—	—	T	—	—	H J K
TO-52 3 Lead										
 TO-247 3 Lead	P	—	—	—	—	—	—	—	—	—
 Plastic SO 8 Lead	S-8	M	D	—	D	D	—	—	—	—
 Plastic SO 14, 16 Lead	S	M	D	—	D	D	—	—	—	—
 Plastic SOL 16, 18, 20 Lead	S	M	D	—	D	D	—	—	—	—
PROPRIETARY DEVICE PREFIXES	LT LTC	LF LP LH MF LM	NE SE	µA	MC	TL	SG	AM	RM RC	OP REF CMP

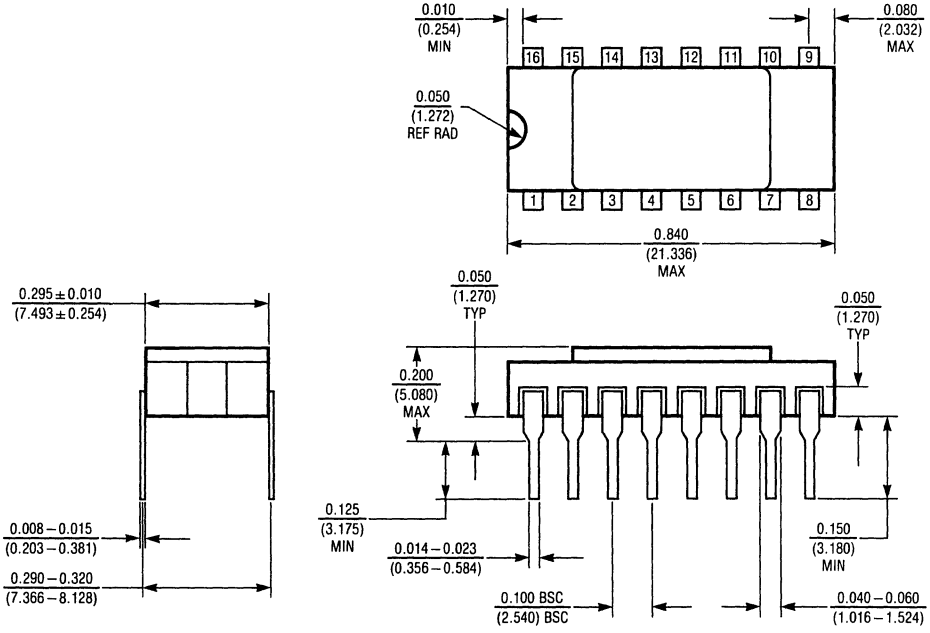
D Package
8 Lead Sidebrazed



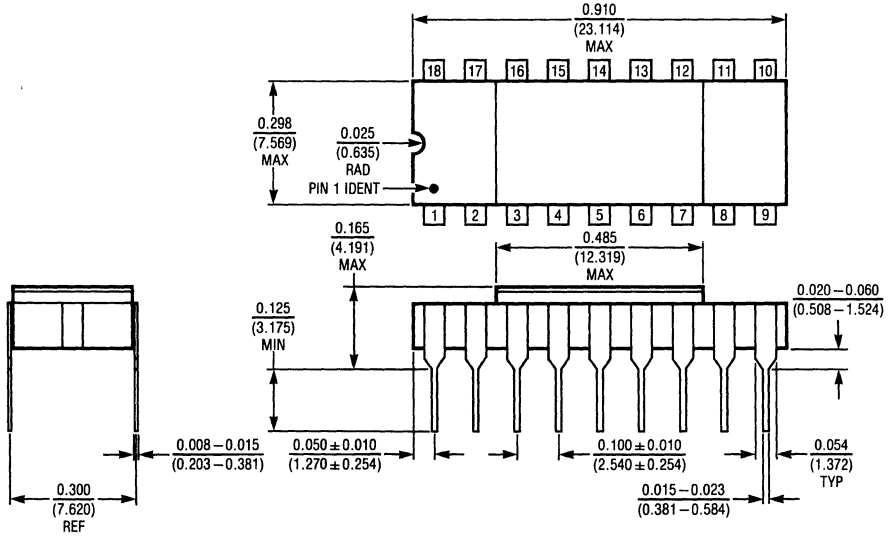
D Package
14 Lead Sidebrazed



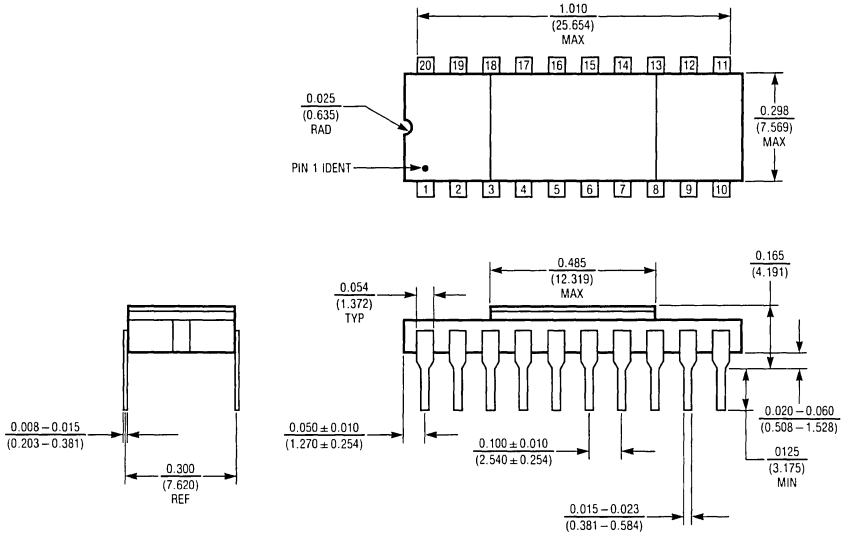
D Package
16 Lead Sidebrazed



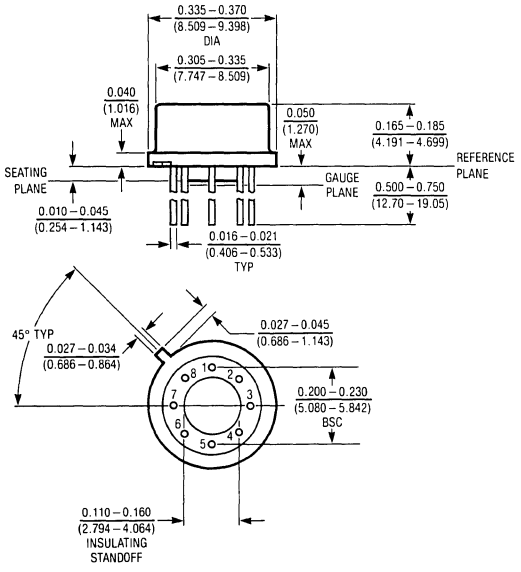
D Package
18 Lead Sidebrazed



D Package
20 Lead Sidebrazed

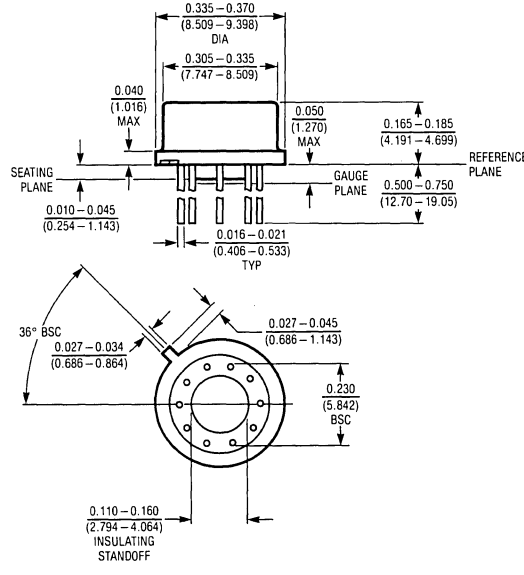


H Package
8 Lead TO-5 Metal Can



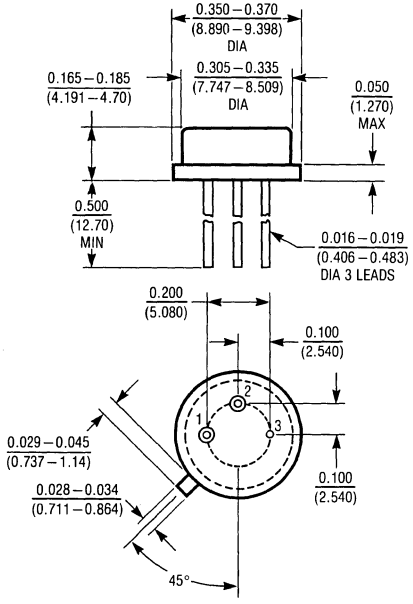
NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

H Package
10 Lead TO-5 Metal Can

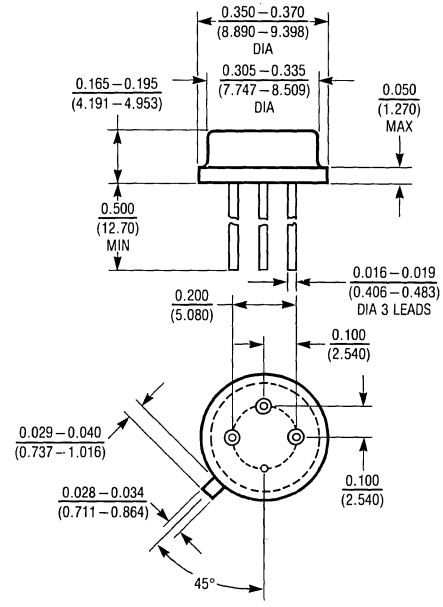


NOTE:
1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

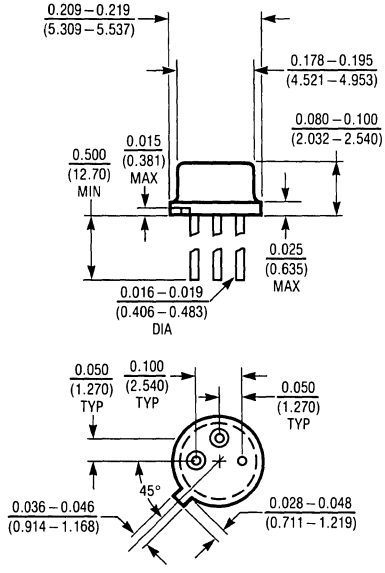
H Package
3 Lead TO-39 Metal Can



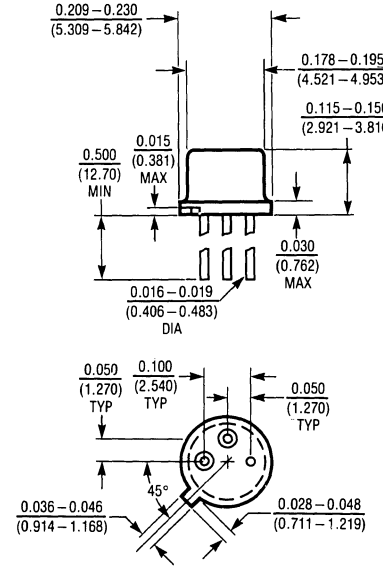
H Package
4 Lead TO-39 Metal Can



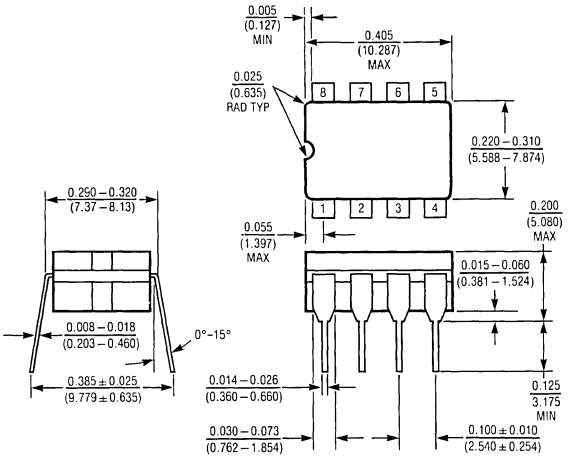
H Package
3 Lead TO-46 Metal Can



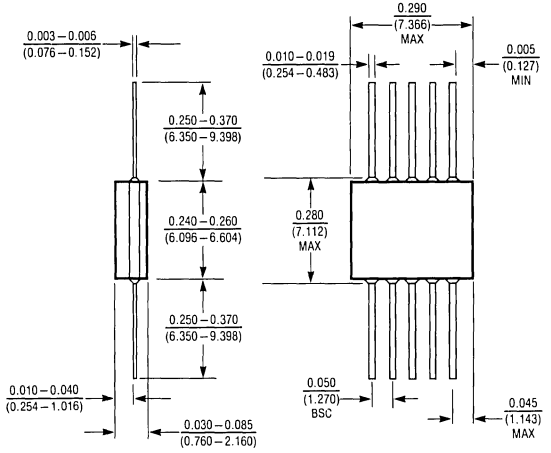
H Package
3-Lead TO-52 Metal Can



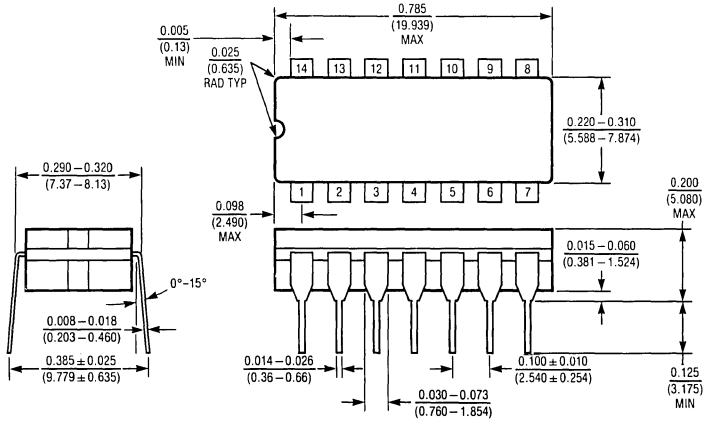
J Package
8 Lead Cerdip



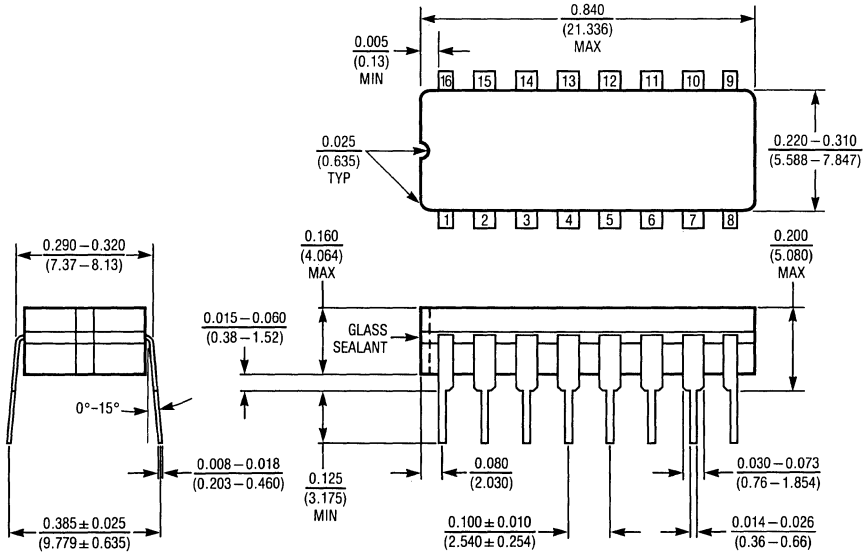
J Package
10 Lead Cerpac



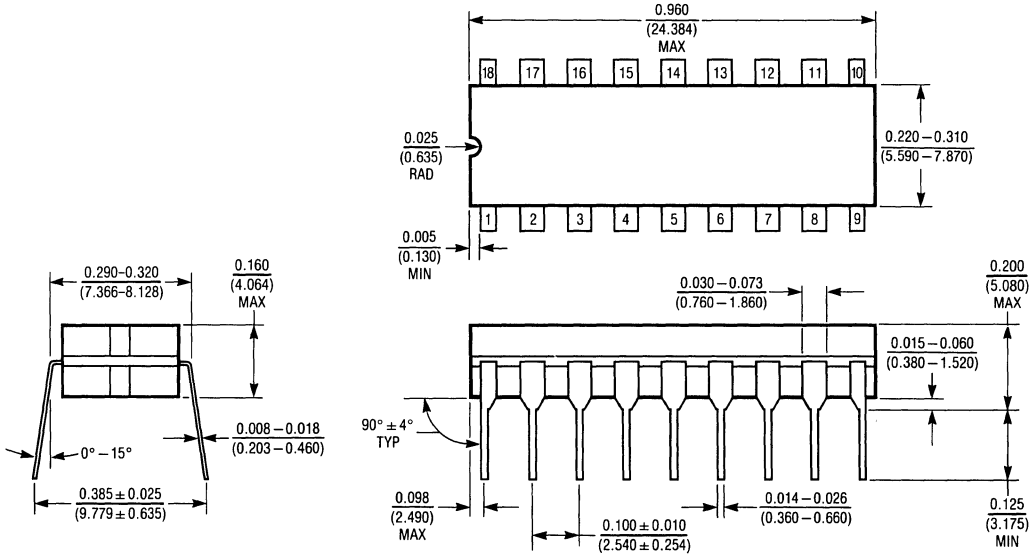
J Package
14 Lead Cerdip



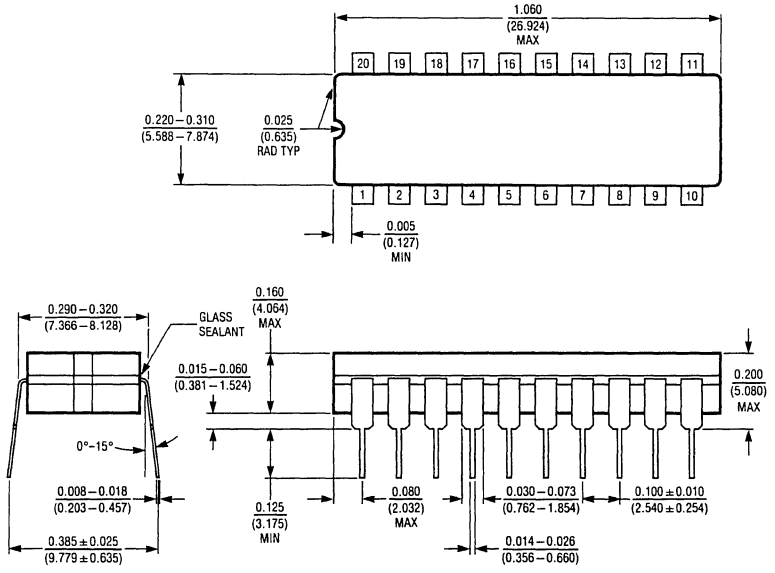
J Package
16 Lead Cerdip



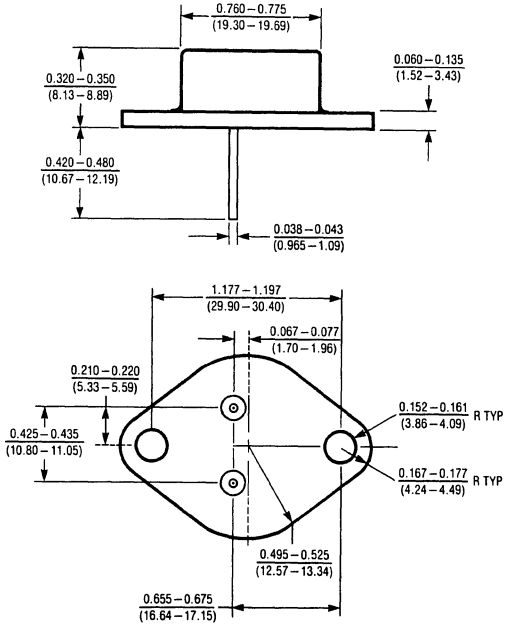
J Package
18 Lead Cerdip



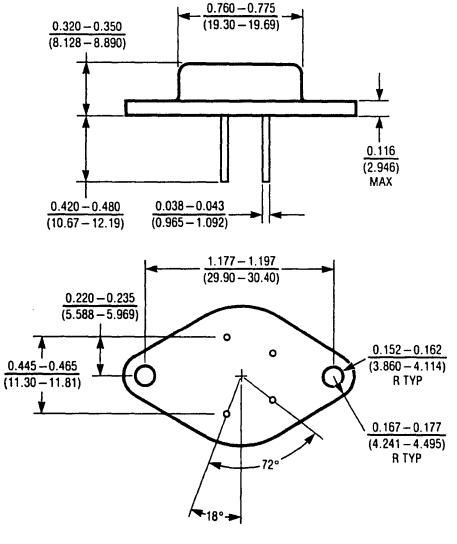
J Package
20 Lead Cerdip



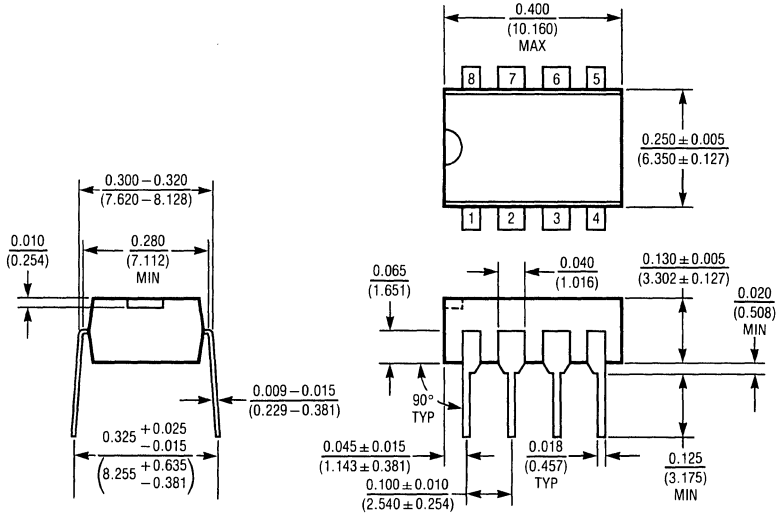
K Package
2 Lead TO-3 Metal Can



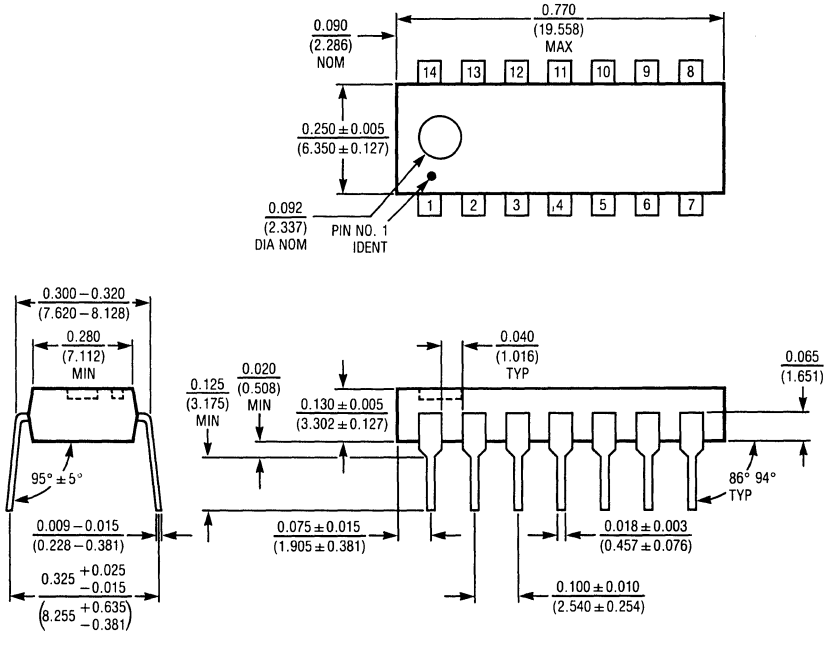
K Package
4 Lead TO-3 Metal Can



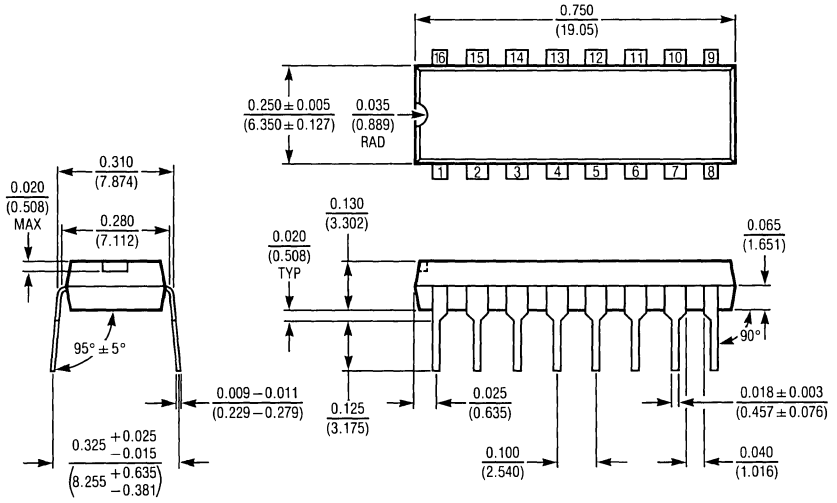
N Package
8 Lead Molded DIP



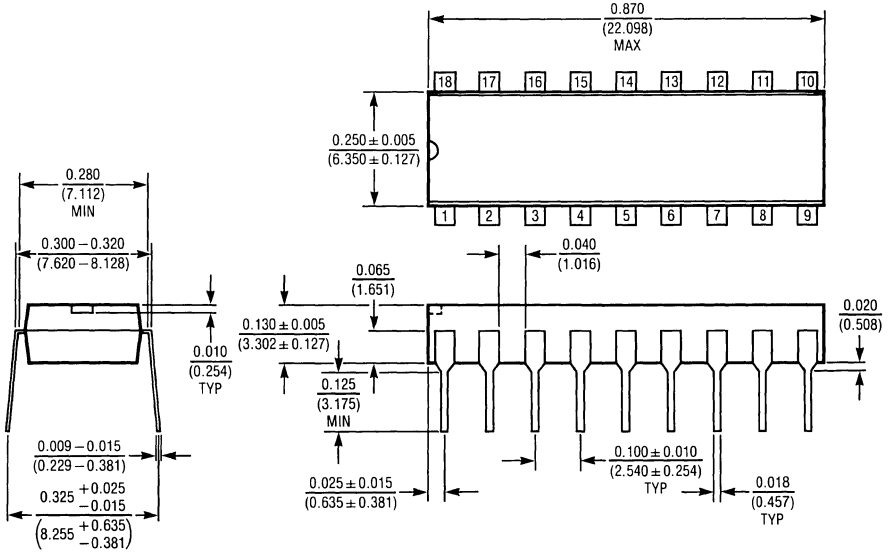
N Package
14 Lead Molded DIP



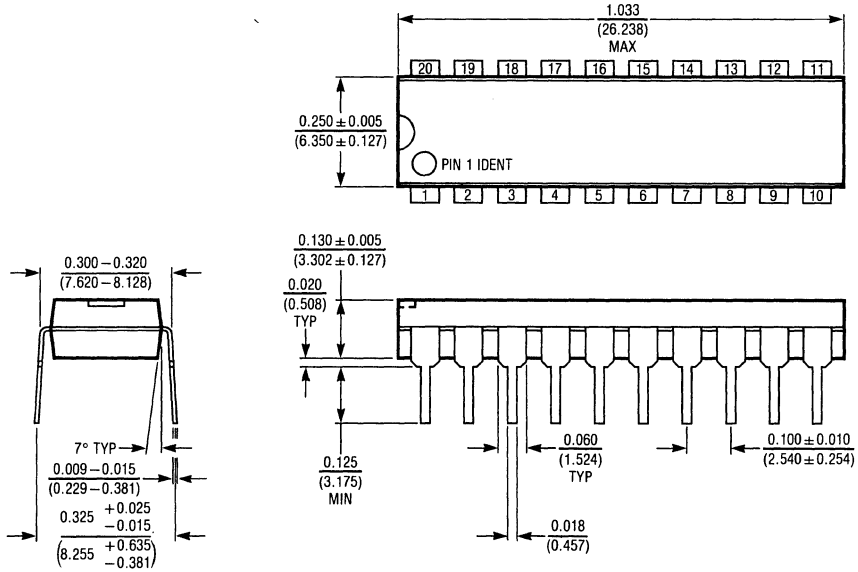
N Package
16 Lead Molded DIP



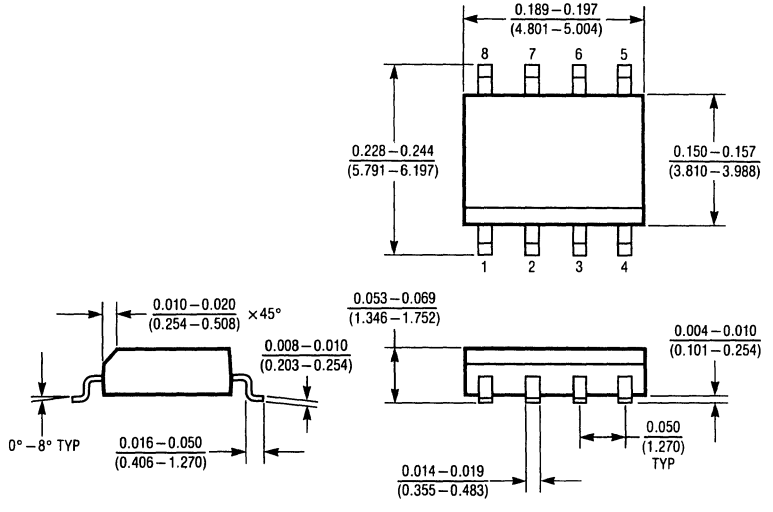
N Package
18 Lead Molded DIP



N Package
20 Lead Molded DIP

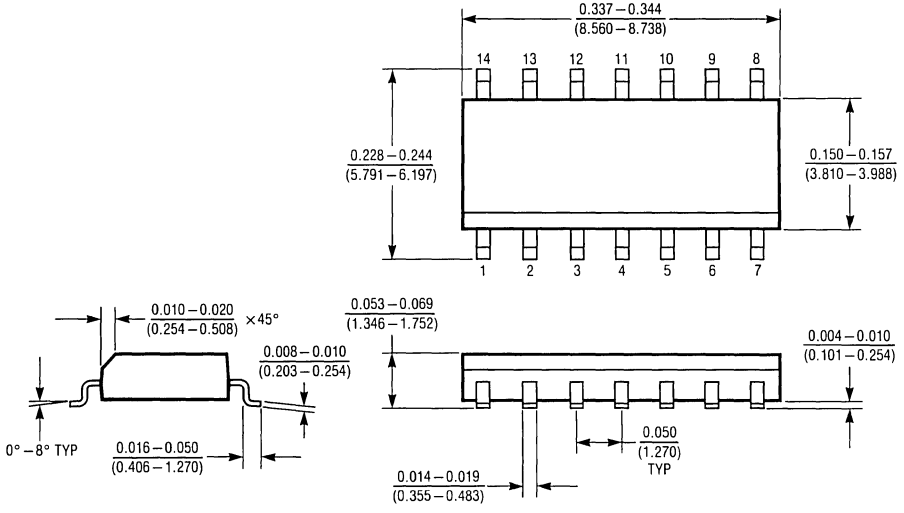


SO Package
8 Lead Small Outline



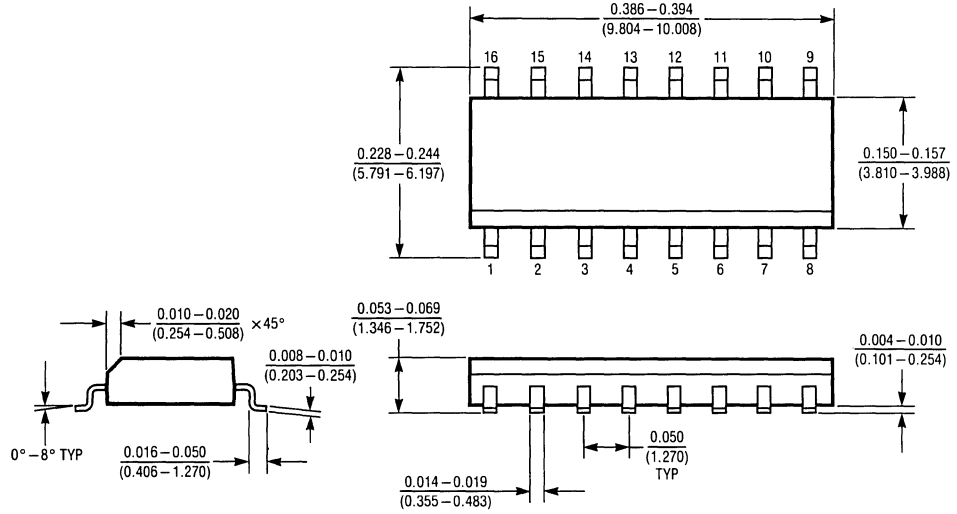
NOTES:
1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

SO Package
14 Lead Small Outline



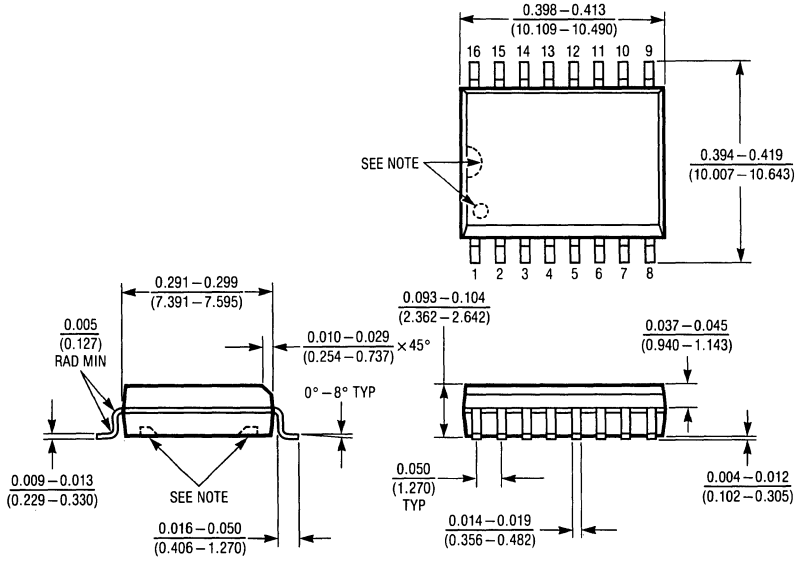
NOTES:
1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

SO Package
16 Lead Small Outline



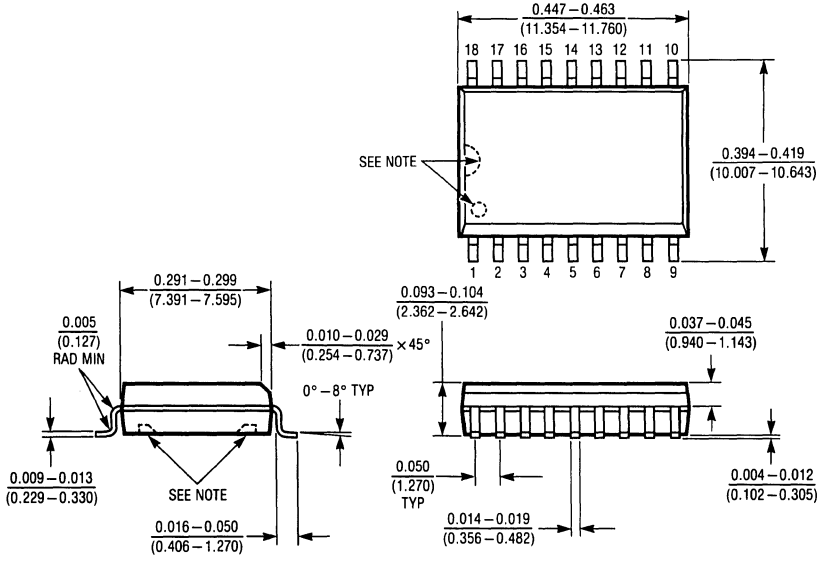
NOTES:
1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

SOL Package
16 Lead Small Outline (Wide)



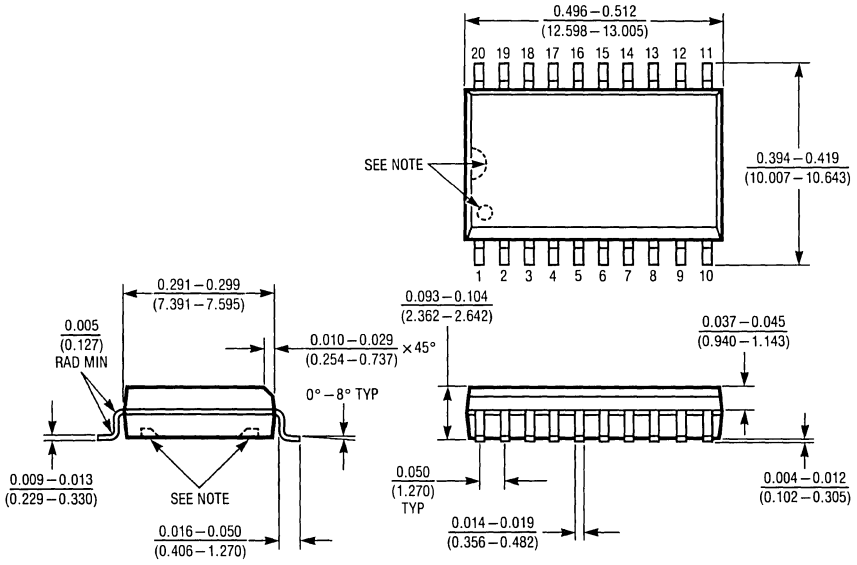
NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGE ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

SOL Package
18 Lead Small Outline (Wide)



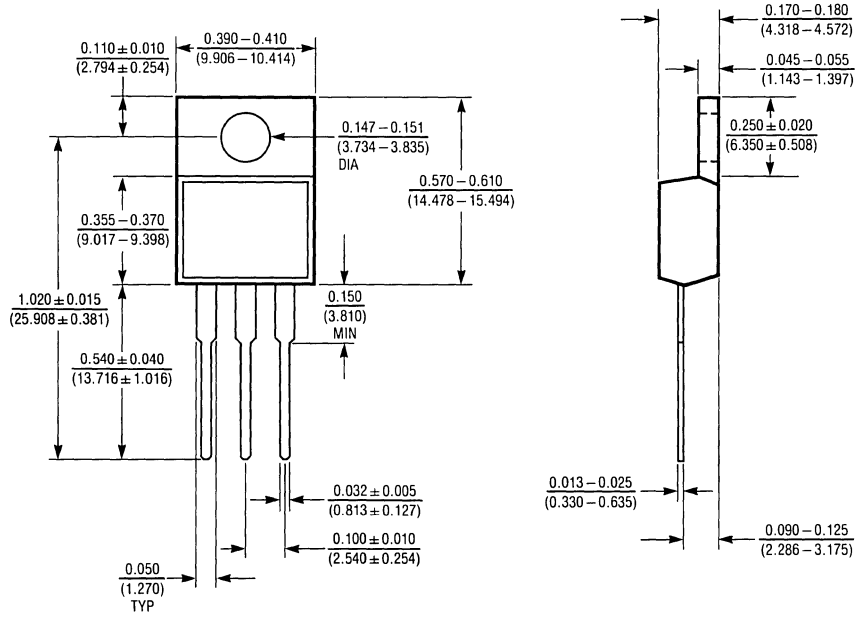
NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGE ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

SOL Package
20 Lead Small Outline (Wide)



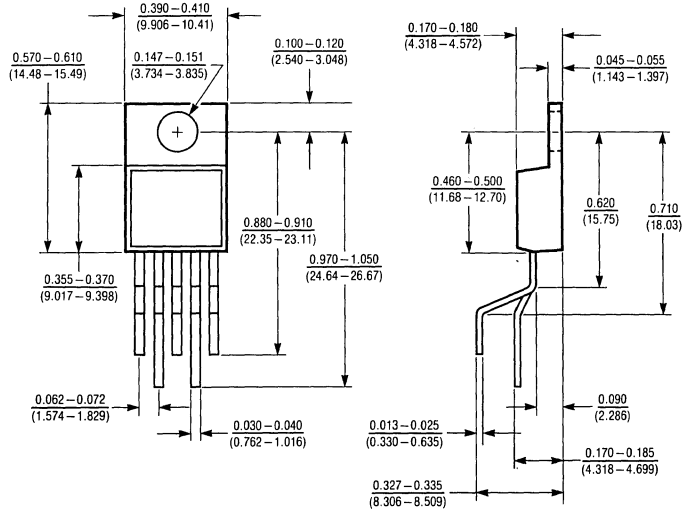
NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGE ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

T Package
3-Lead TO-220

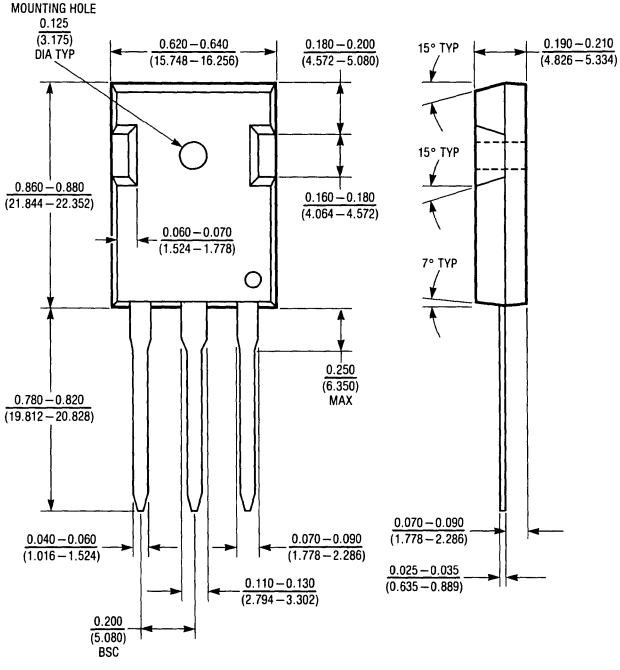


PACKAGE DIMENSIONS

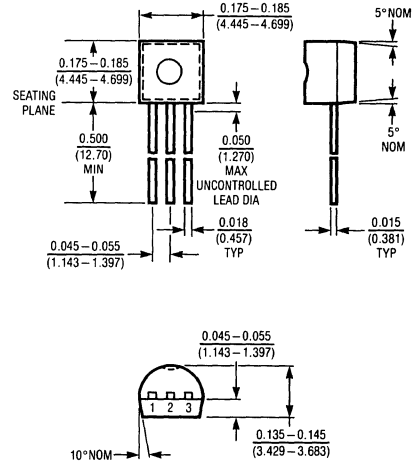
T Package
5 Lead TO-220



P Package
3 Lead TO-247



Z Package
3-Lead TO-92



SECTION 13— APPENDICES

SECTION 13—APPENDICES

Introduction

As integrated circuit technologies achieve higher speed, smaller geometries, lower power and lower voltage, there is a trend toward greater ESD (Electrostatic Discharge Damage) susceptibility. State-of-the-art CMOS ICs can be susceptible to as little as 50V, a static level that is way below the 500V to 15,000V commonly found in an ESD unprotected work environment. As these state-of-the-art ICs get designed into systems, the ESD susceptibility of system hardware also increases proportionately. Industry estimates of losses due to ESD are in the range of a few billion dollars annually.

It has now become increasingly more important for all semiconductor manufacturers and users of semiconductor and other electronic components to fully understand the nature of ESD, the sources of ESD, and its impact on quality and reliability, to effectively deal with this *silent chip killer.*

Linear Technology Corporation has successfully undertaken a simple but effective ESD Protection Program as part of an overall program designed to enhance product quality and reliability. Described in this section are the keypoints of this program.

The objective is to provide increased ESD awareness by showing the sources of ESD in the work environment, and to recommend keypoints for the successful implementation of an ESD program on a company-wide basis.

The end result of a successful ESD program would be the reduction of line failures, final inspection failures and field failures, improved manufacturing yields, improved product quality and reliability and lower warranty costs. We hope that this will help to convince the reader that an ESD Protection Program must be an integral part of every electronic company's product quality and reliability program.

Key Elements of a Successful ESD Protection Program

Recent improvements in failure analysis techniques to correctly identify ESD failures together with an increase in ESD related information from technical publications, EOS/ESD symposiums and vendors have significantly helped to increase ESD awareness.

The ESD Protection Program at Linear Technology Corporation was successfully launched in 1983 when production of ICs was first started. A constant upgrading of the program is still underway. During the ongoing efforts to improve product quality and reliability, previously unrecognized ESD related problems have been brought to light and corrected.

An effective ESD Protection Program must start at product design, and encompass all manufacturing and handling steps up to and including field service and repair.

Since the sources of static in any work environment are similar, key elements of the program successfully implemented at Linear Technology Corporation can also be applied to all users of electronic components. Where these key elements apply, static controls generic to an electronic systems manufacturer are included.

The key elements of a successful ESD Protection Program include:

1. Understanding static electricity.
2. Understanding ESD related failure mechanisms.
3. ESD sensitivity (ESD) testing.
4. Establishing an ESD task force to outline the requirements of the program, sell the program to management, implement the program, review progress against milestones, and follow-up to ensure the program is continuously improved and upgraded. Selecting an ESD coordinator to interface with all departments affected.
5. Conducting a facility evaluation to help identify the sources of ESD and establish static control measures.
6. Setting up an audit program.
7. Selection of ESD protective materials and equipment.
8. Establish a training and ESD awareness program.

What is Static Electricity?

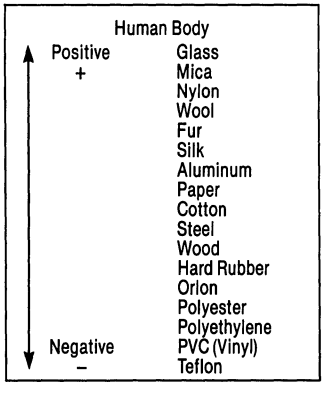
Lightning and sparks from a metallic doorknob during a dry month are examples of static electricity. The magnitude of a static charge is dependent on many variables, among them the size, shape, material composition, surface characteristics and humidity. There are basically three primary static generators, namely triboelectric, inductive and capacitive charging.

Triboelectric Charging

The most common static generator is triboelectic charging. It is caused when two materials (one or both of which are insulators) come in contact and are suddenly separated or rubbed together, creating an imbalance of electrons on the materials and thus static charge.

Some materials readily give up electrons whereas others tend to accumulate excess electrons. The Triboelectric Series lists materials in descending order from positive to negative charging due to this triboelectric effect. A sample triboelectric series is shown here. A material that is higher on the list, e.g., a human body, will become positively charged when rubbed with a material, e.g., polyester, that is lower on the list, due to the transfer of electrons from the human body to the polyester material.

Triboelectric Series



Inductive Charging

Static can also be caused by induction, where a charged surface induces polarization on a nearby material. If there is a path to ground for the induced charge, an ESD event may take place immediately. An example of an induced charge is when the plastic portion of a molded IC package acquires a charge either through triboelectric charging or other means, produces an electrostatic field and induces a charge on the conductive leads of the device. When the device leads are grounded, a short duration damaging static pulse can take place.

Capacitive Charging

The capacitance of a charged body relative in position to another body also has an effect on the static field. To see that this is true, one need only look at the equation $Q = CV$ (charge equals capacitance times voltage). If the charge is constant, voltage increases as capacitance decreases to maintain equilibrium. As capacitance decreases the voltage will increase until discharge occurs via an arc. A low voltage on a body with a high capacitance to ground can become a damaging voltage when the body moves away from the ground plane. For example a 100V charge on a common plastic bag lying on a bench may increase to a few thousand volts when picked up by an operator, due to a decrease in capacitance.

These sources of static can be found almost anywhere in an unprotected work environment, on personnel wearing synthetic clothing and smocks, on equipment with painted or anodized surfaces, and on materials such as carpets, waxed vinyl floors, and ungrounded work surfaces.

Understanding the Failure Mechanisms

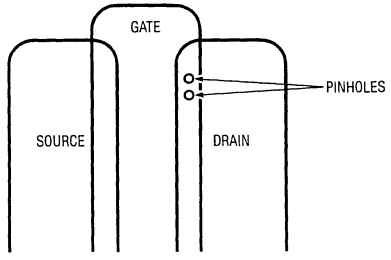
In the past, analysis of electrical failures to pinpoint ESD as a cause was often difficult. But with a better understanding of failure mechanisms and their causes, and the use of more sophisticated techniques like scanning electron microscopy (SEM), pinpointing ESD failures can now be part of a routine failure analysis.

Parametric or functional failure of bipolar and MOS ICs can occur as a result of ESD.

The primary ESD failure mechanisms include:

1. **Dielectric Breakdown:** This is a predominant failure mechanism on MOS devices when the voltage across the oxide exceeds the dielectric breakdown strength. This failure mechanism is basically voltage dependent where the voltage must be high enough to cause dielectric breakdown. As such, the thinner the oxide, the higher the susceptibility to ESD. MOS device failures are characterized by resistive shorts from the input to V_{DD} or V_{SS}.

MOS Transistor Structure
Showing ESD Included Pinholes at Gate Oxide



This failure mechanism can also be found on bipolar ICs which have metallization runs over active semiconductor regions separated by a thin oxide. Device failures are characterized by resistive or high leakage paths.

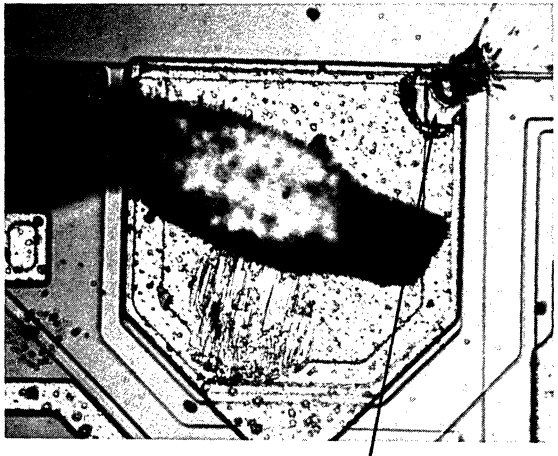
2. **Thermal Runaway (Second Breakdown):** This failure mechanism results in junction melting when the melting temperature of silicon (1415°C) is reached. This is basically a power dependent failure mechanism, namely the ESD pulse shape, duration and energy can produce power levels resulting in localized heating and eventually junction melting, even though the voltage level is below that required to cause dielectric breakdown. Second breakdown of the emitter-base junction of a NPN transistor is a common ESD related failure mode on bipolar ICs, since the highest current density occurs on the smallest current carrying area which is typically the emitter-base junction. Low current gain (h_{FE}) is a very sensitive indicator of emitter-base junction damage on bipolar linear ICs.

3. **Metallization Melting:** When junction melting and a short occurs, localized melting of the metallization can occur if there is enough energy in the ESD pulse. This is frequently a secondary failure mechanism, following a short resulting from one of the other failure modes.

4. **Parametric Degradation:** On precision, high speed ICs (e.g., bipolar operational amplifiers with a typical input bias current of 10pA and low input offset voltage of typically 50μV) ESD can cause device degradation, besides functional failures. This can impact electrical performance and adversely affect device reliability.

   This degradation in device parametric performance is far more difficult to pinpoint as an ESD related failure mode. It is also the least understood among the failure modes. The extent of this degradation is dependent on the number of ESD pulses and the level of damage sustained. The first ESD pulse may not cause an IC to fail the electrical datasheet limits, but with each subsequent ESD pulse, the parametric performance can degrade to the point where the device no longer meets the datasheet limits.

   There is a great deal of current research focused on ESD induced latent failures, and there now appears to be more evidence of this type of failure mechanism.



RESISTIVE SHORT ON A METALLIZATION STRIP OVER A THIN OXIDE N+ REGION ON A BIPOLAR IC

ESD Failure Analysis Program

ESD defect identification must be an integral part of a failure analysis program. The key objectives are to help identify the ESD failure mechanism, isolate the cause for failure, and implement corrective action to prevent recurrence. All devices suspected of being damaged by ESD after initial electrical verification, should be failure analyzed.

An ESD failure analysis program is outlined below.

1. Initial electrical test verification.
2. Review device history to determine if there are any similar failures in the past. Review ESD sensitivity data if available.
3. Investigate conditions in any area that can potentially cause ESD damage. Common potential problem areas include:
   - Proper grounding procedures not being followed (e.g., conductive table/floor mats not grounded, personnel not wearing wrist strap, etc.)
   - Improper handling (e.g., handling devices at a non-ESD protected station)
   - Transporting devices in unapproved containers (e.g., in common plastic bags/tubes/tote boxes)
   - Changes in procedures or operation
   - Changes in equipment
   - Design deficiencies
4. Failure analysis sequence:
   - Bench testing and curve tracer analysis
   - Pin-to-pin analysis
   - Internal visual (10 x to 1000 x)
   - Liquid crystal hot spot detection
   - Scanning electron microscopy (SEM), secondary ion mass spectrometry (SIMS), energy dispersive X-ray analysis (EDX), scanning auger microprobe (SAM)
   - Plasma/chemical etching
   - Special fault decoration
   - Micro-sectioning
   - Documentation

   An excellent failure analysis manual is published by the Rome Air Development Center titled "Failure Analysis Techniques—A Procedural Guide".
5. Duplication of failure by stressing identical devices. The same or similar electrical failure mode is a good indicator of an ESD induced failure mode.
6. Implement corrective action to prevent recurrence. Corrective action may include:
   - Component, board, sub-system or system level redesign
   - Improve ESD controls
   - Improve part handling
   - Improve ESD awareness
   - Improve compliance with ESD protection procedures
   - Increase audit frequencies
   - Improve packaging materials and procedures

   Corrective action taken by the end user should include a thorough review of electrical and mechanical packaging designs. In addition the end user should consult with the IC manufacturer on their findings, request failure analysis of suspected ESD failures if needed and require the IC manufacturer to take appropriate corrective action on any confirmed ESD failure.

ESD Sensitivity (ESDS) Testing

ESDS testing is crucial in helping the IC designer and the end user evaluate the ESD susceptibility of a particular device. At Linear Technology Corporation, ESDS testing is incorporated into the failure anaylsis program and is performed on each device as part of the product characterization program. The ESDS testing is also part of new product qualification. Linear Technology performs this ESDS testing according to MIL-STD-883C, Method 3015.

The ESDS testing provides immediate feedback to the IC designer on any weakness found in the design and permits design correction before product release. The ESDS data collected is also used as baseline data to evaluate the effect of any future design changes on the ESDS testing performance, and to help ensure that the final packaging methods meet MIL-M-38510F requirements. Devices which are classified as Category A devices, susceptible to 2000V or less, on this ESDS testing are top marked with an equilateral triangle per MIL-M-38510F requirements.

Since people are considered to be a prime source of ESD, the ESDS test circuit is based on a human ESD model. A 1500Ω resistor and a 100pF capacitor are used in the test circuit. Human capacitance is typically 50pF to 250pF, with the majority of people at 100pF or less, and human resistance ranges from 1000Ω to 5000Ω. Five combinations of input, output, V^+ and V^- pins are tested. An ESD failure is defined as a voltage level which causes sufficient damage to the device such that it no longer meets the electrical datasheet limits.

After initial ESDS testing, it is important that ESDS test monitoring be performed periodically on devices from various lots to determine lot-to-lot variation. The VZAP-1 report titled "Electrostatic Discharge (ESD) Susceptibility of Electronic Devices" published by the Reliability Analysis Center, Rome Air Development Center, contains a wealth of information on ESDS testing data on devices of different process technologies from many manufacturers. The data in this report clearly indicates a large lot-to-lot variation relating to ESD susceptibility on the same device.

Design for ESD Protection

ESD protection designs employed on Linear Technology Corporation devices include:

1. Input clamp diodes
2. Input series resistors to limit ESD current in conjunction with clamp diodes
3. Keeping critical junctions out of reverse breakdown, or physically enlarging it
4. Eliminating metallization runs over thin oxide regions when they are tied directly to external pins

ESD Task Force

An ESD task force should consist of members from each affected department to do the foundation work, sell the program to management, and implement the program with the following objectives:

1. Develop, approve and implement an ESD control specification covering all aspects of design, ESD protected materials and equipment, and manufacturing
2. Raise the level of ESD awareness
3. Develop a training and certification program
4. Work with all departments on any ESD questions or problems
5. Develop a program to educate and assist sales offices, distributors and customers to minimize ESD
6. Review and qualify new ESD protective materials and equipment, and keep specifications and training program updated
7. Measure the cost-to-benefit ratio of the program

Facilities Evaluation

The ESD task force should be responsible for facility evaluation. This evaluation should be guided by the ESD coordinator. The ESD coordinator should be chosen for strong knowledge of ESD controls, and for the ability to effectively interface with all affected departments. The primary objective of the task force is to pinpoint areas that represent sources of static electricity and potential yield losses due to ESD.

A representative, preferably the engineering or production manager, from each of the key manufacturing areas should be represented on this task force. At Linear Technology Corporation this effort is headed by the Quality Assurance Manager and the Package Engineering Manager. The balance of the ESD task force members are the Test Engineering, Product Engineering, and Production Managers.

The only equipment needed for this survey is a field static meter which measures static up to a level of 50kV. Both nuclear and electronic type static meters are available from manufacturers like 3M, Simco, Wescorp and Scientific Enterprises.

Regardless of area classification, all manufacturing areas can be broken down into the following categories for evaluation purposes.

1. Personnel

Personnel represents one of the largest sources of static, from the type of clothing, smocks and shoes that they wear (for example, polyester or nylon smocks).

2. The Environment

The environment includes the room humidity and floors. Relative humidity plays a major part in determining the level of static generated. For example, at 10-20% RH a person walking across a carpeted floor can develop 35kV versus 1.5kV when the relative humidity is increased to 70%-80%. Therefore the humidity level must be controlled and should not be allowed to fluctuate over a broad range.

Floors also represent one of the greatest contributors of static generation on personnel, moving carts or equipment because of movement across its surface. Carpeted and waxed vinyl floors are prime static generators.

3. Work Surfaces

Painted or vinyl covered table tops, vinyl covered chairs, conveyor belts, racks, carts and shelving are also static generators.

4. Equipment

Anodized surfaces, plexiglass covers, ungrounded solder guns, plastic solder suckers, heat guns and blowers are also static generators.

5. Materials

Look out for common plastic work holders, foam, common plastic tote boxes and packaging containers.

Examples of typical static levels are shown in the table below.

	RELATIVE HUMIDITY	
	70%-80%	10%-20%
Walking across a carpeted floor	35kV	1.5kV
Walking across a vinyl floor	12kV	0.3kV
Picking up a common plastic bag	15kV	0.5kV
Sliding plastic box over bench/conveyor	15kV	2.0kV
Ungrounded solder sucker	8kV	1.0kV
Plastic cabinets	8kV	1.0kV

This ESD survey should include all direct and support manufacturing areas where semiconductor and other electronic components are handled, and should be extended to cover distribution and field sales offices, and field service centers. Once the facility evaluation is completed, the results are reviewed by the ESD task force, and controls are selected to combat each potential ESD problem area.

The ESD Protection Program

The degree of static control should be determined by the most static sensitive device or assembly in the operation. Top management support and implementing the same basic controls in all areas with no double standards will help to ensure success.

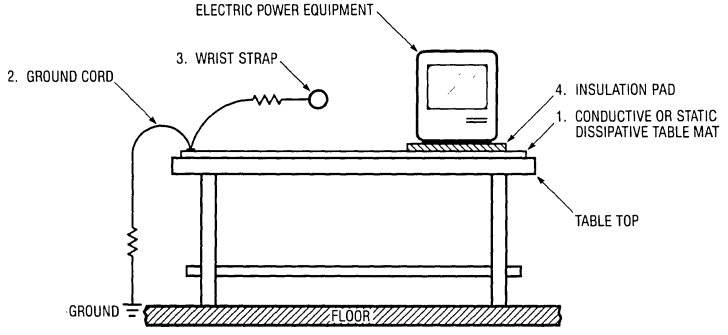
The basic concept of complete static protection is the prevention of static buildup, the removal of any already existing charges, and the protection of electronic components from induced fields. The first and foremost line of defense is the personnel wrist strap together with grounded conductive or static dissipative table tops, and conductive heel straps and grounded conductive or static dissipative floor mats.

To increase ESD awareness at Linear Technology Corporation, all ESD Protection Areas are marked by an identifying label shown below. This label alerts all personnel that ESD protection procedures are enforced in the area.

ESD Protected Workstation

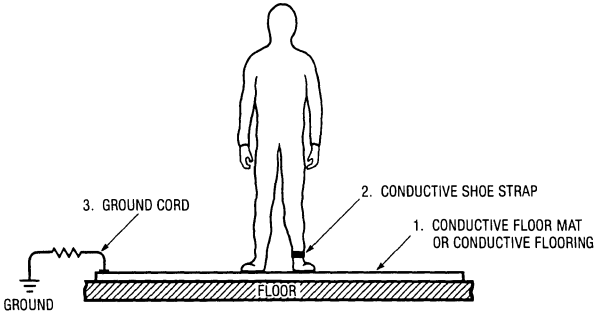
Examples of ESD Protected Workstations are shown in Figures 1 and 2.

Option 1 (Figure 1): All electronic components, sub-assemblies and assemblies must be handled at an ESD Protected Workstation only. The figure illustrates an ESD Protected Workstation consisting of a static dissipative table mat grounded to earth or electrical ground through a 1MΩ series resistor, with the requirement that the operator wears a grounded insulated conductive wrist strap with a 1MΩ series resistor. This 1MΩ series resistor protects the operator from electrical shock, should the operator come in contact with a potentially lethal voltage. Option 1 should be used where the operator does not require a large degree of freedom, e.g., during product inspection, component soldering, board repair, etc.



MATERIALS:
1. 1/16″ THICK CONDUCTIVE OR STATIC DISSIPATIVE TABLE MAT WITH SURFACE RESISTIVITY OF $\leq 10^6\Omega$ PER SQUARE.
2. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ± 10%, AND 18AWG OR LARGER INSULATED WIRE.
3. INSULATED CONDUCTIVE WRIST STRAP WITH 1/4W MINIMUM, 1MΩ ± 10%, AND 20AWG OR LARGER INSULATED WIRE. THE CURRENT LIMITING 1MΩ RESISTOR MUST BE LOCATED RIGHT NEXT TO THE WRIST TO PREVENT THE POSSIBILITY OF SHUNTING THE RESISTOR.
4. POWER TEST EQUIPMENT MUST BE CHASSIS GROUNDED VIA A THREE-PRONG PLUG, AND PLACED ON AN INSULATION PAD MADE OF FORMICA, FIBERGLASS OR EQUIVALENT MATERIAL.

Figure 1



MATERIALS:
1. OPTIONAL 1/8″ THICK CONDUCTIVE OR STATIC DISSIPATIVE MAT OR CONDUCTIVE FLOORING (e.g., CONDUCTIVE FLOOR TILES) WITH A SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
2. CONDUCTIVE SHOE STRAP WITH A SURFACE RESISTIVITY OF $< 10^5\Omega$ PER SQUARE.
3. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ± 10%, AND 18AWG OR LARGER INSULATED WIRE.

Figure 2

Option 2 (Figure 2): Shows an alternate installation method for an ESD Protected Workstation. It consists of a conductive or static dissipative floor mat grounded to earth or electrical ground through a 1MΩ series resistor with the operator wearing a conductive shoe strap. This installation is typically used where the operator needs freedom of movement over a large area, e.g., environmental chamber loading and unloading, electrical testing, etc. To be effective the conductive shoe strap must be attached to the wearer's shoe to maximize contact between the strap and the conductive floor.

Option 3: Utilizes the same conductive or static dissipative floor mat installation as Option 2 with the exception that the operator is grounded via a wrist strap through the equipment ground instead of a conductive shoe strap. It is utilized where an operator is working with a piece of free-standing equipment and does not require a great deal of freedom of movement.

Handling

At Linear Technology Corporation all products are handled, transported and staged in volume conductive tote boxes. This offers maximum protection to the components from triboelectrically generated and inductive static charges. The rule is under no circumstances should components be removed from their approved containers except at an ESD protected workstation.

Final Packaging

Only antistatic and conductive final packaging containers (for example, antistatic or conductive dip tubes, volume conductive carbon loaded plastic bags or metallic film laminate bags, foil lined boxes) are used. Filler (dunnage) material used should be antistatic, non-corrosive, and should not crumble, flake, powder, shred or be of fibrous construction. Conductive packing materials are preferred since they not only prevent buildup of triboelectric charge, but also provide shielding from external fields.

Other ESD Preventative Measures

- Where possible, ban all static bearing materials, e.g., common plastics, styrofoam from the work environment.
- Use only synthetic material smocks with 1% to 2% interwoven steel.
- Ensure all electronic and electro-mechanical equipment is chassis grounded, including conveyor belts, vapor degreasers and baskets, solder pots, etc.
- Tips of hand soldering irons are to be grounded.
- All parts of hand tools (e.g., solder suckers, pliers, etc.) which can be expected to come in contact with electronic components are to be made of conductive material and grounded.
- Conductive shorting bars are to be installed on all terminations for PC boards with electronic components during assembly, loading, inspecting, repairing, soldering, storing and transporting.
- All PC boards with electronic components are not to be handled by their circuitry, connector points or connector pins.
- High velocity air movement is to be delivered through a static neutralizer.
- Air ionizers are to be employed in neutralizing static buildup on insulators if they have to be used or as an extra precautionary measure for extremely sensitive assemblies.
- Do not slide electronic components over a surface.

Air ionizers come in three basic types: nuclear, AC and pulsed DC. These ionizers can neutralize static charges on non-conductive materials by supplying the materials with a stream of both positive and negative ions.

The advantage of the AC or pulsed DC type air ionizer is that there is no recurring annual replacement cost. The disadvantages are: it emits ozone which can damage rubber in equipment; EMI (Electro Magnetic Interference); and an imbalance in the stream of ions if not properly maintained, therefore necessitating frequent preventive maintenance.

The advantages of the nuclear type air ionizer are low maintenance, no ozone, no EMI and no imbalance problems. The disadvantages are that it requires careful handling because of the radioactive source, and the annual recurring cost to replace the radioactive source.

The selection of air ionizers must be done with care with awareness of the above limitations. The squirrel cage ionized air blower has been proven to produce a significantly more even distribution of ion patterns than does a conventional fan blower design.

Maintenance

ESD protective floor and table coverings must be properly maintained. Do not wax over them. Cleaners must not degrade their electrical properties. Vacuum to remove loose particles, followed by a wet mop with a solution of mild detergent and hot water.

Periodic Audits

At Linear Technology Corporation periodic audits are conducted to check on the following at least once a month, unless otherwise noted.

- Compliance with ESD control procedures.
- Ensure that the conductive ground cord connection is intact by measuring the series resistance to ground with an ohmmeter.
- Ensure that wrist straps are still functional by measuring the resistance from the person to ground. The ground lead of the ohmmeter is connected to the ground connection of the wrist strap, and the positive lead is connected to a stainless steel electrode (one inch in diameter, and three inches long #304 stainless steel) which is held by the person. This test method not only checks the resistance of the series resistor, but also resistance through the ground cord and also any contact resistance between the wrist strap and the person's skin. This test procedure is required when wrist straps with an elastic nylon band with interwoven metallic strands are used, since the metallic strands breakdown with prolonged use. This monitor frequency may be shortened depending on audit results.
- Measure the surface resistivity of conductive or static dissipative table tops once every 6 months using ASTM-F-150-72, ASTM-D-257 or ASTM-D-991 test methods as appropriate.

Materials Selection and Specification

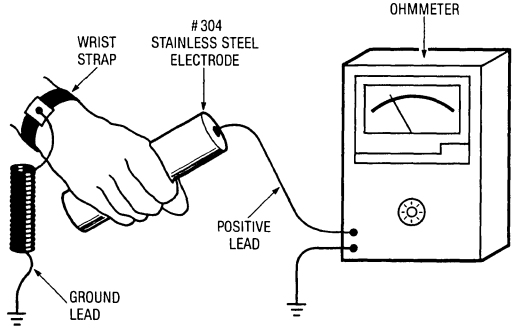
Based on the tremendous amount of ESD protective materials available, it is important that materials are selected based on a stringent qualification. Once the materials have been selected and specifications defined, a material procurement specification needs to be initiated that defines the materials and quality requirements to the vendor. One of the major pitfalls is to procure material in haste, e.g., a wrist strap, only to find out it does not perform reliably.

The SOAR-1 report titled "ESD Protective Material and Equipment: A Critical Review" published by the Rome Air Development Center is an excellent reference on the various types of ESD protective materials available.

At Linear Technology Corporation a minimum of three manufacturing lots from a potential vendor are subjected to qualification testing per the requirements of the material procurement specification for ESD protective materials. The vendor is considered qualified only when all three lots are found to be acceptable. Once vendors have been qualified, all incoming ESD protective materials are subjected to a stringent incoming inspection.

The following table summarizes a sample material and test specification for ESD protective materials.

Wrist Strap Resistance Test Set-Up



MATERIAL	PROPERTIES/DESCRIPTION	TEST METHODS
Wrist Strap	• Insulated coil cord with a 1MΩ ± 10%, ¼W minimum series resistor molded into snap fastener (at wrist end), and an elastic wrist band with inner metallic filaments and insulative exterior.	Measure series resistance with ohmmeter. Apply normal tug to both ends of strap and remeasure series resistance. Resistance must be between 0.8 to 1.2MΩ.
Conductive or Static Dissipative Table and Floor Coverings, Conductive Tote Boxes, Conductive Shoe Straps	• Must not shed particles • Must not support bacterial or fungal growth • Conductive: surface resistivity $<10^5$Ω/square. Static Dissipative: surface resistivity $>10^5$ and $<10^9$Ω/square.	Test per ASTM-F-150-72, ASTM-D-257, ASTM-D-991 (for surface resistivity $<10^6$Ω/square).
Conductive Foam	• Shall not contain more than 30ppm C1, K, Na when a quantitative chemical analysis is performed • Must not support bacterial or fungal growth	With devices inserted into the foam, the foam must not cause lead corrosion after a 24 hour 85°C/85% RH temperature/humidity storage.
Antistatic and Conductive Dip Tubes	• Must not exhibit an oily-like film	Must meet an Electrostatic Decay test per Federal Test Method Standard 101 Test Method 4046. Material charged to 5000V must be discharged to 1% of its initial value (50V) in 2 seconds after a 24 hour conditioning at 15% relative humidity.
Antistatic and Conductive Bags	• Antistatic bags must meet MIL-B-81705 type 2 • Conductive bags must meet MIL-B-117 and sealing requirements of MIL-B-81705 • Must not support bacterial or fungal growth	Test method for antistatic bags same as for antistatic/conductive dip tubes. Test method for conductive bags same as for conductive table/floor coverings.
Static Eliminators/Ionized Air Blowers	• Ozone level: 0.1ppm maximum for 8 hour exposure • Noise: 60dB maximum • EMI: non-detectable when measured 6 inches away	Voltage Decay test: A non-conductive sheet of material charged to 5kV must be discharged to 1% of its initial value (50V) in 2 seconds at a distance of 2 feet from the ionizer or larger distance if application calls for a larger distance.

Training and Certification Program

The training program should be developed to increase ESD awareness and to assist all personnel in complying with the ESD control specification. The program should include:

1. A discussion on "What is Static Electricity?"
2. How ESD affects ICs
3. Estimated cost of ESD related losses
4. Materials and equipment for controlling static
5. The importance of wearing the wrist strap
6. The importance of an audit program
7. Encourage floor personnel to feedback any ESD potential areas to the ESD task force

ESD training should be incorporated into the personnel training and certification program. At Linear Technology Corporation only fully trained and certified personnel are allowed to do actual production work. To help increase ESD awareness, it is often a good idea to show ESD awareness films and video tapes which are available from a variety of sources (Reference 3 provides a list of films and video tapes). Personnel are retrained and recertified at a minimum frequency of once per year.

Measuring the Benefits

Where possible, the benefits of an ESD Protection Program should be tracked and quantified. The two yardsticks used at Linear Technology Corporation are final test yields and QA electrical average outgoing quality (AOQ). Since the implementation of this program, there has been a significant improvement in final test yields especially on static sensitive CMOS devices. With the elimination of ESD as a potential failure cause, the electrical AOQ has averaged well under 100ppm for all products combined. Improvements such as this help to provide positive feedback to manufacturing and support personnel on the importance of an ESD Protection Program, and also help to ensure its continuing success.

References

1. DOD-STD-1686 — Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment.
2. DOD-HDBK-263 — Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment.
3. SOAR-1 — State-of-the-Art Report ESD Protective Materials and Equipment: A Critical Review, published by the Rome Air Development Center.
4. VZAP-1 — Electrostatic Discharge (ESD) Susceptibility of Electronic Devices published by the Rome Air Development Center.
5. EOS-1, EOS-2, etc. — Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1979 to current year.
6. MIL-STD-883C — Test Methods and Procedures For Microelectronics
7. MIL-M-38510F — Microcircuits, General Specification for
8. MIL-M-55565A — Microcircuits, Packaging of
9. MIL-M-81705B — Barrier Materials, Flexible, Electrostatic—Free, Heat Sealable
10. FED-STD-101 — Preservation, Packaging and Packing Materials Test Procedures; Test Methods. 4046: Electrostatic Properties of

AN1 **Understanding and Applying the LT1005 Multifunction Regulator**
This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.

AN2 **Performance Enhancement Techniques for 3-Terminal Regulators**
This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.

AN3 **Applications for a Switched-Capacitor Instrumentation Building Block**
This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F to V and V to F converters, 12-bit A to D converter and more.

AN4 **Applications for a New Power Buffer**
The LT1010 150μA power buffer is described in a number of useful applications such as boosted op amp, a feed-forward, wideband DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.

AN5 **Thermal Techniques in Measurement and Control Circuitry**
6 applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, an anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.

AN6 **Applications of New Precision Op Amps**
Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.

AN7 **Some Techniques for Direct Digitization of Transducer Outputs**
Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.

AN8 **Power Conditioning Techniques for Batteries**
A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.

AN9 **Application Considerations and Circuits for a New Chopper-Stabilized Op Amp**
A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.

AN11 **Designing Linear Circuits for 5V Operation**
This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.

AN12 **Circuit Techniques for Clock Sources**
Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.

AN13 **High Speed Comparator Techniques**
The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz-30MHz V to F converter, a 200ns 0.01% sample-hold and a 10MHz fiber optic receiver. Five appendices covering related topics complete this note.

AN14 **Designs for High Frequency Voltage-To-Frequency Converters**
A variety of high performance V to F circuits is presented. Included are a 1Hz to 100MHz design, a quartz stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output and non-linear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V to F conversion.

AN15 **Circuitry for Single Cell Operation**
1.5V powered circuits for complex linear functions are detailed. Designs include a V to F converter, a 10 bit A→D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section on component considerations for 1.5V powered linear circuits.

AN16 **Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers**
This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.

AN17 **Considerations for Successive Approximation A→D Converters**
A tutorial on SAR type A→D converters, this note contains detailed information on several 12-bit circuits. Comparator, clocking, and pre-amplifier designs are discussed. A final circuit gives a 12-bit conversion in 1.8μs. Appended sections explain the basic SAR technique and explore DAC considerations.

AN18 **Power Gain Stages for Monolithic Amplifiers**
This note presents output stage circuits which provide power gain for monolithic amplifiers. The circuits feature voltage gain, current gain, or both. Eleven designs are shown, and performance is summarized. A generalized method for frequency compensation appears in a separate section.

AN19 **LT1070 Design Manual**
This design manual is an extensive discussion of all standard switching configurations for the LT1070; including buck, boost, flyback, forward, inverting and "Cuk". The manual includes comprehensive information on the LT1070, the external components used with it, and complete formulas for calculating component values.

AN20 **Applications for a DC Accurate Low-Pass Switched-Capacitor Filter**
Discusses the principles of operation of the LTC1062 and helpful hints for its application. Various application circuits are explained in detail with focus on how to cascade two LTC1062's and how to obtain notches. Noise and distortion performance are fully illustrated.

AN21 **Composite Amplifiers**
Applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. AN21 shows examples of composite approaches in designs combining speed, precision, low noise and high power.

AN22 **A Monolithic IC for 100MHz RMS-DC Conversion**
AN22 details the theoretical and application aspects of the LT1088 thermal RMS-DC converter. The basic theory behind thermal RMS-DC conversion is discussed and design details of the LT1088 are presented. Circuitry for RMS-DC converters, wideband input buffers and heater protection is shown.

AN23 **Micropower Circuits for Signal Conditioning**
Low power operation of electronic apparatus has become increasingly desirable. AN23 describes a variety of low power circuits for transducer signal conditioning. Also included are designs for data converters and switching regulators. Three appended sections discuss guidelines for micropower design, strobed power operation and effects of test equipment on micropower circuits.

AN24 **Unique Applications for the LTC1062 Lowpass Filter**
Highlights the LTC1062 as a lowpass filter in a phase lock loop. Describes how the loop's bandwidth can be increased and the VCO output jitter reduced when the LTC1062 is the loop filter. Compares it with a passive RC loop filter.

Also discussed is the use of LTC1062 as simple bandpass and bandstop filter.

AN25 **Switching Regulators for Poets**
Subtitled "A Gentle Guide for the Trepidatious", this is a tutorial on switching regulator design. The text assumes no switching regulator design experience, contains no equations, and requires no inductor construction to build the circuits described.

Designs detailed include flyback, isolated telecom, off-line, and others. Appended sections cover component considerations, measurement techniques and steps involved in developing a working circuit.

LINEAR TECHNOLOGY CORPORATION

1630 McCarthy Blvd., Milpitas, CA 95035
Phone: (408) 432-1900
FAX: (408) 434-0507
Telex: 499-3977

IM/GP/BC 1187 50M